Medipix2, a 64k pixel readout chip with 55 mm square elements working in single photon counting mode[1]

X. Llopart[2], M.Campbell[2], R. Dinapoli[2], D. San Segundo[3], E. Pernigotti[2,4]

***Abstract*-- The *Medipix2* chip is a pixel detector readout chip consisting of 256 x 256 identical elements, each working in single photon counting mode for positive or negative input charge signals. Each pixel cell contains around 500 transistors and occupies a total surface area of 55 μm x 55 μm. A 20 μm width octagonal opening connects the detector and the preamplifier input via bump-bonding. The preamplifier feedback provides compensation for detector leakage current on a pixel by pixel basis. Two identical pulse height discriminators are used to create a pulse if the preamplifier output falls within a defined energy window. These digital pulses are then counted with a 13-bit pseudo-random counter. The counter logic, based in a shift register, also behaves as the input/output register for the pixel. Each cell also has an 8-bit configuration register which allows masking, test-enabling and 3-bit individual threshold adjust for each discriminator. The chip can be configured in serial mode and readout either serially or in parallel. The chip is designed and manufactured in a 6-metal 0.25 μm CMOS technology. First measurements show an electronic pixel noise of 140 e^- rms and an unadjusted threshold variation around 360 e^- rms**

I. Introduction

Advances in CMOS technology open up new possibilities in particle detection and imaging. In recent years particle physics experiments have been transformed by the introduction on ASIC circuits particularly for tracking detectors. Pixel detectors have become key components in tracking systems especially in high multiplicity environments where excellent spatial resolution is combined with extremely high signal to noise ratios allowing physicists to find traces of rare particle tracks in very complicated events [1]. At the same time investigations have been continuing into the adaptation of this technology to X-ray imaging applications. In particular this technology enables the counting of particles which are deposited in each pixel. A first large prototype chip, the Photon Counting Chip (PCC or Medipix1) [2], has been successfully developed and measured. This chip demonstrated that the photon counting approach provides images with excellent dynamic range which are practically free of non-photonic noise [3,4]. The performance of the system was limited mainly by the size of the pixel (170 μm x 170 μm) which was determined by the component density of the 1 μm CMOS process used.

Encouraged by these results we decided to make a new version of the chip in a 0.25 μm CMOS technology. Each pixel measures only 55 μm by 55 μm and contains around 500 transistors. This reduction in pixel dimension is possible because of the tiny dimensions of the individual transistors as well as the high number of metal interconnect layers. The new system provides a spatial resolution comparable to that achieved by much simpler integrating readout systems whilst keeping excellent signal-to-noise and dynamic range, inherent properties of the photon counting method. Moreover, some new features could be included in the pixel cell: leakage current compensation on a pixel by pixel basis, sensitivity to carriers of both types and an energy windowed discriminator.

The architecture and functional behavior of Medipix2 chip are described in this paper. First preliminary measurements are presented. Some new ideas for future pixel detectors are explained at the end of this paper.

II. Chip description

The Medipix2 chip has been designed to minimize the dead area between chips covering large areas when butting several chips together. This is achieved placing the *periphery* at the bottom of the chip, and minimizing the *non-sensitive area* in the other three edges to less than 50 μm. Figure 1 shows the *Medipix2* floor plan organization. The *sensitive area* (top box) is arranged as a matrix of 256 x 256 pixels of 55 x 55 μm^2 resulting in a detection area of 1.98 cm^2 which represents 87% of the entire chip area. The periphery (bottom box) contains 13 8-bit DACs and the Input/Output control logic. There are 5 lateral IO wire-bonding pads which can be used to make a daisy chain of chips. In a multi-chip detector there would be no dead area between neighbouring chips except two 200 μm wide pixel rows and columns.

Both the analog and digital circuitry have been designed to operate with independent 2.2 V power supplies with a total analog power consumption of about 500 mW. The chip contains around 33 million transistors.

[1] This project has been undertaken in the framework of the Medipix2 Collaboration. http://www.cern.ch/MEDIPIX

[2] CERN 1211 Geneva 23, Switzerland

[3] NIKHEF Kruislaan 409, 1098 SJ Amsterdam, The Netherlands

[4] University and INFN of Pisa, Italy, now at ST Microelectronics, Milano, Italy

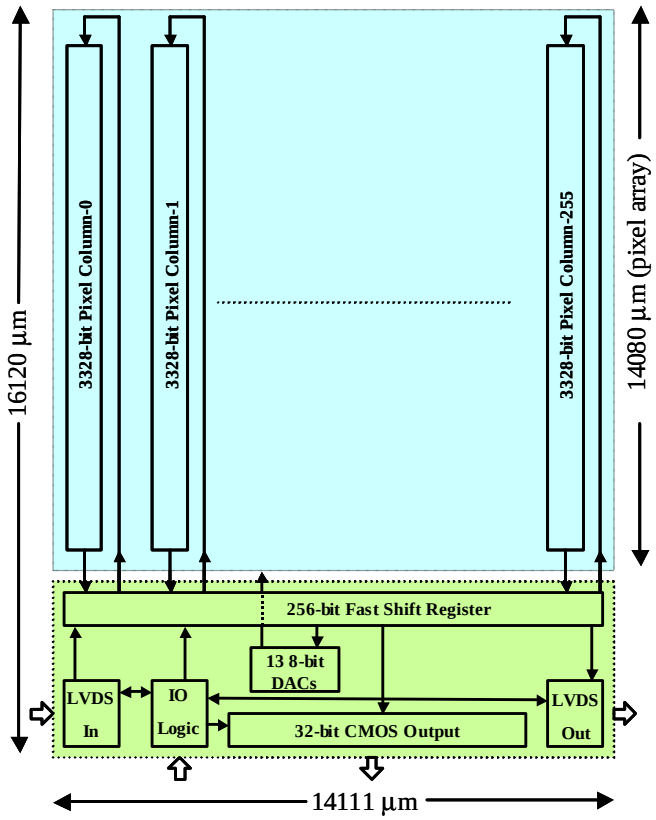

Figure 1: Schematic floorplan of the Medipix2 chip.

A. *The Pixel Cell*

When a charged particle interacts in the detector material it deposits a charge which drifts towards the collection electrode. This charge is then amplified and compared with two different thresholds that form an energy window. If the detected charge falls inside this energy window the digital counter is incremented.

The pixel has two working modes depending on the CMOS input *Shutter* state. When the *Shutter* signal is low the pixel is in acquisition mode. In this case, the output of the double discrimination logic (see II.A.2) is used as the clock of the counter [5]. When the *Shutter* is high an external clock is used to shift the data from pixel to pixel (see II.A.3). Each pixel has eight independent configuration bits. Six of them are used for the fine threshold adjustment (three bits foe each discriminator), one for masking noisy pixels, and one to enable the input charge test through the 8 fF on-pixel capacitance.

Figure 2 shows the schematic of the Medipix2 pixel cell. The analog side contains a charge preamplifier with DC leakage current compensation, a test capacitance, and two branches of identical discriminators. The digital side contains the Double Discriminator Logic (DDL) and the 13-bit shift register. The dimensions of the cell are 55 x 55 μm^2. Each pixel has 504 transistors and a static power consumption of ~ 8 µW. The octagonal bump bond opening, placed on top of the analog side, has a diameter of 20 µm. In Figure 3 the layout of the pixel cell is shown where the most important blocks are confined in a box.

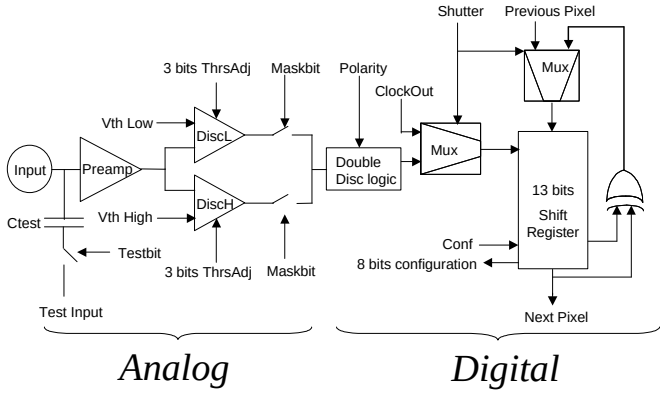

Figure 2: Medipix2 pixel cell schematic.

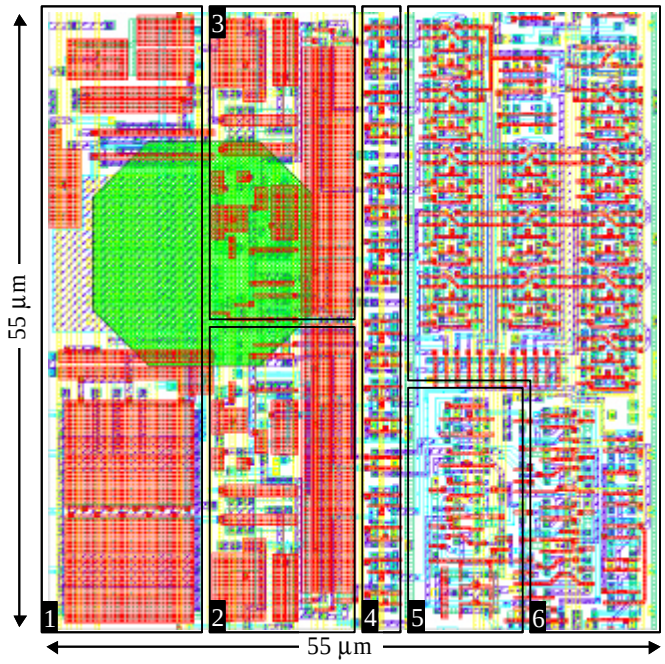

Figure 3: Medipix2 pixel cell layout. 1:Preamplifier. 2: High Threshold discriminator. 3: Low level discriminator. 4: 8-bit configuration register. 5:Double discriminator logic. 6: Shift Register and control logic.

1) *The charge Preamplifier*

The preamplifier follows the scheme proposed by Krummenacher [6] based on a differential CMOS amplifier as shown in Figure 4. A differential input amplifier was chosen for better rejection of substrate and power supply noises.

This configuration provides a constant current fast return to zero through the transistors M1a and M1b controlled by the *IKrum* current DAC. The M2 transistor compensates the detector DC leakage current. Positive leakage currents (hole collection) smaller than *IKrum* and negative (electron collection) smaller than *IKrum/2* can be compensated in each pixel. Another voltage DAC controls the Vfbk node. This node sets the DC output voltage optimizing the dynamic range depending whether holes or electrons are being collected. The polarity of collection is selected using the *Polarity* input pad at the DAC level. The change of this voltage affects the overall gain of the preamplifier due to the

change in the biasing point, resulting in slightly different gains for the two collection modes.

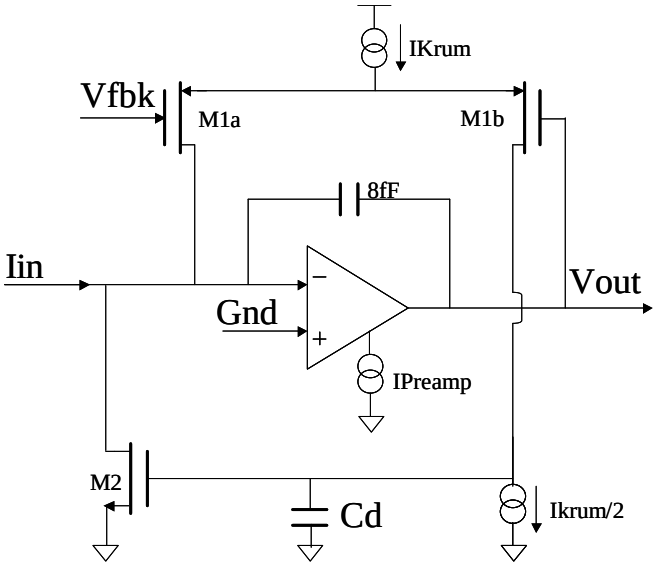

Figure 4: Preamplifier scheme.

2) The Discriminator

The output of the preamplifier feeds two identical discriminators which have a linear behaviour up to 80 ke⁻. These two branches are independent and the discrimination energy can be set differently depending on the application. The difference between the two energy levels ($W_{th}=V_{thHigh} - V_{thLow}$), defines the energy window (W_{th}) into which the incoming particle energy has to fall in order to increment the counter. This window discrimination is performed by the DDL (*Double Discrimination Logic*).

If the V_{thHigh} is set to be smaller than V_{thLow}, the DDL works in single discrimination mode, and the counter is incremented when the incoming particle energy exceeds the V_{thLow} threshold.

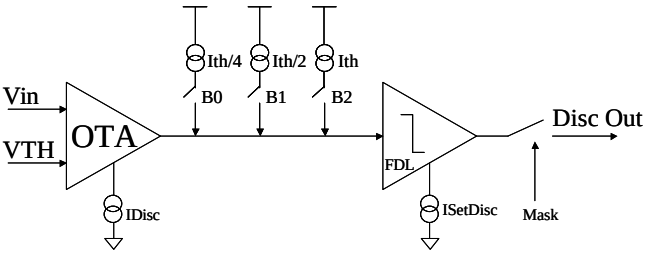

Figure 5: Discriminator scheme

In Figure 5 only one discriminator branch is shown. Each branch includes a differential amplifier configured to work as an OTA (*Operational Transimpedance Amplifier*), three independent selectable current sources to minimize the spread of the threshold distribution from pixel to pixel, and a current discriminator. The output can be masked in case of malfunction or excessive noise.

3) The Shift Register

The shift register has two modes depending on the state of the *Shutter* signal. When the *Shutter* is low the shift register works as a pseudo-random counter of 13 bits with a dynamic range of 8001 counts. Every pulse coming from the discriminator logic increments by one the counter value. When the *Shutter* is high an external clock can be used to shift the data from pixel to pixel. This mode is used both for setting the 8 configuration bits and for reading the 13-bit counter information.

4) The Periphery

The periphery contains;

- 13 8-bit DACs [7] which set the different bias voltages in the chip;
- A 256-bit FSR (*Fast Shift Register*) used to write in or readout the sensitive area;
- 127 Input/Output pads;
- LVDS drivers and receivers;
- IO logic that controls the chip.

When the matrix is accessed to perform any IO operation the data is organized in 256 columns of 256x13 bits. Therefore each chip has 851968 bits to be read or written for any matrix IO operation. The *Medipix2* uses a high-speed *LVDS* (*Low Voltage Differential Signaling*, [8]) logic for configuration and readout of the chip in serial mode. Also a parallel 32-bit single-ended CMOS bus is present for applications requiring even higher frame rates. The readout can be performed serially by using the LVDS output drivers or in parallel by means of the 32-bit CMOS bus. The setting of the configuration register in the entire matrix and of the 13 8-bit DACs is always done serially through the LVDS receivers. Using a clock of 100 MHz the entire matrix is readout in less than 9 ms through the serial port, while using the parallel option the readout is done in 266 μs.

III. Measurements

Preliminary measurements were performed using an *IMS ATS* digital IC tester. All of the logic at the chip periphery (see Figure 1) performed without error at 100 MHz, which is the highest clocking frequency available on the IC tester. The setting of the DACs, the Fast Shift Register, the peripheral control logic, the 32-bit CMOS bus and the *LVDS* drivers and receivers performed without errors.

A first characterization of the pixel front-end has been achieved by applying a test pulse to the on-pixel injection capacitance of several pixels. Output pads from a 3 x 3 pixel cluster of the active matrix have been provided to allow direct testing. Each of the preamplifier outputs of these test pixels and one digital output resulting from OR-gating the 9-discriminator outputs are accessible via output pads in the chip. An example of these test outputs is seen in Figure 6. Using these test pads and reading the pixel counter information the pixel cell can be characterized. Table 1

summarizes these measurements. All the sub-blocks of the pixel cell perform as in simulation.

Depending on the collection type different bias conditions of the amplifier are used achieving different results in gain and linearity. For deposited charges smaller than 50 ke^- a maximum count rate of 1 MHz per pixel is obtained without pile-up following the specifications.

The electronic noise is measured using the s-curve method [9] because of the poor precision in the measurement of the preamplifier noise at its output. This method gives information of the noise in all the front-end chain. Having a fixed threshold an input charge is swept from no counter counts (under threshold) to 100% hits, creating an s-shaped curve. The effective threshold is at 50% of this s-curve. The charge difference between the 97.75% and 2.25% of the s-curve is four times the RMS noise of the front-end assuming gaussian distributed noise. Having a double discriminator system, an electronic noise for each branch can be given. One is generated when the injected charge crosses the *Vth Low* threshold (σ_{nL}), and the second when crossing the *Vth High* threshold (σ_{nH}). The threshold dispersion in one row is also shown for both threshold crossings (σ_{nTHL},σ_{nTHH}). The threshold dispersion between pixels can be later corrected adjusting the 3-bit threshold fine-tuning present in each discriminator branch.

TABLE 1: PREAMPLIFIER MEASURED CHARACTERISTICS

	Electron Collection	Holes Collection
Gain	*12.5 mV/ke⁻*	*13.25 mV/ ke⁻*
Non linearity	*<3% to 100 ke⁻*	*<3% to 80 ke⁻*
Peaking time	*<150ns*	
Return to baseline	*<1µs for Qin <50 ke⁻*	
Electronic Noise	σ_{nL}*~ 141 e⁻* σ_{nH}*~ 200 e⁻*	
Threshold dispersion in 1 row	σ_{nTHL}*~ 360 e⁻* σ_{nTHH}*~ 800 e⁻*	
Analog power dissipation	*~8 µW/channel for 2.2V supply*	

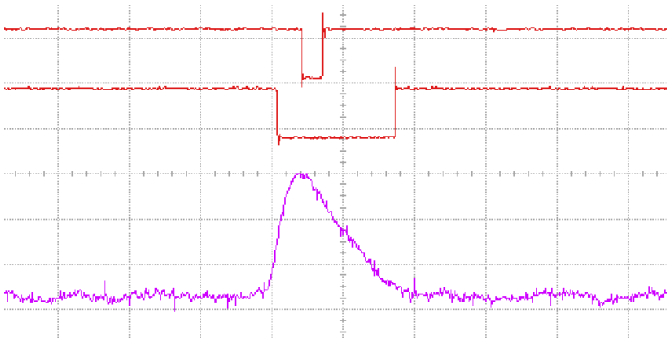

Figure 6: Preamplifier analog output response to an injected charge of 17200e^- (bottom), and discriminator digital output with threshold setting at 16400e^- (top) and 6300e^- (middle). X=500ns, Y_{analog}=50mV, $Y_{digital}$=2V.

A radiation hardness measurement of *Medipix2* has been made using a dedicated machine (*Seifert RP149*). The target material used in the tube was tungsten and the X-ray energy peaked at 10 keV. Doses of 3.9 krad/min up to 150 krad and 8.04 krad/min from 150 krad to 500 krad were applied to the chip. An increase of the analog power supply current was observed from 200 mA to 260 mA, while a knee at around 200 krad was observed in the digital power supply, which feeds more than the 90% of the chip transistors. The chip worked properly up to 300 krad but with an overall increase of the power supply currents. After an irradiation of 500 krad the chip was annealed (1 week at 100°C) and it recovered to pre irradiated values.

IV. FUTURE DEVELOPMENTS

When using the *photon counting* method with very small pixel cells (less than about 100 µm side), the phenomenon of *charge sharing* has to be addressed [10]. The photon interaction with the detecting medium convoluted with diffusion gives rise to an extended cloud of charge, whose lateral dimension might reach a size comparable to the pixel pitch. The study of energy deposition in segmented sensors and the signal formation in pixel detectors with different geometries will be the subject of numerous future studies.

At this point a short description of some aspects can be given already. We describe two different approaches to reduce or cancel the effects of *charge sharing*, one at the detector level and the other one at the electronics level.

A. *Proposed detector solution*

In a 3x3 square pixel matrix the distance between the central pixel and the orthogonal pixels is shorter than to the diagonal pixels. Using hexagonal pixels, as shown in Figure 7, one can create an homogeneous environment for each pixel, with six equivalent neighbors. By doing this, the distance between neighboring pixels is constant in all directions achieving a much better spatial uniformity than square pixels.

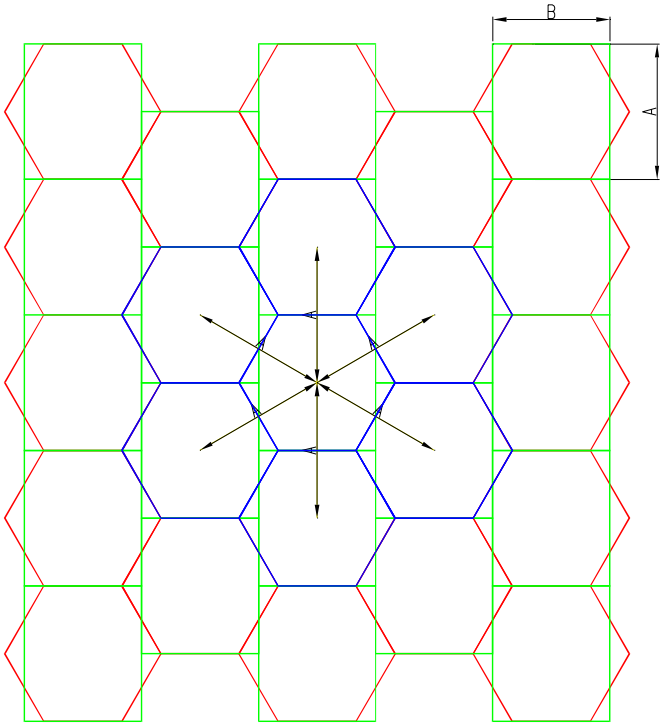

Figure 7: Proposed detector layout. B=3A/2√3

This homogeneity in the sensor can only be achieved at the cost of more complexity in the readout. In order to physically match the hexagonal detector with the electronics, the pixel cells at the electronics level must be rectangular, as shown in Figure 7. Moreover from column to column they have to be shifted up or down half a cell.

B. *Proposed electronic solution*

Charge sharing is related to the comparator threshold at the electronics level: as soon as the charge collected on one pixel falls below the threshold the hit will be ignored. Thus, in practice, the threshold would have to be set low enough to still increment the pixel's counter with the bigger fraction of collected charge without counting the event more than once. Consequently one would lose one advantage of a very precise threshold setting close to the incident photon energy. The other possibility of simply accepting the lower detection efficiency would imply an increased dose to patients and is therefore undesirable for medical applications. Assuming that the *charge sharing* effect only happens between adjacent pixels, a charge sharing control system can be built using the information coming from the 6 surrounding pixels and comparing it with the central pixel creating a 7-pixel cluster cell, as shown in Figure 7.

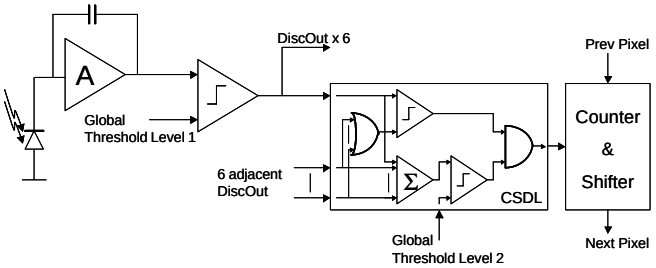

Figure 8: Scheme of the proposed solution to take into account charge sharing effects.

In the proposed scheme of Figure 8 the pixels in the cluster share the information of their discriminator output pulse (*DiscOut*). A voltage level discriminator generates this pulse with a threshold level set to a fixed value in the entire pixel matrix, slightly higher than the amplifier electronic noise (typically 3 times higher). The discriminator output pulse length is proportional to the charge of the detected particle in this case. Two items of useful information can be obtained from the local pulse and the six neighboring pixels pulses. First, if the local pulse length is longer than any of the other six neighboring pixel pulses, then the local pixel collected the biggest *share* of charge generated by the incoming detected particle. This gives information of the position where the particle converted with an error smaller than $2A/\sqrt{3}$ with respect to the pixel centroid (where A is the apothem of the hexagonal pixel). Second, adding up all the discriminator pulses, one can get the total deposited charge in this 7-pixel cluster, which is compared with a global threshold level (*Global Threshold Level2*) in order to count only the photons with energies higher than the fixed threshold. These two last conditions must then be asserted at the same time to increment the counter.

This proposed system has to face two major constraints. First, the design and layout of a multi-pixel structure with connections between them, which must be contained in a very small pixel size (between 40-60 μm side), is very difficult to achieve with our actual design technology (0.25 μm minimum gate length and 6 metal layers). This can be overcome by moving to newer commercial CMOS deep sub-micron technologies with smaller gate length and more interconnection metal layers. The second constraint is the design of very low noise amplifier and discriminator cells, in order to minimize the threshold spread distribution and mismatch between adjacent channels.

V. Conclusions

The *Medipix2* chip has been designed using a commercial deep-submicron technology building a pixel cell of 55 μm x 55 μm.

First measurements show an electronic pixel noise of 140 e^- rms and an unadjusted threshold variation around 360 e^- rms. A final design of a dedicated Medipix2 readout system is in its last production stages. Once this readout system is finished, more precise and complete measurements about threshold calibration and variation will be done in order to provide a full calibration of the chip.

VI. Acknowledgment

The authors would like to thank all members of the *Medipix Collaboration* for their support and encouragement.

VII. References

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