Introduction to SOI pixel sensor

27 Jan. 2006

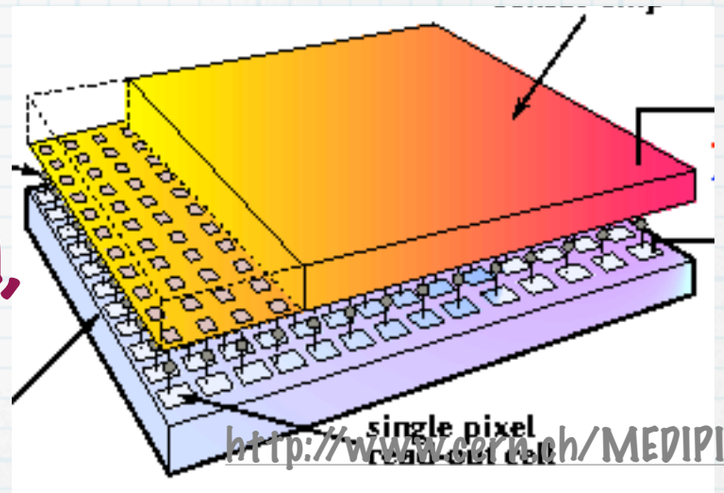
T. Tsuboyama (KEK)
for
KEK Detector R&D group
Pixel Subgroup

Collaboration

- **KEK** Y. Unno, S. Terada, Y. Ikegami, T. Tsuboyama, M. Hazumi, O. Tajima, Y. Ushiroda, **Y. Arai(＊Contact person)**
- **Niigata Univ.** : T. Kawasaki
- **Tsukuba Univ.** : K. Hara
- **Tokyo Institute of Technology** : H. Ishino
- **Hiroshima Univ.** : T. Ohsugi
- **JAXA** : H. Ikeda
- **Univ. of Hawaii** : Gary Varner, Marlon Barbero, James Kennedy, Larry Ruckman, Kirika Uchida, Catherine Yang, Elena Martin
- **Stanford Linear Accelerator Center** : Hiro Tajima
- **Reviwer:** Y. Sugimoto (**KEK**) and K. Hirose(**JAXA**)

Pixel sensors

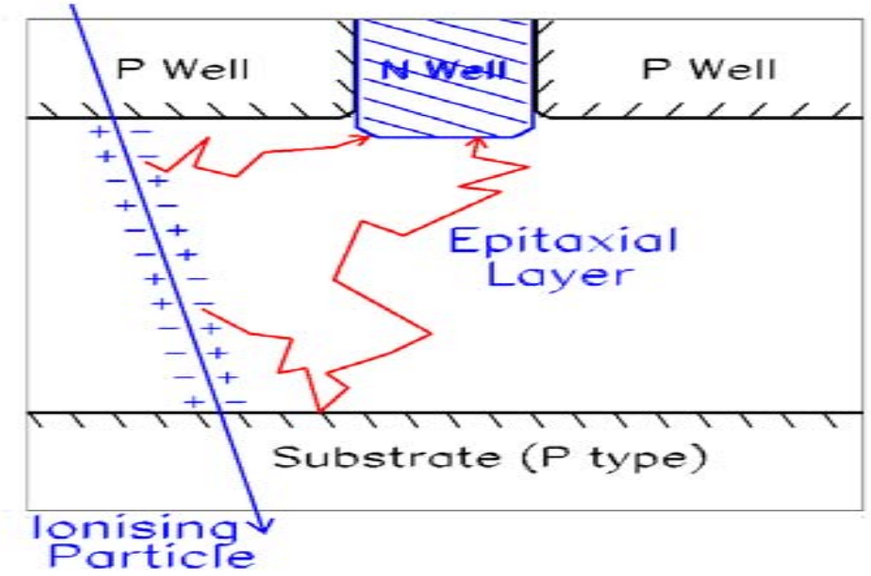
- Hybrid Pixel Sensors
  - Sensor part --> High resistivity silicon, signal is generated in depleted region.
  - Amplifier part --> Standard CMOS circuits, requires low resistivity silicon wafers.



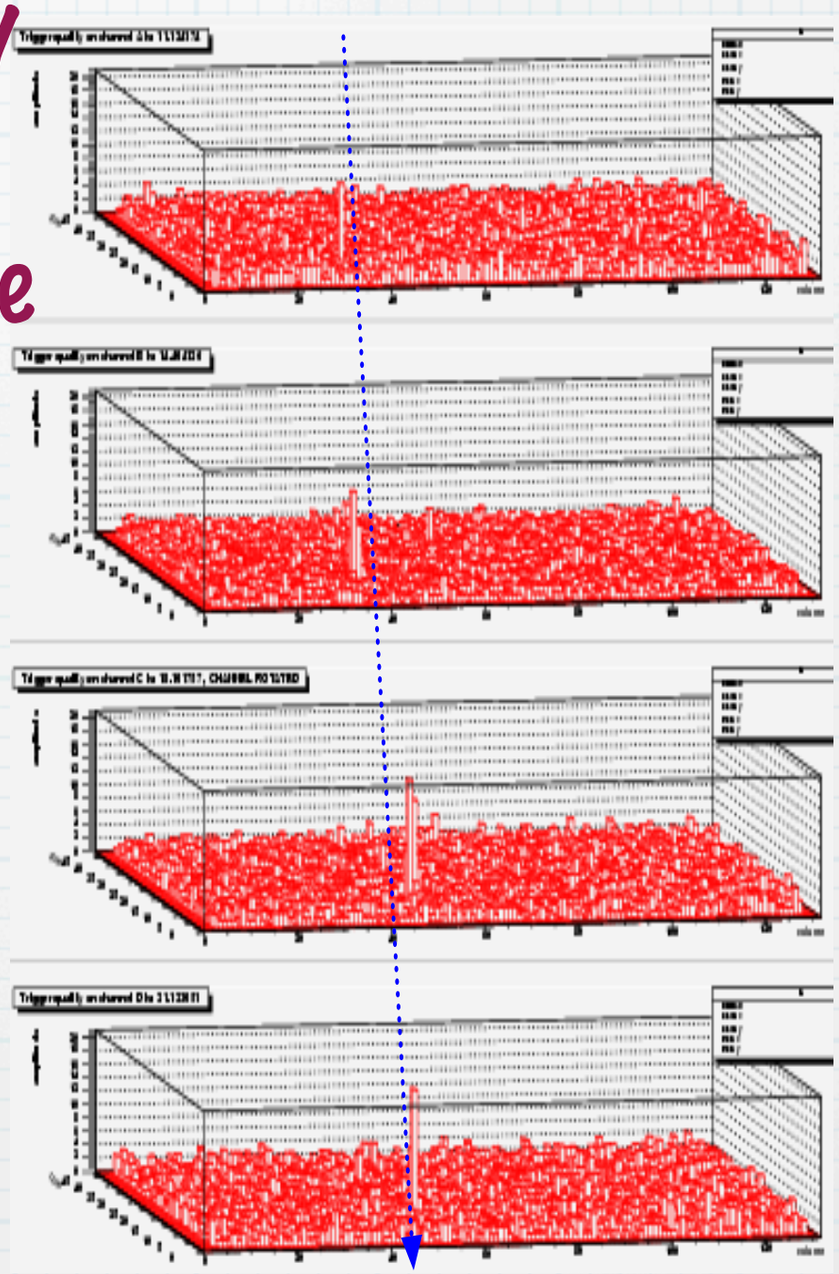
    - Bump bonding techniques
      - Low production yield
      - Large material thickness.
- Monolithic pixels are preferable.
  - Higher production yield
  - Lower material thickness after thinning

Predecessor (I)

* MAPS sensors (Europe, Hawaii)
  * Based on standard CMOS technology
  * Technology for the CMOS camera
  * Thin (<5um) epitaxial layer below the silicon surface is used as the sensor.
  * N-well is used for electrode and PMOS transistors can not be used.



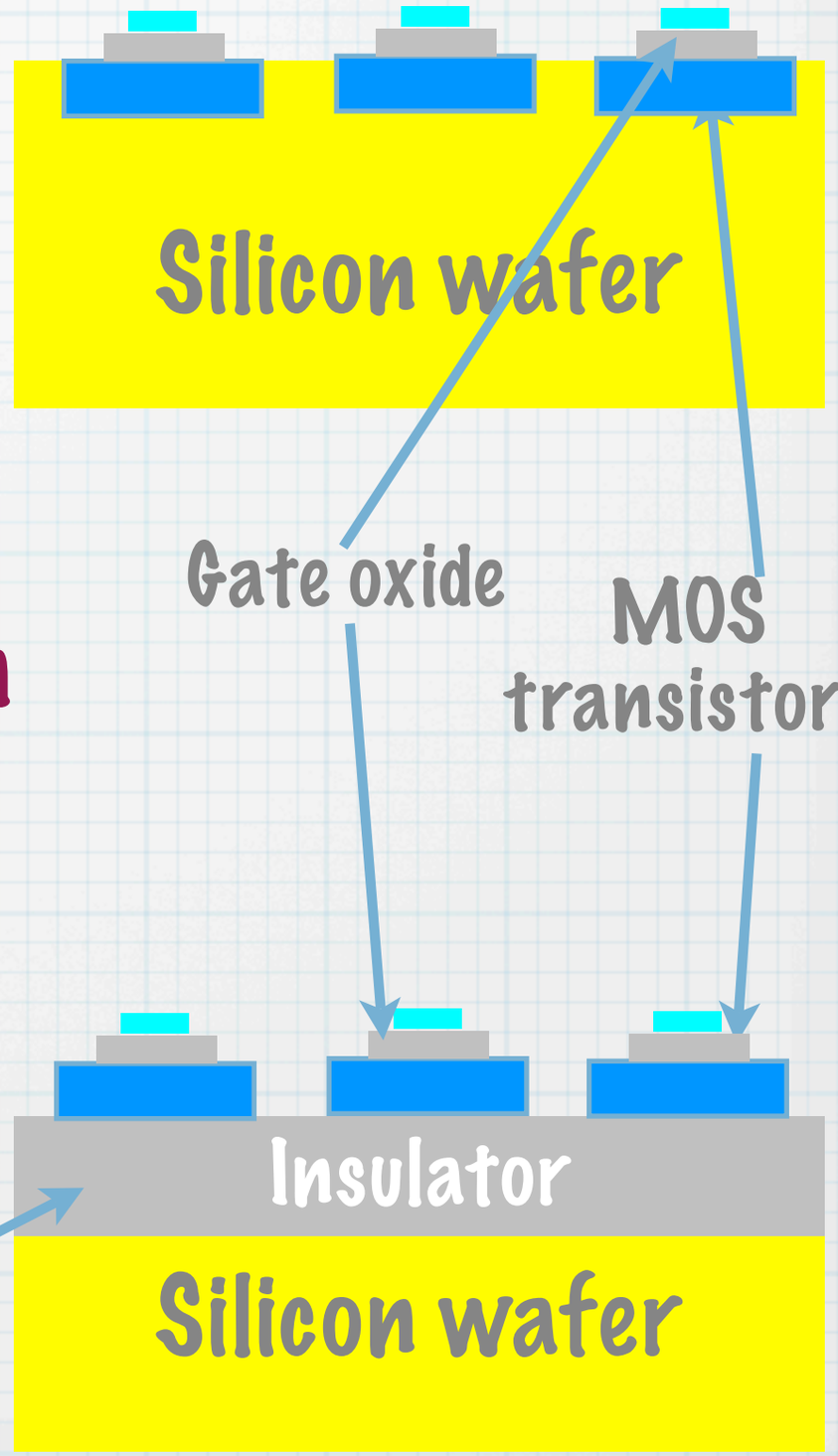
Test beam result



http://www.phys.hawaii.edu/~idlab/

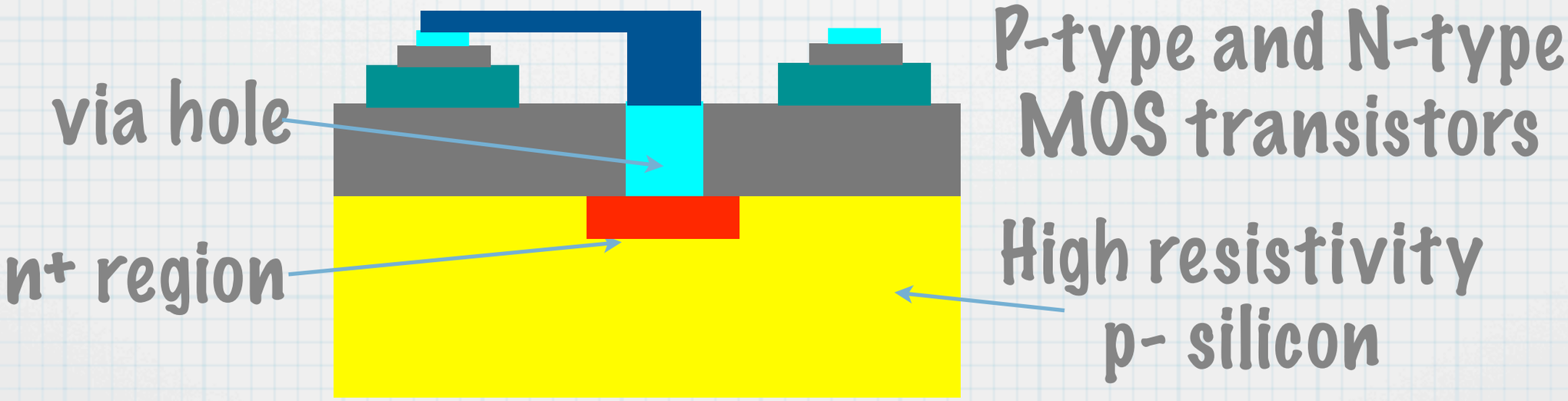
Sol CMOS technology

* Normal (bulk) CMOS IC
  * Components are made inside silicon wafer at 1-2 um from the surface.
* Sol (silicon on insulator) CMOS
  * Active parts are made top of thin SiO2 layer.
    * Transistors are isolated from each other and from the bulk silicon.
    * Smaller stray capacitance.



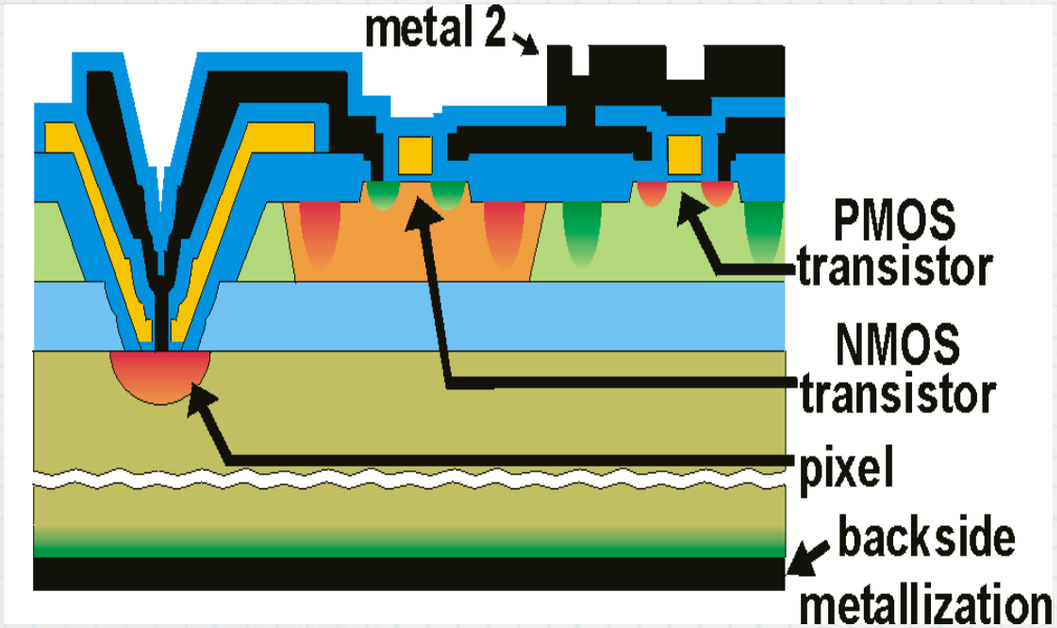
Sol pixel sensors

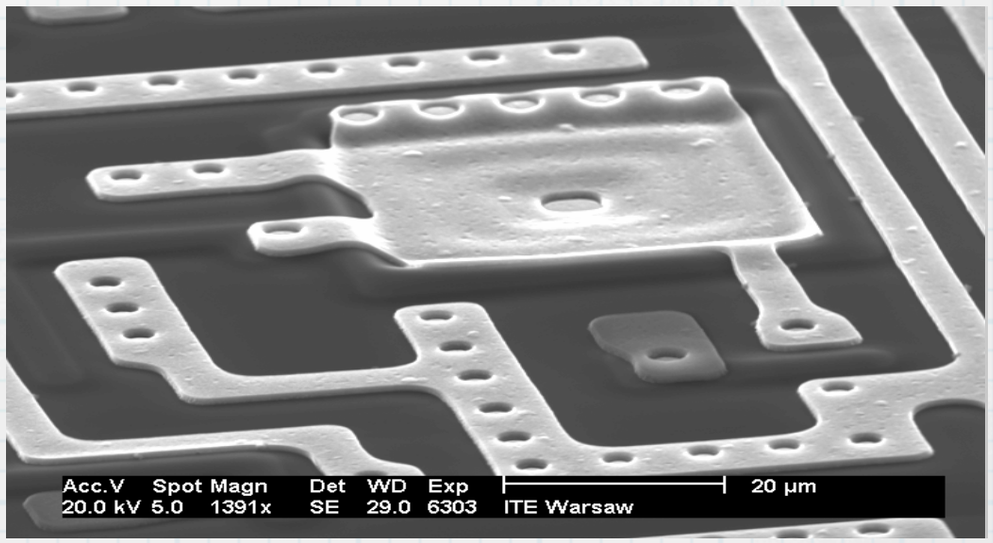
* Monolithic Pixel sensor can be designed using Sol technology
  * High resistivity support silicon can be used.
  * Signal is lead to the circuit through "via"s in the BOX.



Predecessors II

* Sol Pixel in Europe (Sucima)
  * Have succeeded to produce a prototype and observe signal from source particle.
  * Up to 2004, non-standard, 3-um technology is used.

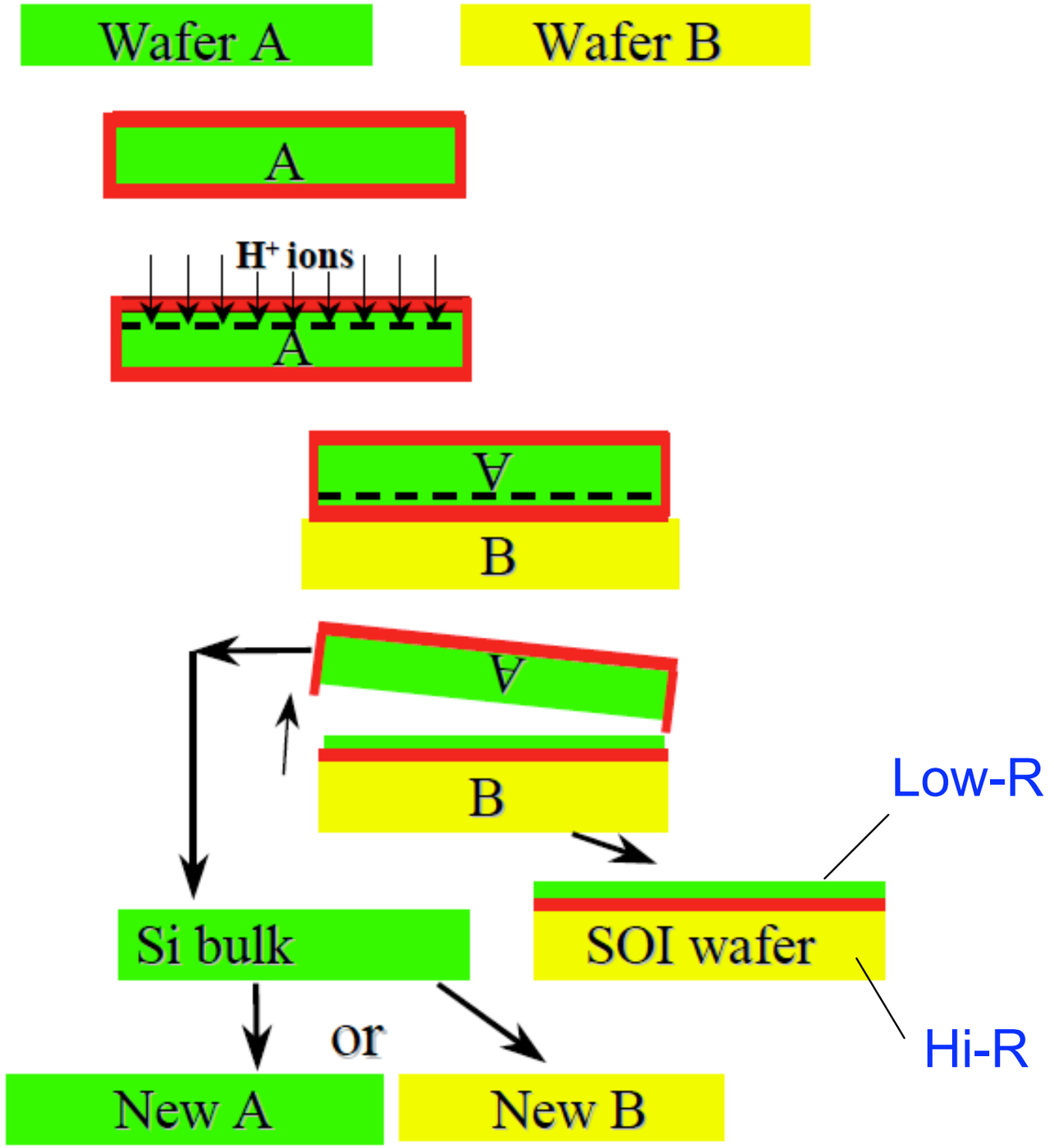




ref: http://sucima.dipscfm.uninsubria.it/wp2.php

SOIウエハーの作り方: Smart Cut (UNIBOND) by SOITEC

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



Purpose of R&D in KEK

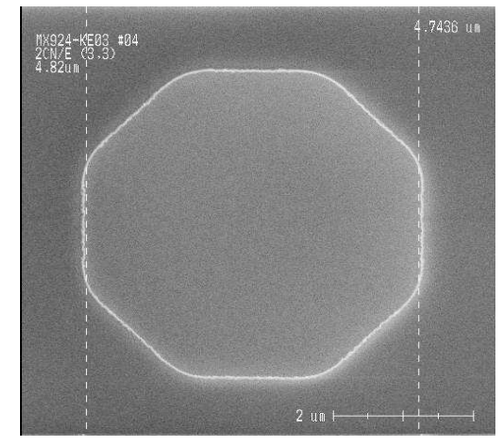
* To establish a monolithic pixel sensor in 2-3 years.
* Accumulate technologies applicable to Linear collider, Belle upgrade, LHC upgrade ...
* Investigate applications outside particle physics experiment (in future)

Key issues

* Adopt standard SoI-CMOS technology
  * State-of-art semiconductor technology is necessary.
  * OKI Semiconductor accepted our R&D
* Build up our knowledge and skills.

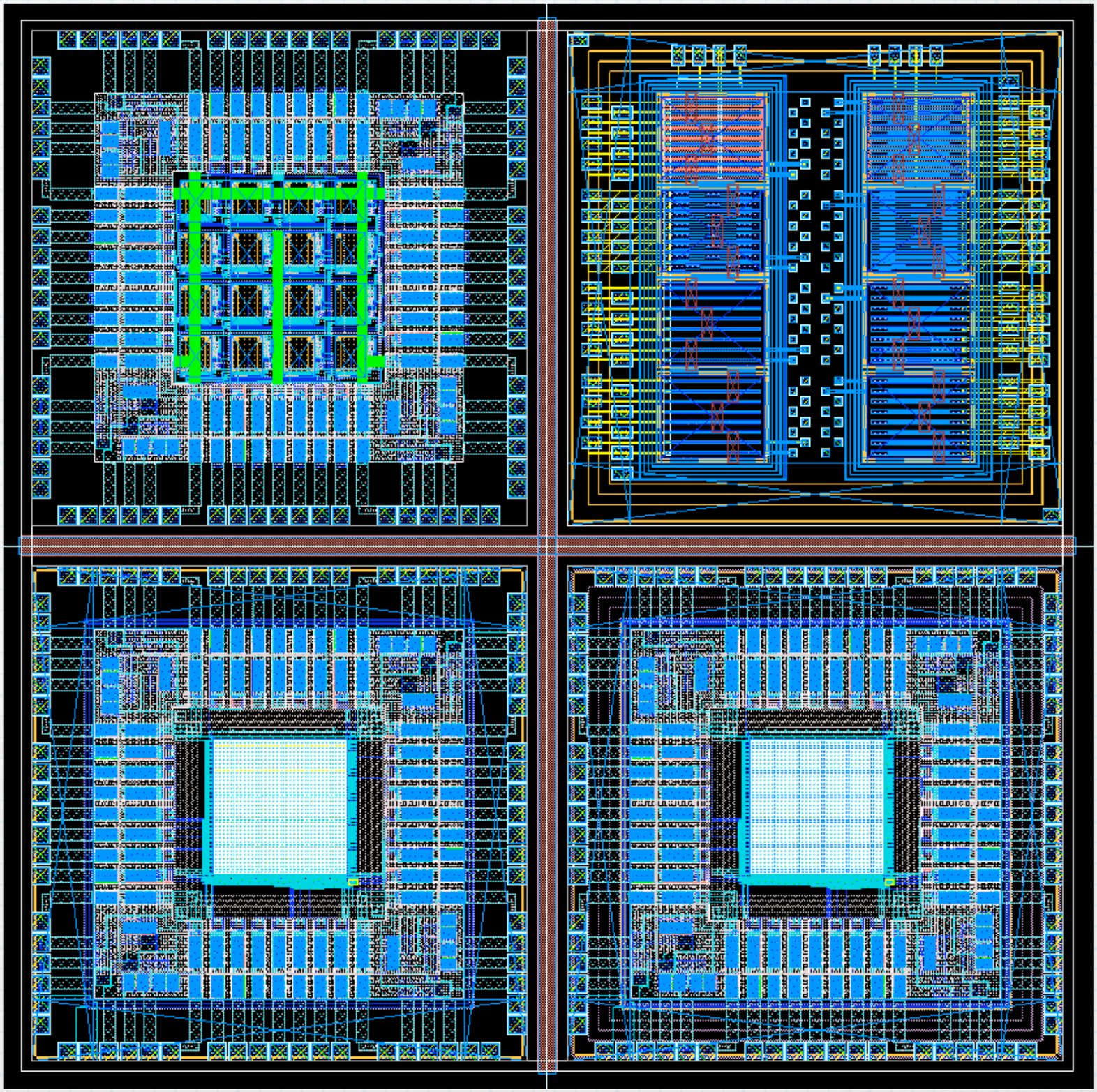
R&D 2005

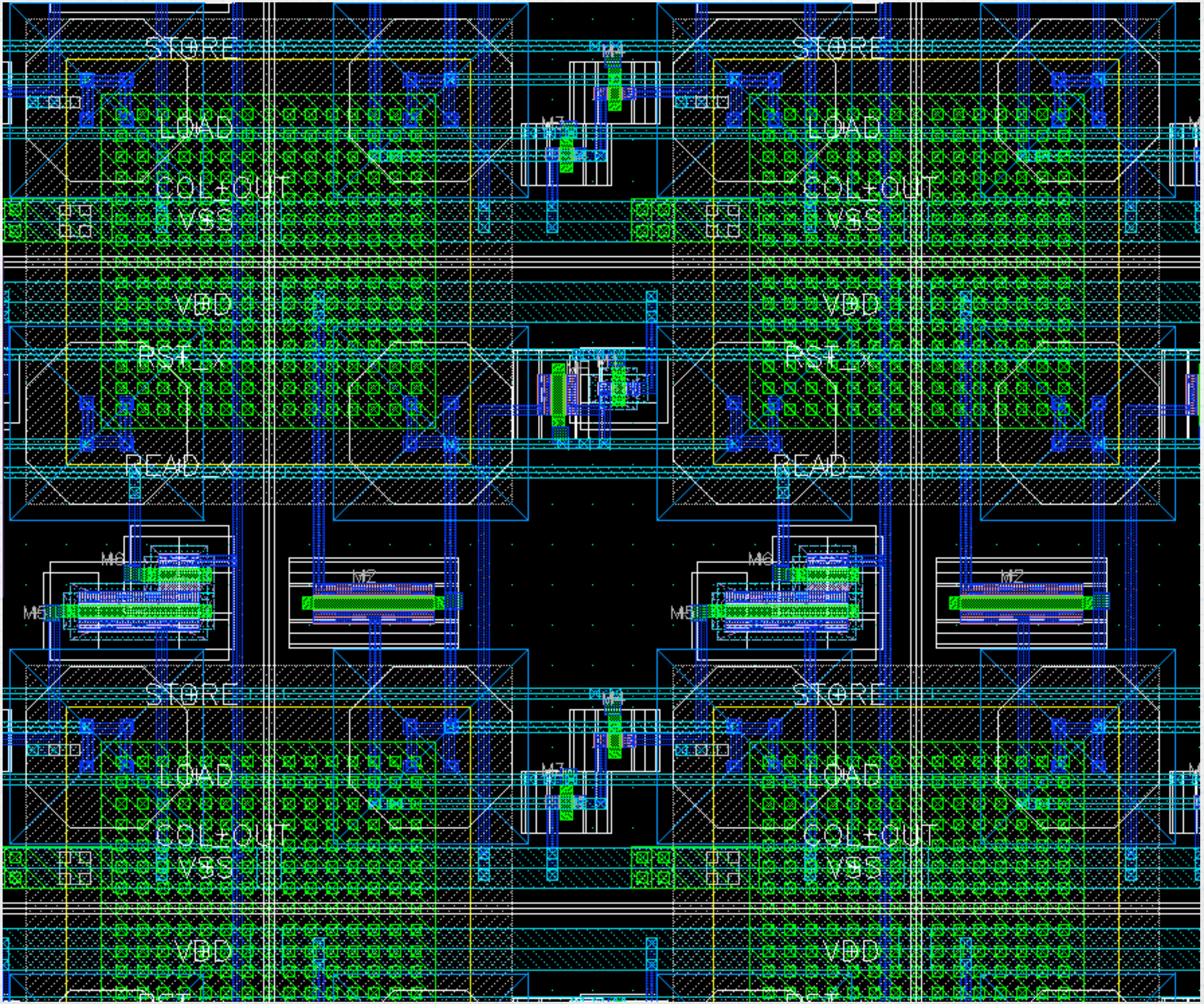
* June: Discussion with Oki started
* October: 9 designs (2.5mmx2.5mm) are submitted
  * Pixel sensor/circuit prototypes
  * Analog circuit prototypes: Preamp, Time-over-threshold, Comparator, Active Feedback etc. (VDEC)
    * 0.15um process: Vd=1.0V. Tight dynamic range for analog amp.
  * Prototype silicon sensor for a hard Xray Compton polarimeter.
  * Small strip sensor prototype p-type/n-type substrate which could be used for evaluation of TCAD outputs
* December 2005
  * The first test sample showed resistance between sensor-amplifier is small enough



Chip design

* 5 mm x 5mm area is divided into four.
*




STORE
LOAD
COL_OUT
VSS
VDD
RST_X
READ_X
M6
M2
M5
M1
M7
STORE
LOAD
COL_OUT
VSS
VDD
RST_X
READ_X
M6
M2
M5
STORE
LOAD
COL_OUT
VSS
VDD
STORE
LOAD
COL_OUT
VSS
VDD

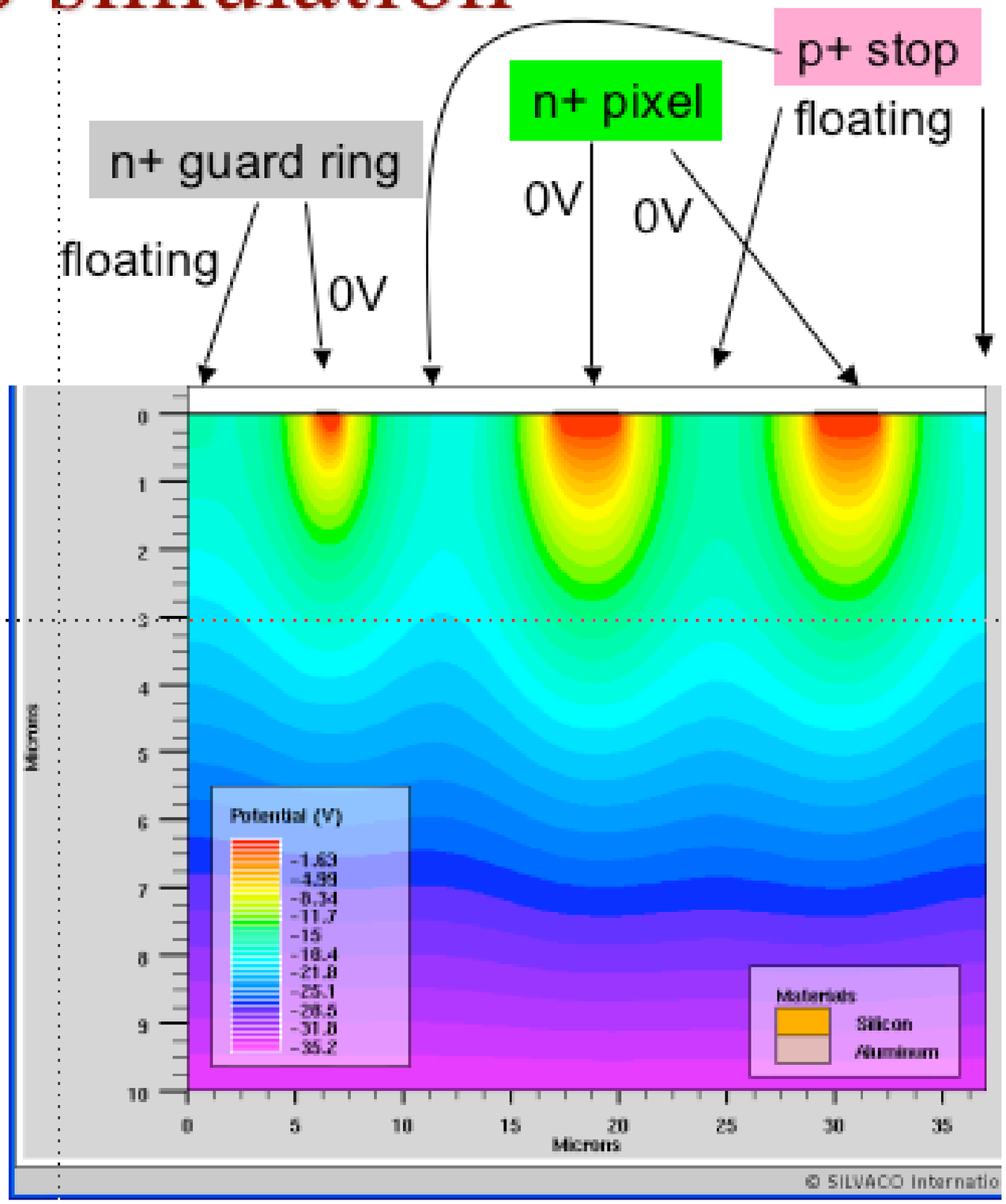
TCAD

* A generic name for
  * Process simulation + Semiconductor Simulation
* Produce a semiconductor virtually and estimate how it works.
  * Feed back to the design before the real silicon process.
    * After a design is submitted, real silicon process takes 4 moths.
    * Even a simple failure could ruin all the chip.

Example of device simulation

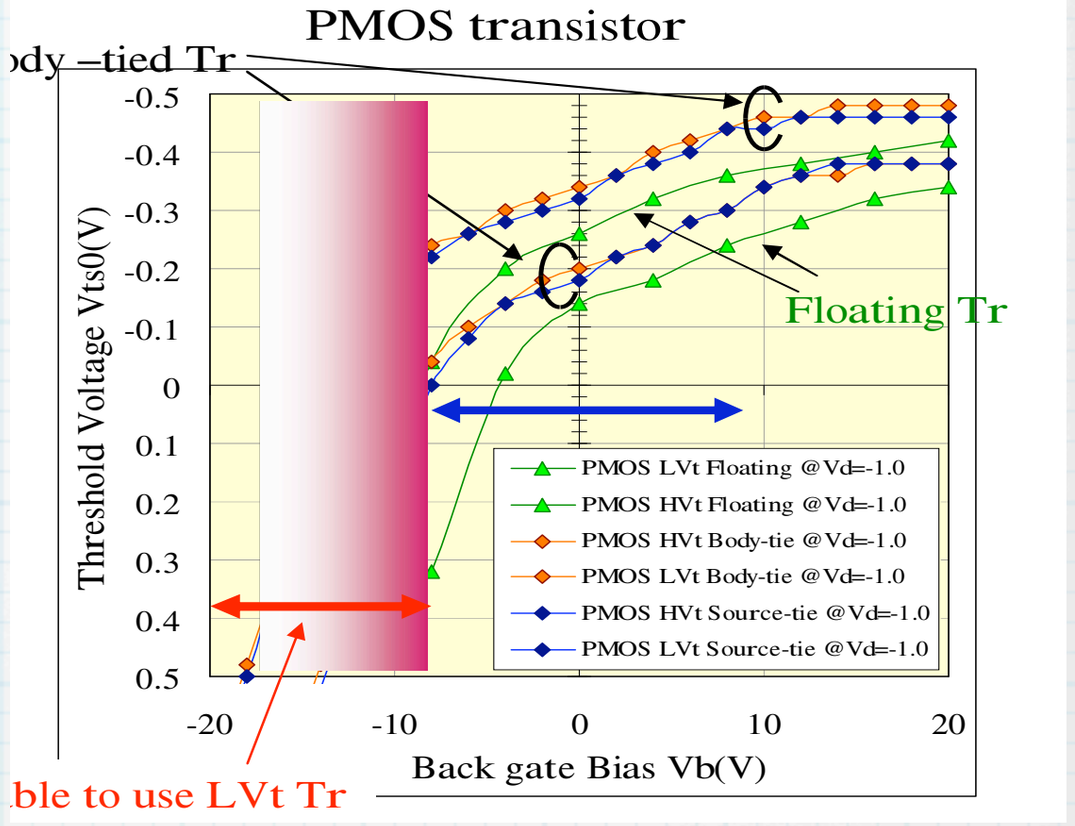
Simulation 1: Basic structure

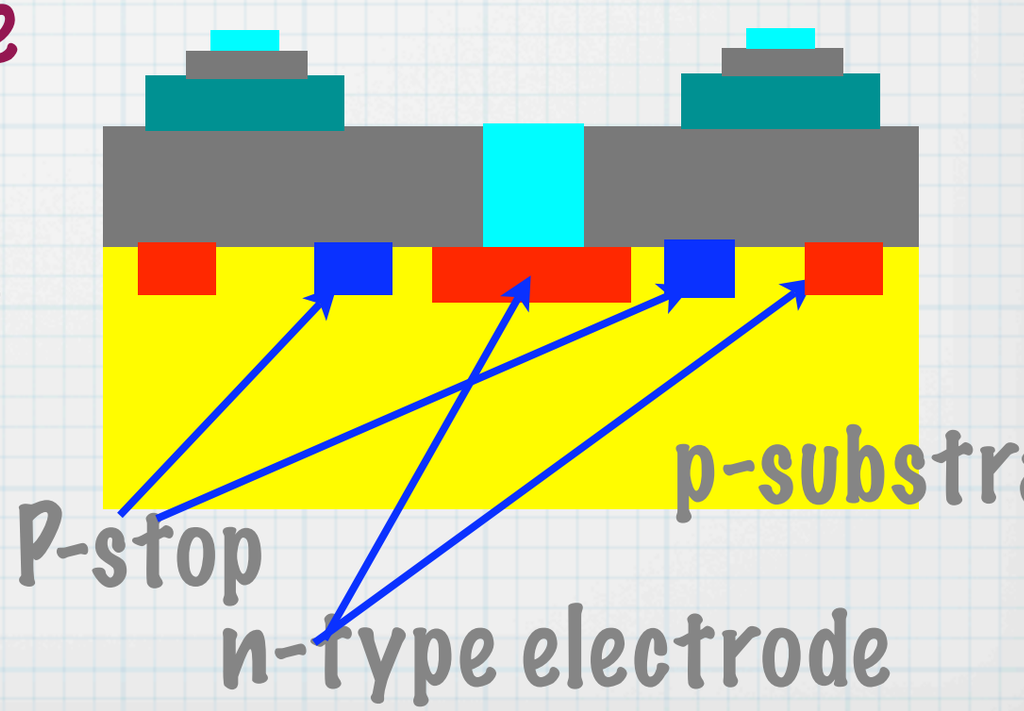
- "SOLVE" voltages, current etc. bias setting proper bias voltages
  - AC voltages possible
  - transient simulation also possible
  - sometimes time-consuming (another ~30min.)
  - sometimes fail to converge



Study items in 2005

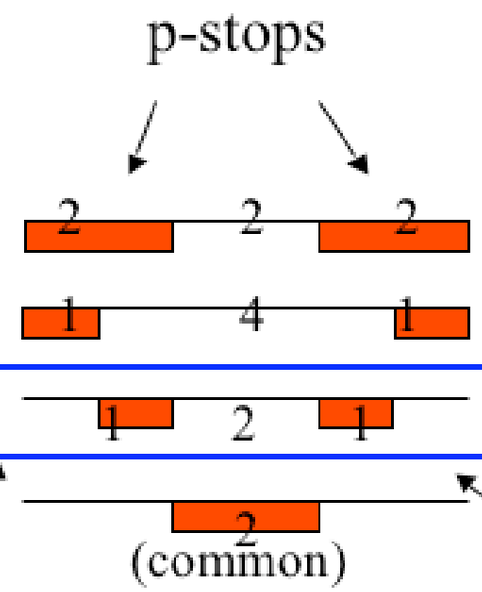
- Back-bias voltage problem
  - Potential in the sensor (back) part affects CMOS transistor above the BOX.
    - The thickness of BOX=200nm.
  - Potential should not exceed +-8V.
  - P-stop is floating and tends to be in high voltage.
- Break down voltage in silicon
  - Electric field <3x10^5V to avoid micro discharge in sensor part



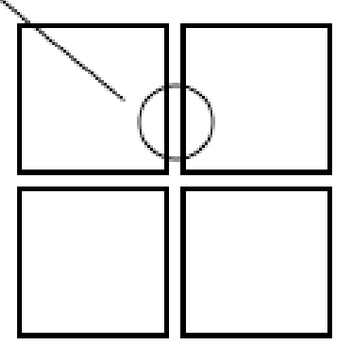


P-stop optimization

(1 small pixel in 1 cell)



V(p-stop) [V]	V(p-p) [V]	Max. Efield (10^5V/cm)
-23.5	-22	10
-20	-18.5	10
-14.5	-13	5
-11	-11	9



Vbias = -500V for 250um thick p-bulk

smaller |Vbias| sufficient for thinner detector

Best result

Cf. 1/1/1 must be even better

Next steps

- What we did not try in 2005
  - Doping in the back surface.
  - (n-type) Higher resistivity wafer in the sensor part
  - Resistivity control in the sensor part
    - Even type flip is expected due to "Thermal Donar generation" in the high temperature silicon processes.
  - Thinning down to <100um
  - Large area sensor, for example 5mmx5mm
- TCAD study
  - Simulate pixel sensor in 3-D and compare characteristics with the 2005 pixel prototype.
  - Simulate sensor part and CMOS transistor at once.

Summary

* We started up SoI pixel R&D project in 2005.
  * Intense evaluation will start in Spring.
* If successful, design with less restrictions would be tried.
  * Example: n-type higher resistivity wafer
* We welcome young people.
* Y. Arai will give a talk at JPS Matsuyama meeting.