Introduction to SoI pixel sensor

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for
KEK Detector R&D group
Pixel Subgroup

Collaboration

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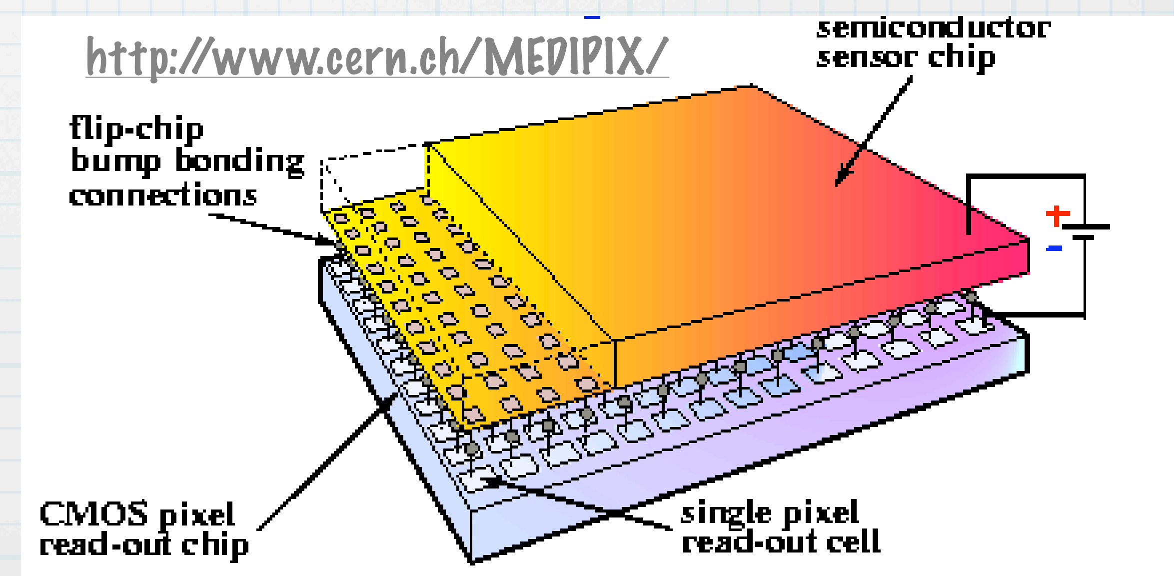
- Tsukuba Univ. ： K. Hara
- Tokyo Institute of Technology ： H. Ishino
- Hiroshima Univ. ： T. Ohsugi
- JAXA ： H. Ikeda
- Univ. of Hawaii : Gary Varner, Marlon Barbero, James Kennedy, Larry Ruckman, Kirika Uchida, Catherine Yang
- Stanford Linear Accelerator Center : Hiro Tajima
- **Reviwer**
- Y. Sugimoto (KEK) and K. Hirose(JAXA)

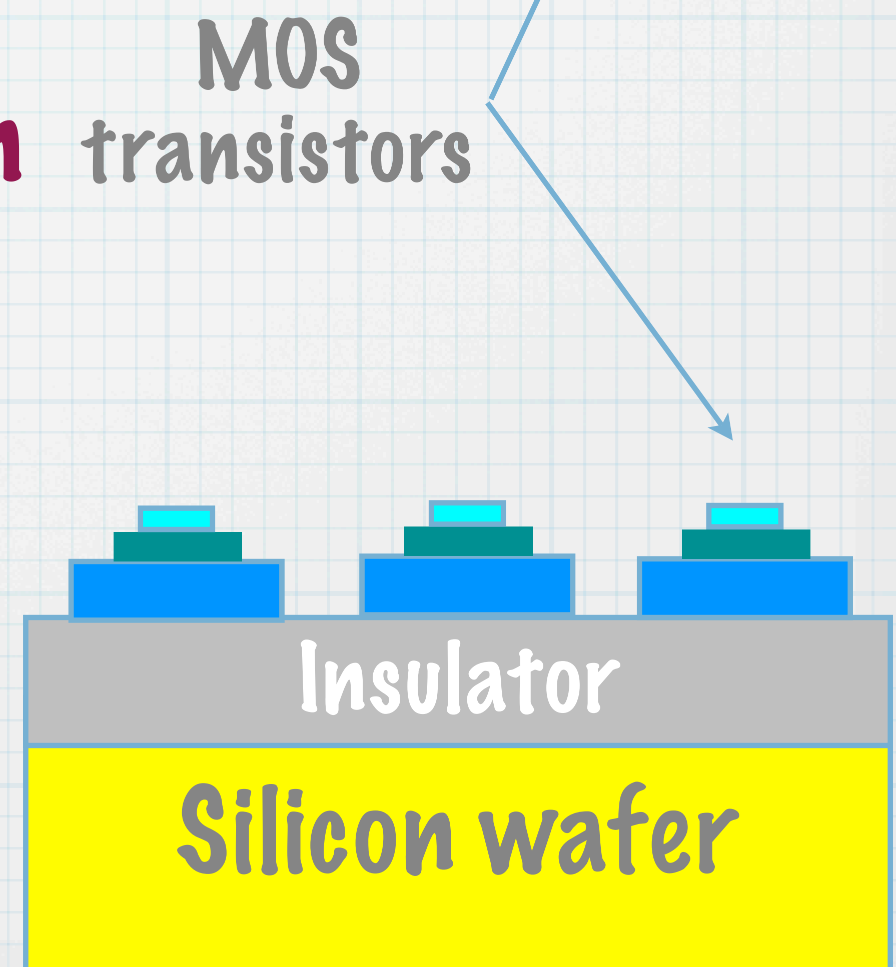
Pixel sensors

* Hybrid Pixel Sensors
  * Sensor part --> High resistivity silicon, signal comes from depleted region.
  * Amplifier part --> Production of standard CMOS circuits requires low resistivity silicon wafers.
  * Bump bonding techniques
    * Low production yield
    * Large material thickness.
* Monolithic pixels are preferable.
  * Higher production yield
  * Lower material thickness



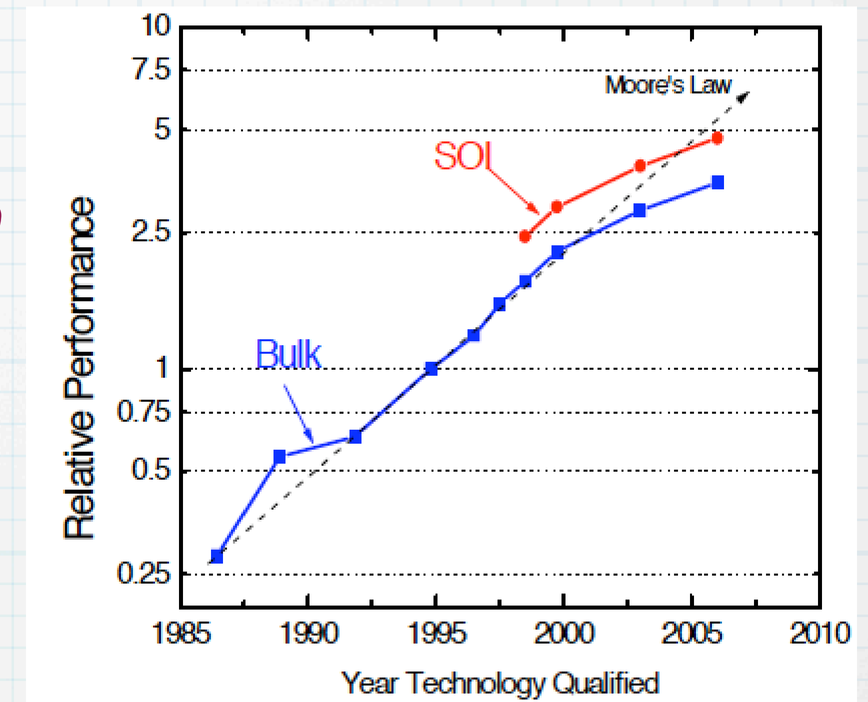
CMOS technology

* Normal (bulk) CMOS IC
  * Components are made inside silicon wafer at 1-2 um from the surface.
* SoI (silicon on insulator) CMOS
  * Active parts are made top of thin SiO2 layer.
    * Transistors are isolated from each other and from the bulk silicon.
    * Smaller stray capacitance.

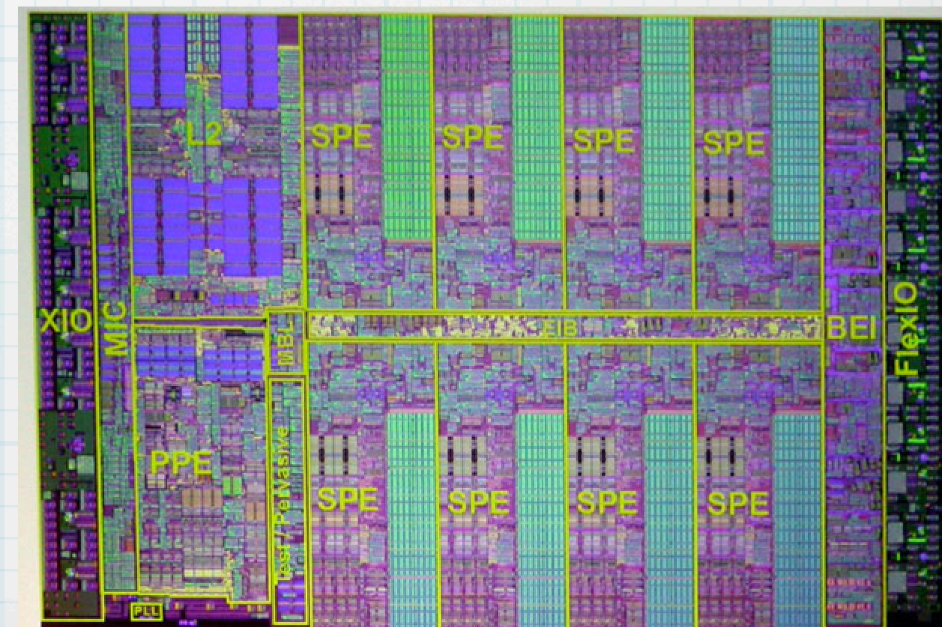


Advantage of SoI CMOS

* SoI (silicon on insulator) CMOS
  * Faster clock at the same power dissipation (IBM Power PC, Cell, AMD Opteron etc.)
  * Insensitive to charge induced in the support silicon
    * Latch-up free
    * Operated in intense radiation condition
* Operable at high temperature.
  * Even at 200-300 degreeC.
* Full depleted MOS transistors using thin Si layer

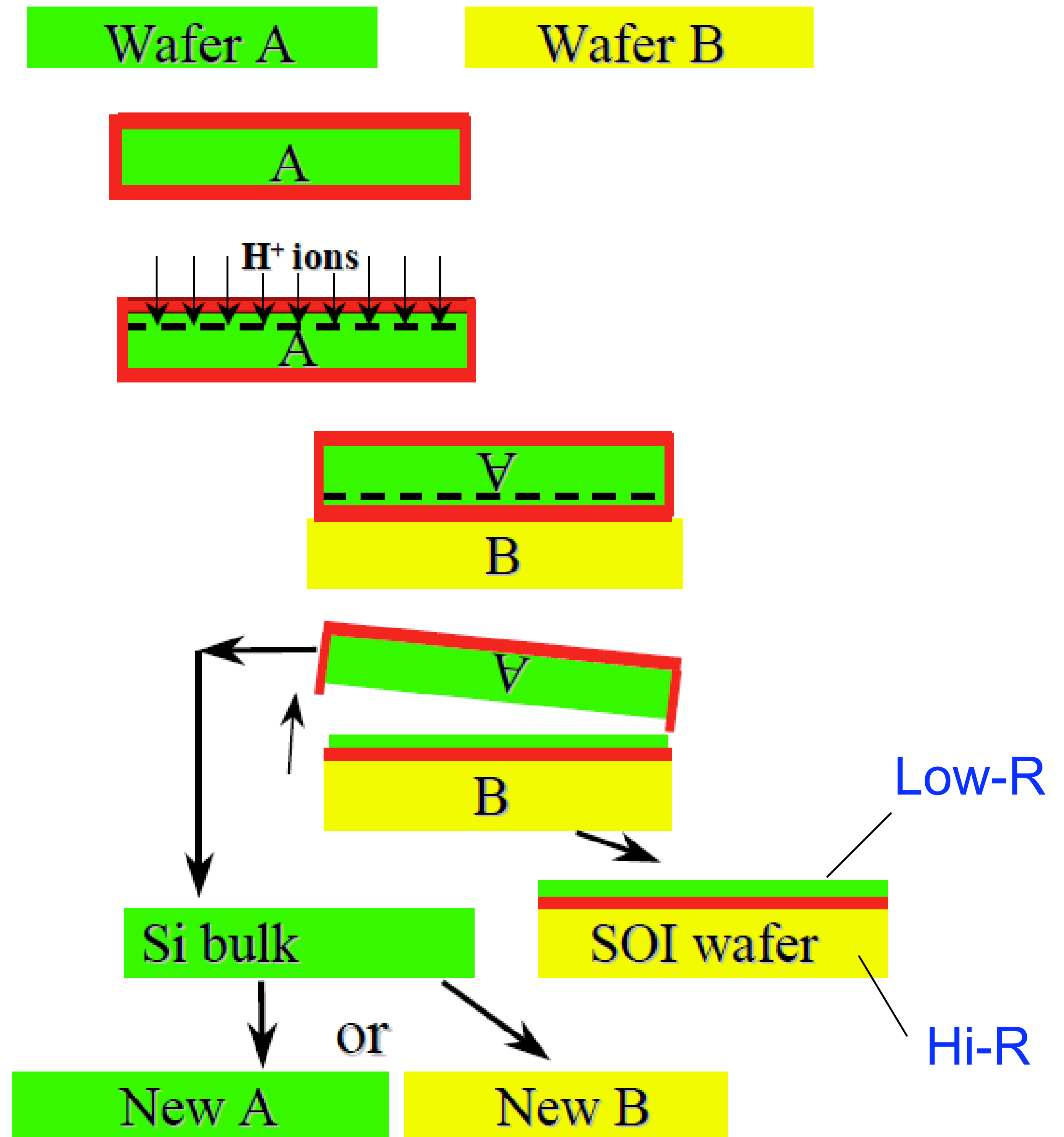


Cell chip (IBM 90nm SoI)



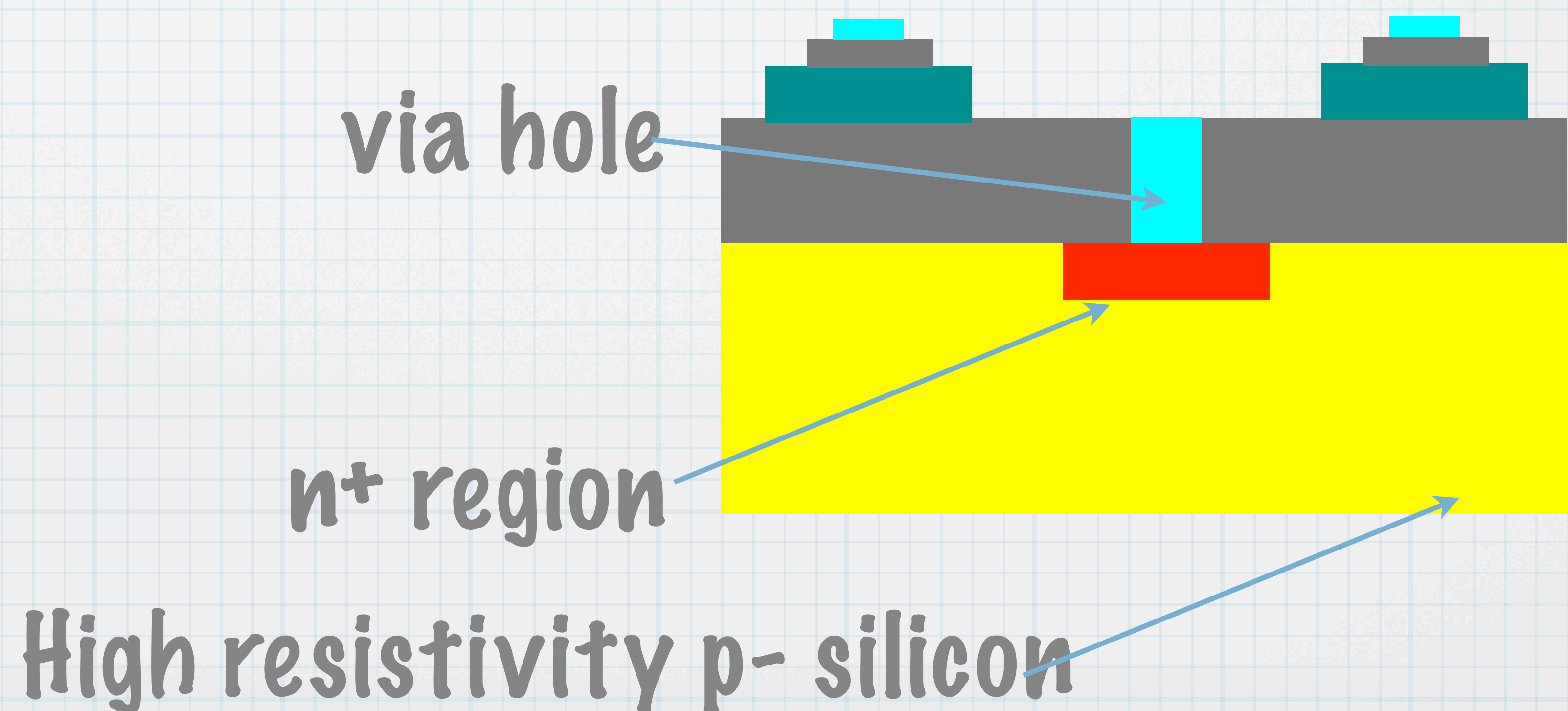
SOIウエハーの作り方: Smart Cut (UNIBOND) by SOITEC

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



Monolithic pixel sensors

* Monolithic Pixel sensor can be designed using SoI technology assuming
  * High resistivity support silicon can be used.
  * Good contacts are made between the surface MOS circuit and bulk sensor part.

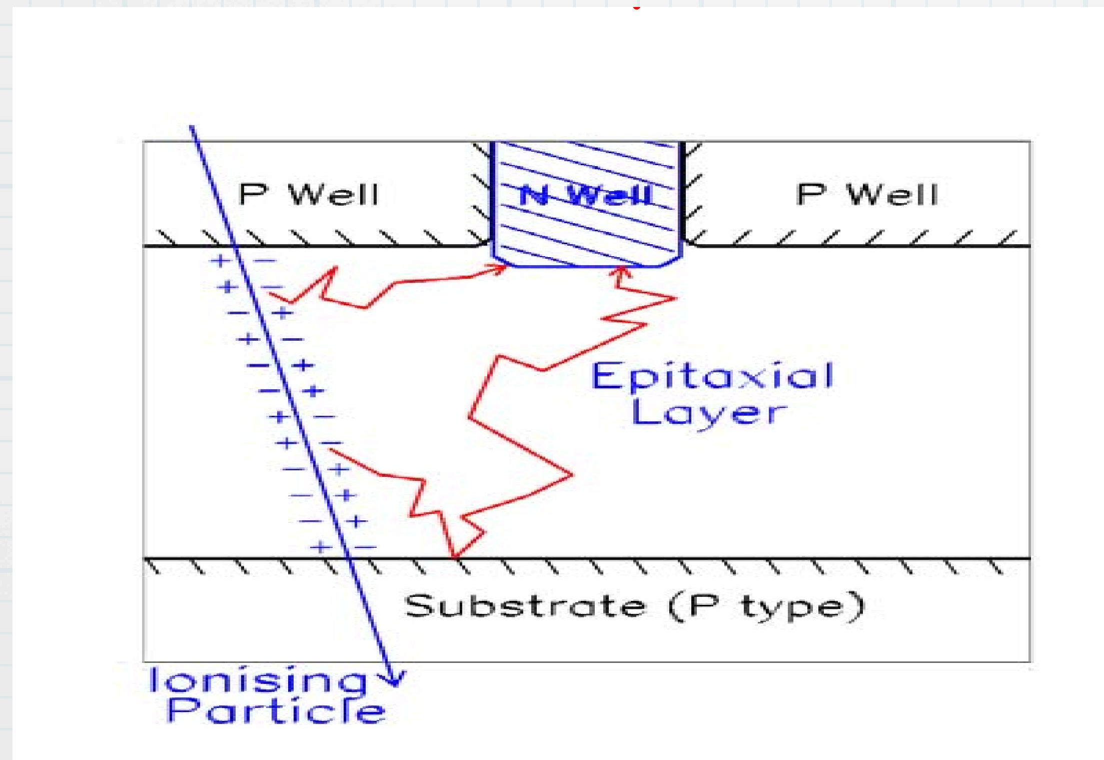


Numbers from catalog

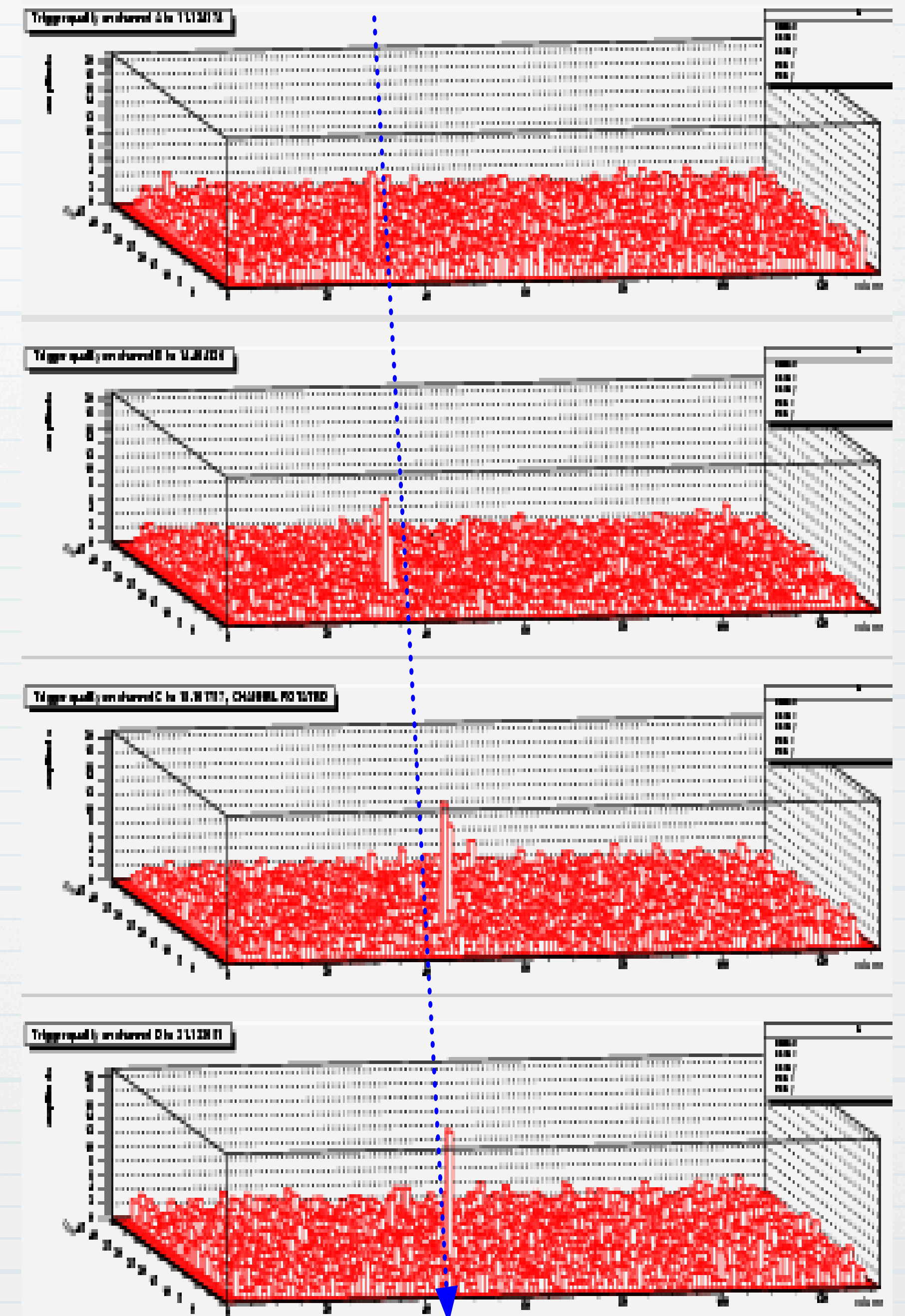
* Top silicon
  * Thickness: $70<t<500$nm
  * Resistivity: 8-22 Ohm-cm, p-type
* Buried oxide (BOX)
  * Thickness: $145<t<400$nm
  * Breakdown voltage: 9 MV/cm
* Handle (sensor) wafer
  * >1000 Ohm-cm (type not specified)
  * Thickness 500 um

Predecessors I

* MAPS sensors (Europe, Hawaii)
  * Technology for the CMOS camera
  * Thin (<5um) epitaxial layer below the silicon surface is used as the sensor.
  * N-well is used for electrode and PMOS tansistors can not be used.



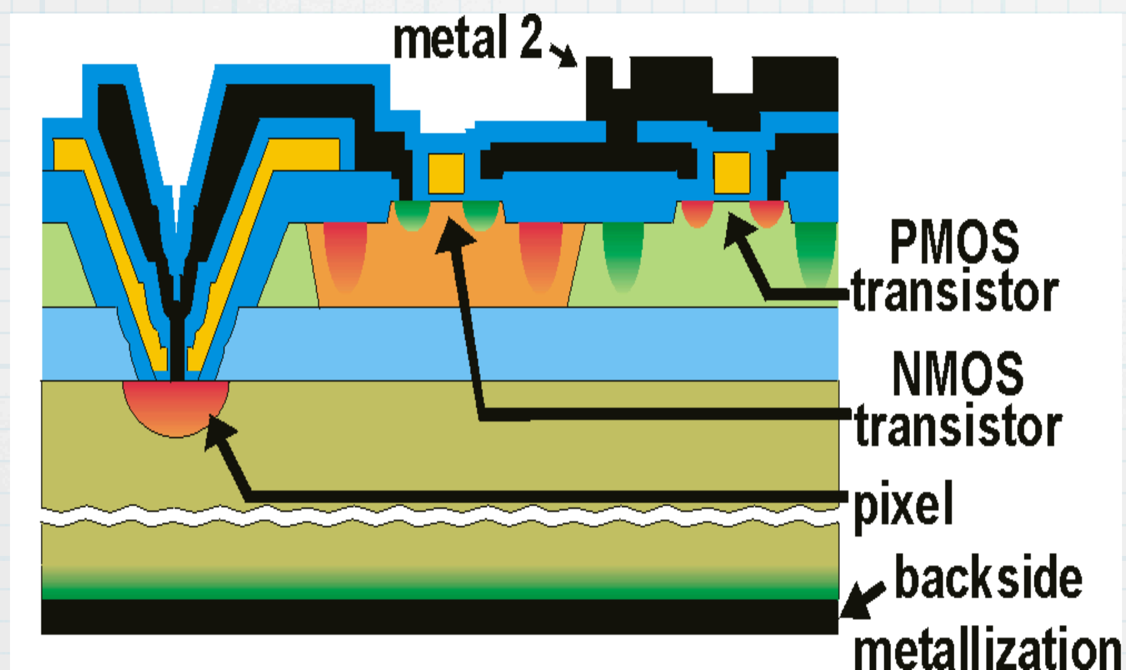
Test beam result

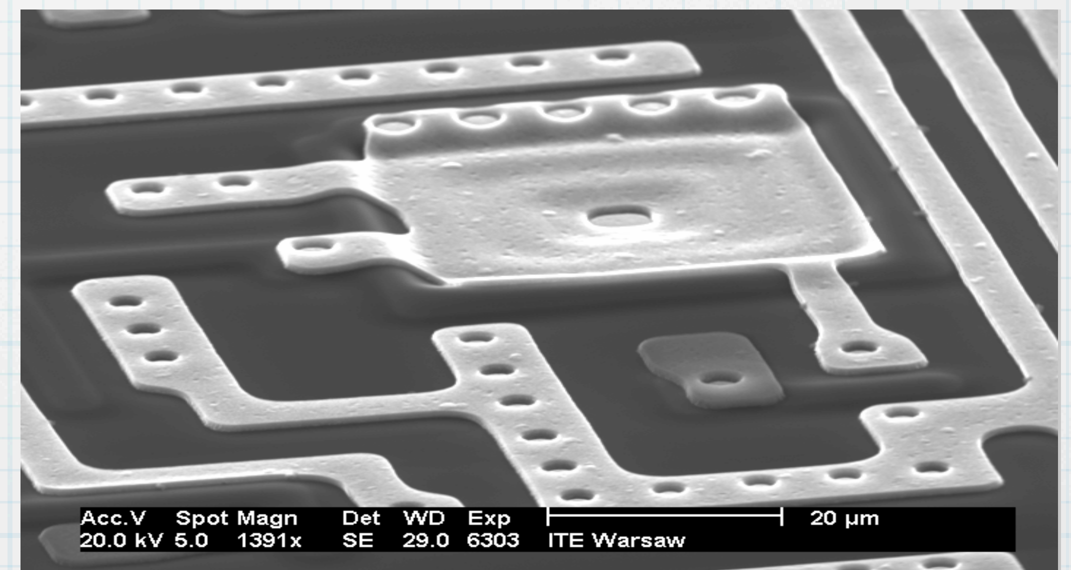


http://www.phys.hawaii.edu/~idlab/

Predecessors II

* Sol Pixel in Europe (Sucima)
  * Have succeeded to produce a prototype and observe signal from source particle.
  * Up to 2004, non-standard, 3-um technology is used.





ref: http://sucima.dipscfm.uninsubria.it/wp2.php

Purpose of R&D in KEK

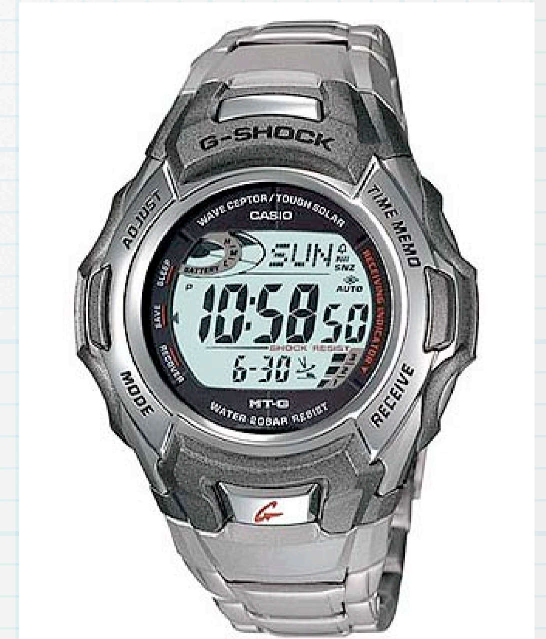
* To establish a Japan-made monolithic pixel sensor in 2-3 years.
* Accumulate technology applicable to Linear collider, Belle upgrade, LHC upgrade ...
* Investigate applications outside particle physics experiment (in future)

Key issues

* Adopt standard SoI-CMOS technology
  * State-of-art semiconductor technology is accessible.
* Build up our knowledge and skills.

Collaboration with Oki

* Oki first produced commercial Sol CMOS
* Similar production is possible in VDEC.

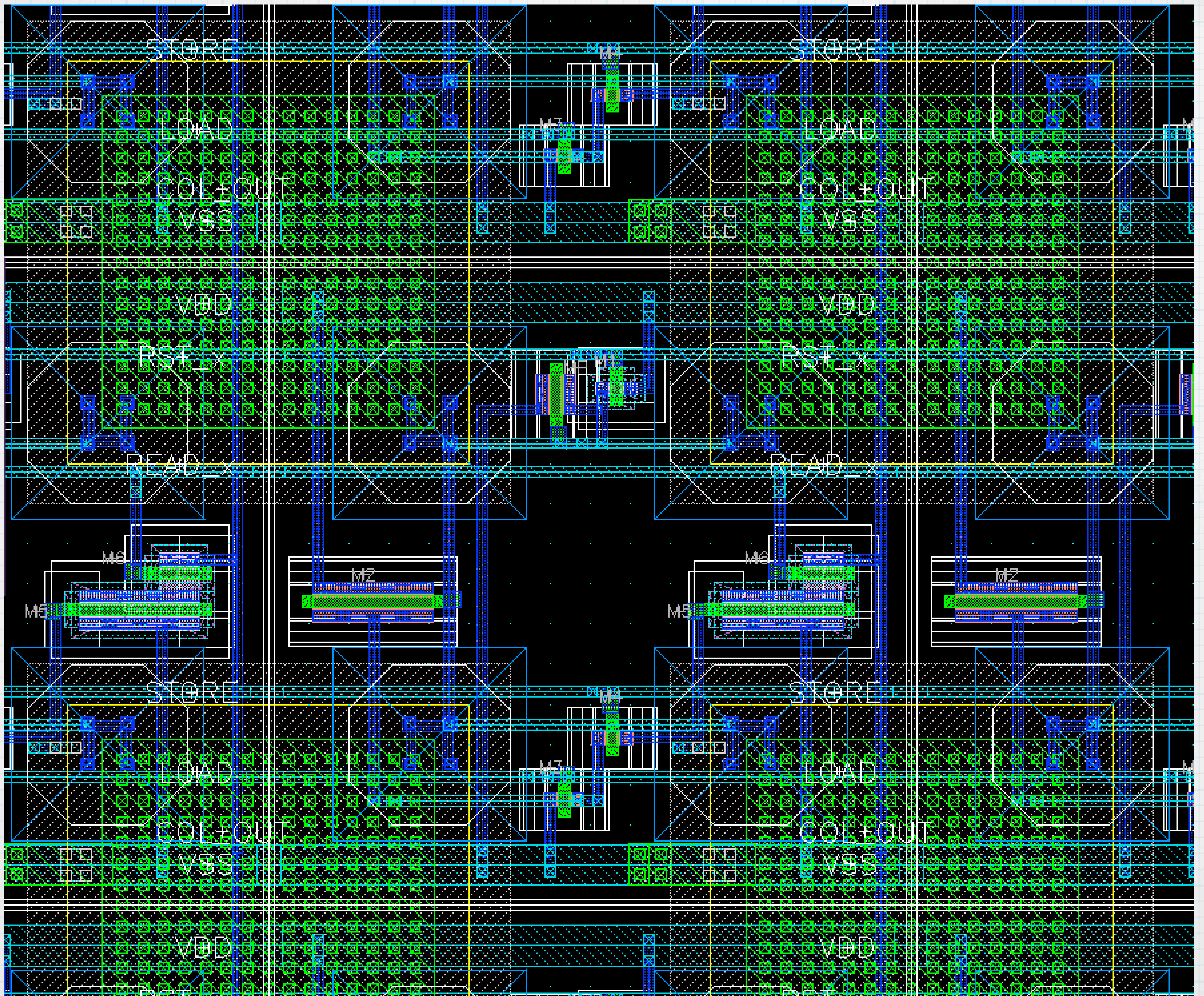


VDEC (VLSI design & Education)

R&D 2005

* April: Starting discussion with Oki
* October: 9 designs (2.5mmx2.5mm) are submitted
  * Pixel sensor/circuit prototypes
  * Analog circuit prototypes:Preamp, Time-over-threshold, Comparator, Active Feedback etc.
  * Prototype for "hard Xray compton polarimeter"
  * Small strip sensor prototype p-type/n-type substrate
  * which could be used for evaluation of TCAD outputs (next next page).
* The products will be delivered in March 2006
* Then evaluation will start immediately

Name	Contents
VDECTEG1	Preamp, TOT, Comparator, Active Feedback
RADTEG1p/n	Pixel, Transistors, Ring oscillators
PixTEG1p/n	32x32 Pixel array
StripTEG1p/n	Short strip (TCAD verification)
HawaiiTEG1p/n	Imaging Hard X-ray Polarimeter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Restrictions

* Substrate: p-type 1kOhm-meter.
  * The highest one for the standard wafer.
  * Vb=800 V is necessary to deplete 250 um thickness.
  * High potential in the sensor part would affect the circuit part.
* Type flip from p-type to n-type could occur in the semiconductor process.
  * Need two designs for pixel and strip prototypes.
* Dope in the backside is not possible.
  * Afraid of pollution of the production line.
  * Metalization will be done instead.
* Depending on the result of first prototype, we

TCAD

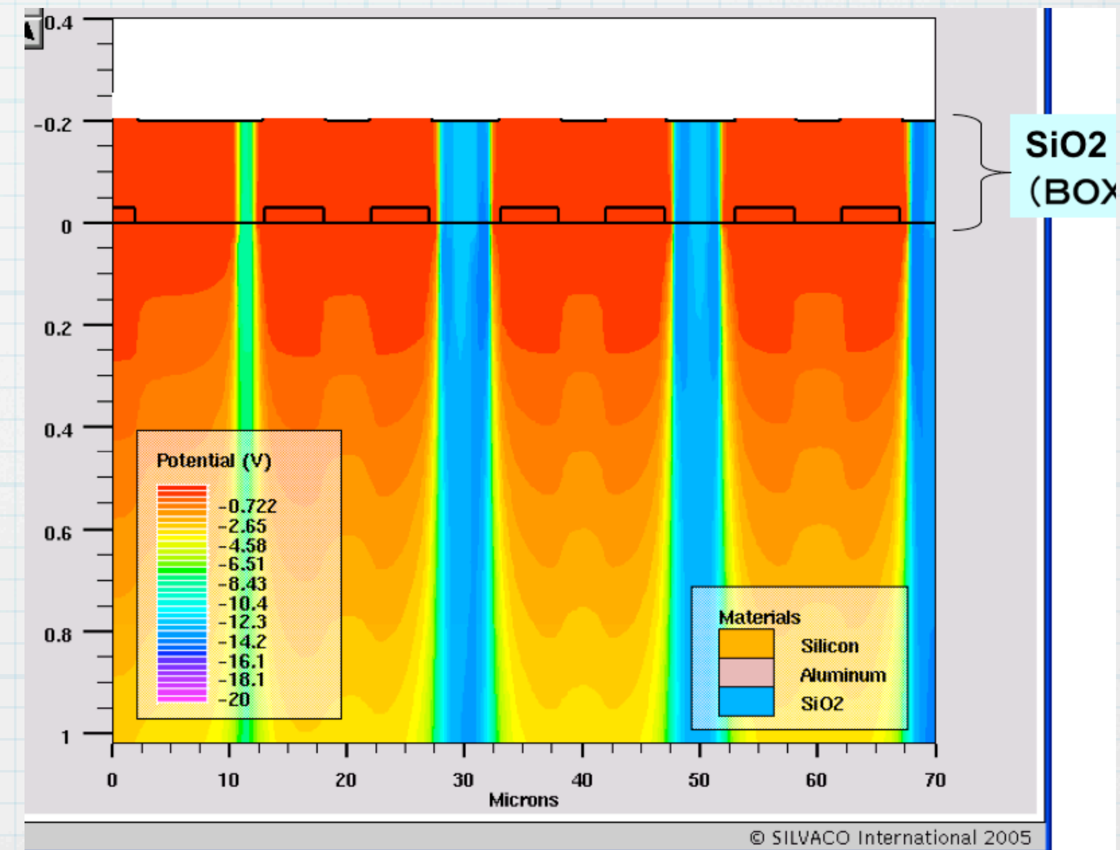
* A generic name for
  * Process simulation + Semiconductor Simulation
* Once a design is submitted, it takes 4 moths Silicon process simulation
* Even a simple failure could ruin all the chip.
  * Estimate the properties of a design helps.
* In our case, we are interested in
  * Effects of "sensor part" to CMOS transistors
  * Potential distribution in the sensor part.

TCAD

* Tools
* Silvaco --- ATHENA (Process). ATLAS(Device)
* 2-dimensional simulation
* Widely used
* ENEXSS --- Japan made
  * 3-dimensional simulation is possible

Back bias problem

* A study item in 2005
* Effect of potential in the support (sensor) part to the CMOS transistor above the BOX.
* Configuration of p/n implants was studied to minimize the effect.



Next steps

* What we did not try in 2005
  * Large area 2.5mmx2.5mm for example,
  * Thinning down to <100um
  * Doping in the back surface
  * Higher resistivity in the support wafer (sensor)
  * Resistivity control in the semiconductor process
  * High resistivity wafers (>4kOhm-cm)
* TCAD study
  * Simulate pixel sensor in 3-D and compare characteristics with the 2005 prototype.
  * Simulate sensor part and CMOS transistor at once.

Summary

* We started up SoI pixel sensor project in 2005.
  * Oki Semiconductor is working with us.
  * First samples will be delivered in March.
* If successful, design with less restrictions will be done.
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