VME register map

19-Feb-2001

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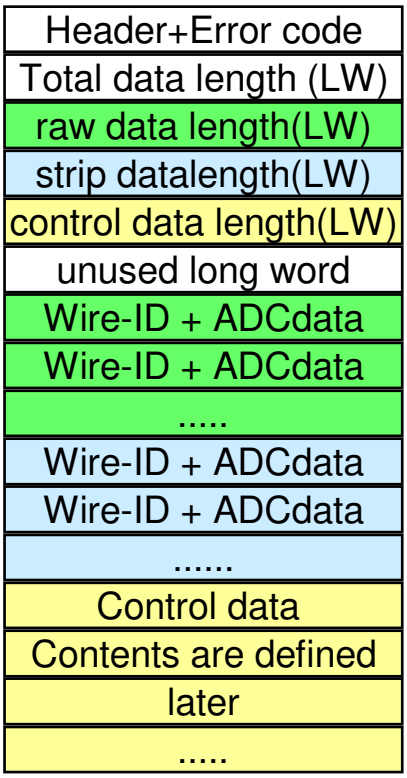
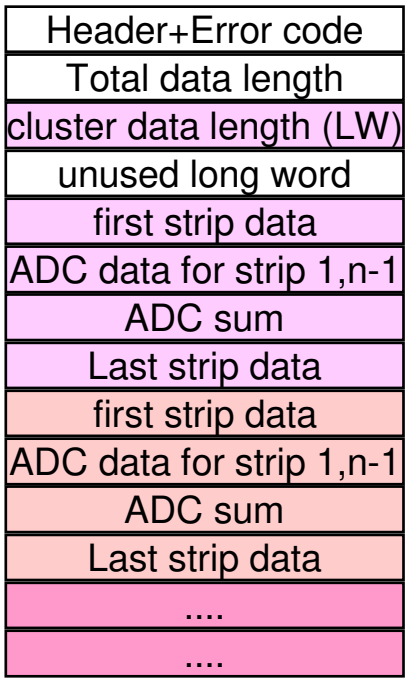
Update

18-oct-2001 Control register bit0-1

20-aug-2003 Bug fix for Readout Type

Data format (output from ADC module)





N.B.

- Wire ID+ADC data : As defined in DDL
- Header format will be determined later.
  (temporal assignment:
  bit 0-7 FLTN
  bit 8-15 BCN
  bit 16-31: Error information; defined later)
- Raw data are sent only for special triggers
  (but the header always exists).
- Three zero suppression modes for strip data
  1. No zero suppression (debugging)
  2. strip level zero suppression
  3. cluster level zero suppression

SLT Data buffer(R/W) test

(example for MM=A1) : A180 0000- A09F FFFF

Address

m	m	m	m	m	m	m	m	1	0	0	x	b	b	b	b	b	b	b	b	b	b	b	b	b	b	0	0

m..mm: 8bit ADC module number (DIP SW)
bbb…bbb: 1MB Data buffer
x this address bit is ignored:

EVB Data buffer(R/W) test

: A1A0 0000- A1DF FFFF

Address

m	m	m	m	m	m	m	m	1	0	1	x	b	b	b	b	b	b	b	b	b	b	b	b	b	b	0	0

m..mm: 8bit ADC module number (DIP SW)
bbb…bbb: 1MB Data buffer
x this address bit is ignored:

Pedestal table (R/W) AF41 XXXX

Address

m	m	m	m	1	1	1	1	0	1	0	0	m	m	m	m	u	u	u	h	h	h	h	s	s	s	s	s	s	0	0

m..mm: 8bit ADC module number (DIP SW)
uuu : 3bit ADC unit number
hhhh : 4bit HELIX number
sssssss : 7bit strip number

Data

0	0	0	0	0	0	0	0	d	d	d	d	d	d	p	p	p	p	p	p	p	p	p	p	p	p	t	t	t	t	t	t	t	t

dddddd : 6bit test ADC data
pppppppppp : 10bit pedestal data
tttttttt : 8bit threshold data

Token connection table (R/W) AF51?0??

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	u	u	u	0	0	0	0	0	0	0	s	s	s	s	0	0

m..mm: 8bit ADC module number (DIP SW)
uuu : 3bit ADC unit number
ssss : 4bit HELIX order

Data

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	h	h	h	h

hhhh : 4bit HELIX ID
(1111 if no helix chips)

Cluster threshold (R/W) AF51 ?040

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	u	u	u	0	0	0	0	0	0	1	0	0	0	0	0	0

Data

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t

tt…tt 16bit threshold for cluster ADCsum

Trailer Thrshold (R/W) AF51 ?044

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	u	u	u	0	0	0	0	0	0	1	0	0	0	1	0	0

m..mm: 8bit ADC module number (DIP SW)

Data

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	T	T	T	T	T	T	T	T	T	T

TTTTTTTTTT: threshold for H/L transition
in trailer bit encoding.
(recommended value 40h)

Clock Timing (R/W) AF51 ?080

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	u	u	u	0	0	0	0	0	1	0	0	0	0	0	0	0

m..mm: 8bit ADC module number (DIP SW)

Write DATA

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	u	p	d	d	d	d	x	x	x	x	x	x	x	x

dddd: clock delay (~4ns Step)
p: clock polarity (i.e. 48nS shift)
u: undefined

Read DATA

1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	u	p	d	d	d	d	0	0	0	v	t	t	t	t

tttt : TDC value. v: 1 if TDC data is valid

Strip Header for each token ring. (R/W) AF51 1000-003F

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m

0	0	0	1	0	0	0	0	0	0	u	u	u	h	0	0

m..mm: 8bit ADC module number (DIP SW)
uuu : 3bit ADC unit number
h : MSB of helix number

Data

i	i	i	i	i	i	i	i	i	i	i	i	x	x	x	x

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

iiiiiiiiiii :Strip ID (12 MSBs)
LSBs are labeled automatically

Command register (Write only) AF51 1100

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0

Data

Bit24:Interrupt disable
Bit25:Interrupt enable
Bit26:Dummy Accept with Abort
Bit27:Dummy Accept for test data
Bit28: Internal FLTN counter reset
Bit29: Error reset
Bit30: Init
Bit31: Init All ADCMs (Init singal on bus)

Control register I (R/W) AF511104

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0

Data

NEW!

Bit00-01: 00 : FLTn is fetched with fixed timing.
01: FLTn is fetched with C&C address bit
10 or 11 : FLTn is fetched with fixed timing and with the correct C&C address bit.
Bit02: Error/Reset request enable
Bit03: Digital Test data enable
(if 0, Digital test data is used f or Test pulse) common to 8 ADCUs
Bit04: Online
Bit05: Not Use dummy 4bit ROT
Bit06: Not Use local FLTn/ 6bit ROT
Bit07: Trigger selection
(0: VME command, 1: C&C)
Bit08: Enable for ADCU0
Bit09: Enable for ADCU1
Bit10: Enable for ADCU2
Bit11: Enable for ADCU3
Bit12: Enable for ADCU4
Bit13: Enable for ADCU5
Bit14: Enable for ADCU6
Bit15: Enable for ADCU7
Bit16: Test Pulse Enable for ADCU0
Bit17: Test Pulse Enable for ADCU1
Bit18: Test Pulse Enable for ADCU2
Bit19: Test Pulse Enable for ADCU3
Bit20: Test Pulse Enable for ADCU4
Bit21: Test Pulse Enable for ADCU5
Bit22: Test Pulse Enable for ADCU6
Bit23: Test Pulse Enable for ADCU7
Bit24-27: Max trigger to be kept before busy is set. (these bits are used only when Bit 28 is set.
Bit28: if 0, Busy is set after 2 events Internal fifo=4k byte.
if all data is read out, max data /event is >~1K. Busy should be set after 2 events, so that max 3 events are kept in the fifo.
(Once we stop read out all events, we can relax this condition)
Bit29:
Bit30:
Bit31:

Control register II (R/W) AF51 1108

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0

Data

Bit0-5: Dummy 6bit ROT
Bit6-7: undefined
Bit8-15: Dummy 8bit ROT (8-9: Sys RO, 11-12: Amb, 13-15 Comp.-dep RO)
Bit16-23: Dummy FLTn
Bit24-31: Dummy GBCN

Readout mode

(bit map from 5 bit GFLT readout type to 4 bit ADC R/O type (R/W)
AF51 1180 -- AF51 11FF

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	1	s	s	g	g	g	0	0

ggg: 3bit GFLT component dependent R/O type
ss : 2bit GFLT system readout type
(aa: 2bit ambiguity flag is not decoded)

Data

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	a	t	c	s	s	r

r: raw data on/off
ss: 11: all (no zero suppression)
10: after zero suppression
01: only belong to cluster
00: no strip data
c: cluster data on/off
t: trailer on/off (in raw data)
a: control data on/off
(if 0, pipeline data are only written (1 word/link)

Data status register I (Read only) AF51 1110

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Data

Bit00-07 : ADCU idle (Empty)
Bit08-15 : Error flagged by ADCU (currently always 0)
Bit16-23 : same as 00-07
Bit24-31 : Internal test (b31:pre-startp, b30 internal emp, b29 dfbusy ...
see schematic fltfo18

Data status register II (Read only) AF51 1114

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0

Data

Bit00-07 : ADCU Full (flagged by FLTFORM)
Bit08-15 : ADCU full (flagged by ADCU)
Bit16-23 : N.D.
Bit 24 : Busy: Trigger fifo is full (this never happens)
Bit 25 : Busy: too many events in a short time.
Bit29 : Interrupt enabled
Bit30 : Interrupt request
Bit31 : Event ready (bus : All ADC modules in the crate)

trigger counter (Read only) AF51 1118

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0

Data

Bit00-15 : Number of FLT received (after the last init command)
Bit16-31 : Number of non-aborted FLTs

proc. counter (Read only) AF51 111C

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0

Data

Bit00-15 : Number of Data formatting requests (after the last init command)
Bit16-31 : Number of Events built

DF temporary control register (R/W) AF51 1064

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	0	1	1	0	0	1	0	0

Data

Bit0-2: (meaningless if bit7 is 0), ADCU address for FIFO access
Bit7: If 1, FiFo can be accessed from VME
Bit15: If 1, Self trigger mode, i.e. ADCM is triggered with analog data valid

DF FIFO access (RO) AF51 10c0, AF51 10c8, AF51 10cc

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	1	1	0	0	f	f	0	0

ff: fifo selector 00: raw fifo, 10 strip fifo 11 cluster fifo

Data

bit31-00 : Fifo output.
(The access is permitted only if bit7 of DF temporary control register is set)

DF Data status register I (Read only) AF51 1068

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0

Data

Bit00-01 : FIFO pointer
Bit02 : Data Formatter Busy
Bit03 : Data Formatter End sequence
Bit04-07 : ADCU pointer
Bit08-11 : Data formatting cycle pointer
Bit12-15 : Memory size information
These 16bits are for HW debugging

Bit16-19: not defined
Bit20 : Data full reported from ADCU
(details are in status reg)
Bit21 : Data buffer or Data pointer full
(i.e. or of bit 25,27,29,31)
Bit22 : Bit 20 or Bit 21
Bit23 : BUSY to C&C (and LED)
(Bit 22 .and.
module_online)
Bit24 :
Bit25 : SLT Buffer full
Bit26 : SLT Pointer Empty
Bit27 : SLT Pointer Full
Bit28 :
Bit29 : EVB Buffer full
Bit30 : EVB Pointer Empty
Bit31 : EVB Pointer full

DF Data status register II (Read only) AF51 106C

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	0	1	1	0	1	1	0	0

Data

Bit00-07 : Error in Raw data Header
Bit08-15 : Error in Strip data
Bit16-23 : Error flagged by ADCU
(via data Fifo)
Bit24-27 : not defined

Bit28 : Or of bit 0-23
Bit29 : Error from ADCU/Trigger control
Bit30 : OR of all Error
Bit31 : Halt Request is sent to C&C
(and to LED)

SLT Data Header FIFO (FIFO Read) AF51 1080

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0

Data

m	m	m	m	m	m	m	m	0	0	1	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p

VME address of the next event header.

SLT Data Size FIFO (FIFO Read) AF51 1084

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0

Data

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p

Data size of the event (in byte).

EVB Data Header FIFO (FIFO Read) AF51 1088

Address

m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0

Data

m	m	m	m	m	m	m	m	0	0	1	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p

VME address of the next event header.

EVB Data Size FIFO (FIFO Read) AF51 108C

Address

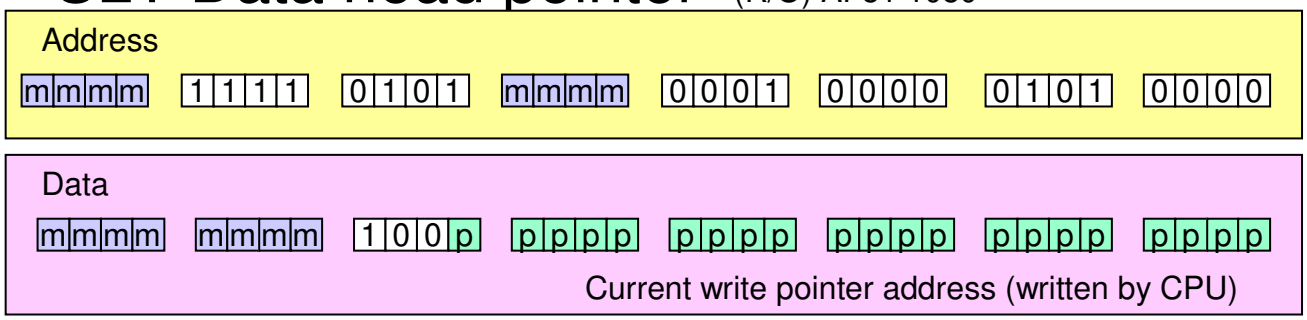
m	m	m	m	1	1	1	1	0	1	0	1	m	m	m	m	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0	0

Data

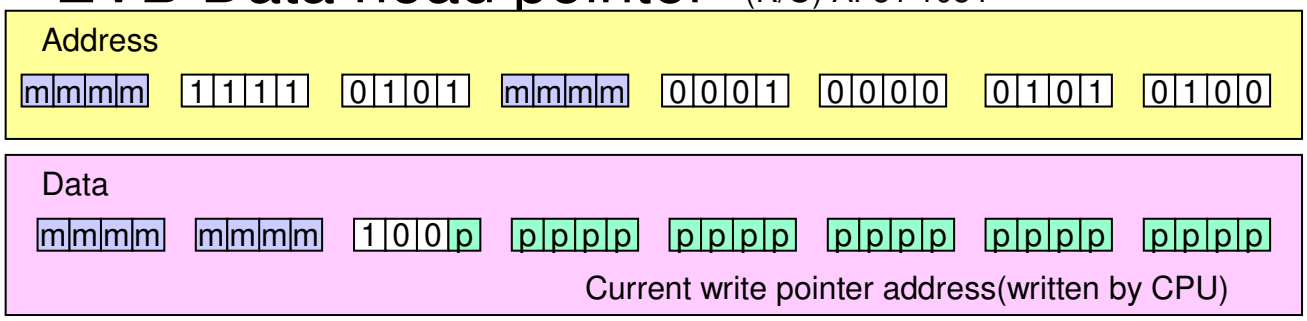
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p

Data size of the event (in byte).

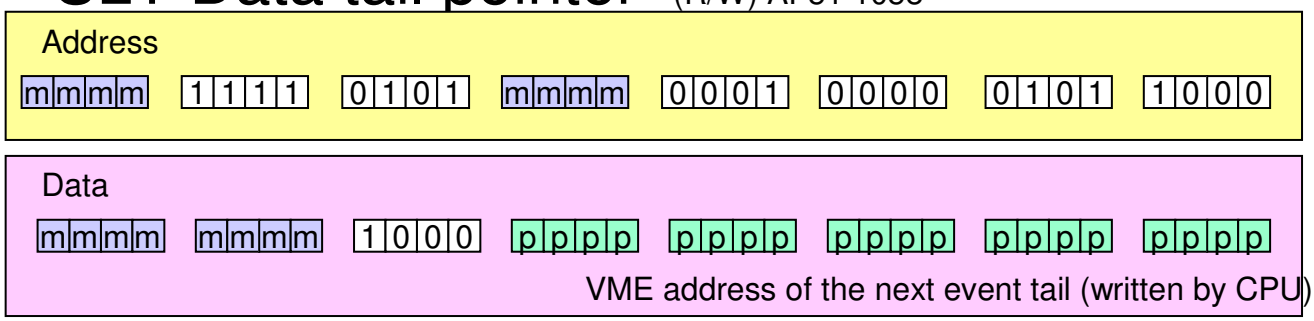
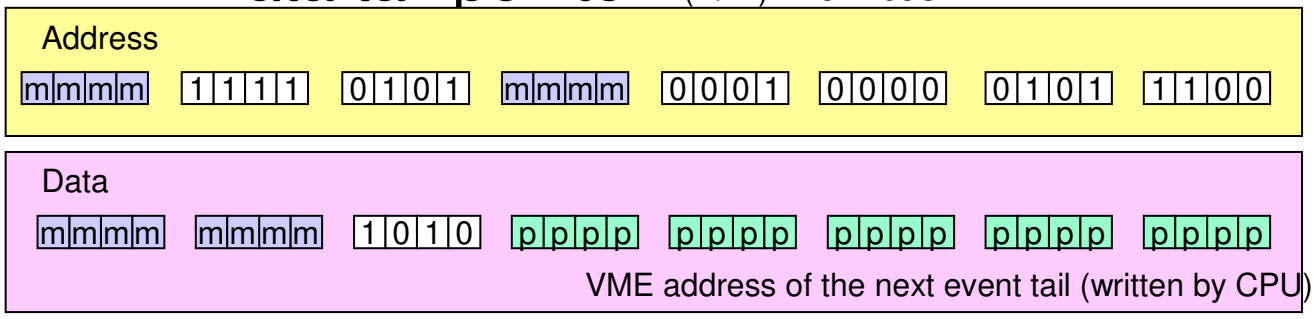
SLT Data head pointer (R/O) AF51 1050



EVB Data head pointer (R/O) AF51 1054



SLT Data tail pointer (R/W) AF51 1058



EVB Data tail pointer (R/W) AF51 105C