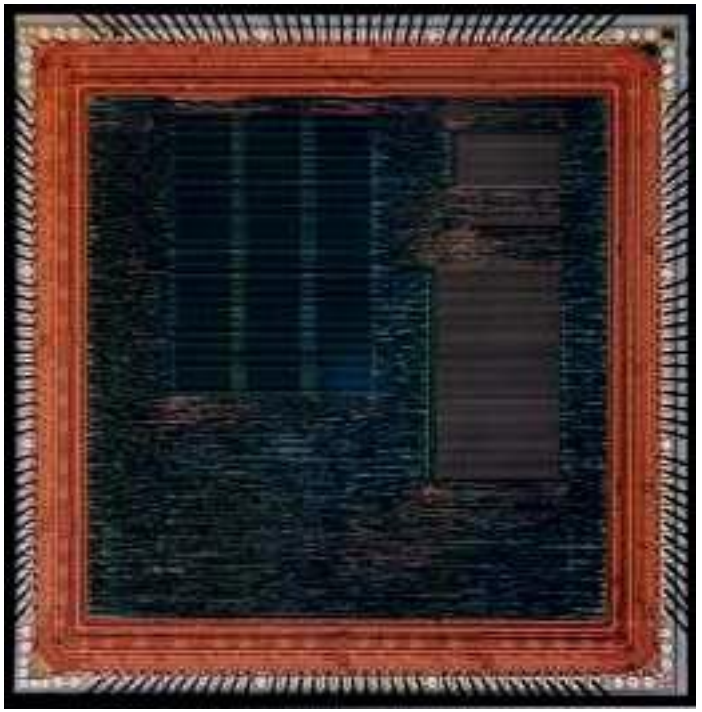
ATLAS Muon TDC (AMT)

Yasuo Arai (KEK)
yasuo.arai@kek.jp
http://atlas.kek.jp/~araiy/

22 Feb. 2001@CERN
ATLAS MDT Electronics
Preliminary Design Review

- Specification
- Design
- Performance
- Schedule



Specifications of ATLAS MDT TDC (AMT)

- ~370 k channels (16,000 chips)
- ~0.5 ns timing resolution
- 400 kHz input rate, 100 kHz trigger rate
- Leading and Trailing edge (width) time measurement
- Trigger Latency > 3 μs
- Low-cost, Low-power (~10 mW) & High-density (24 ch/chip)
- LVDS interface for active signals during measurement
- Serial output (40 Mbps)
- Radiation Tolerant (~11 krad, 1.2×10^{13} n/cm^2 @10year LHC)
- JTAG I/F, BIST, Serial control
- 144 pins plastic QFP

Short History

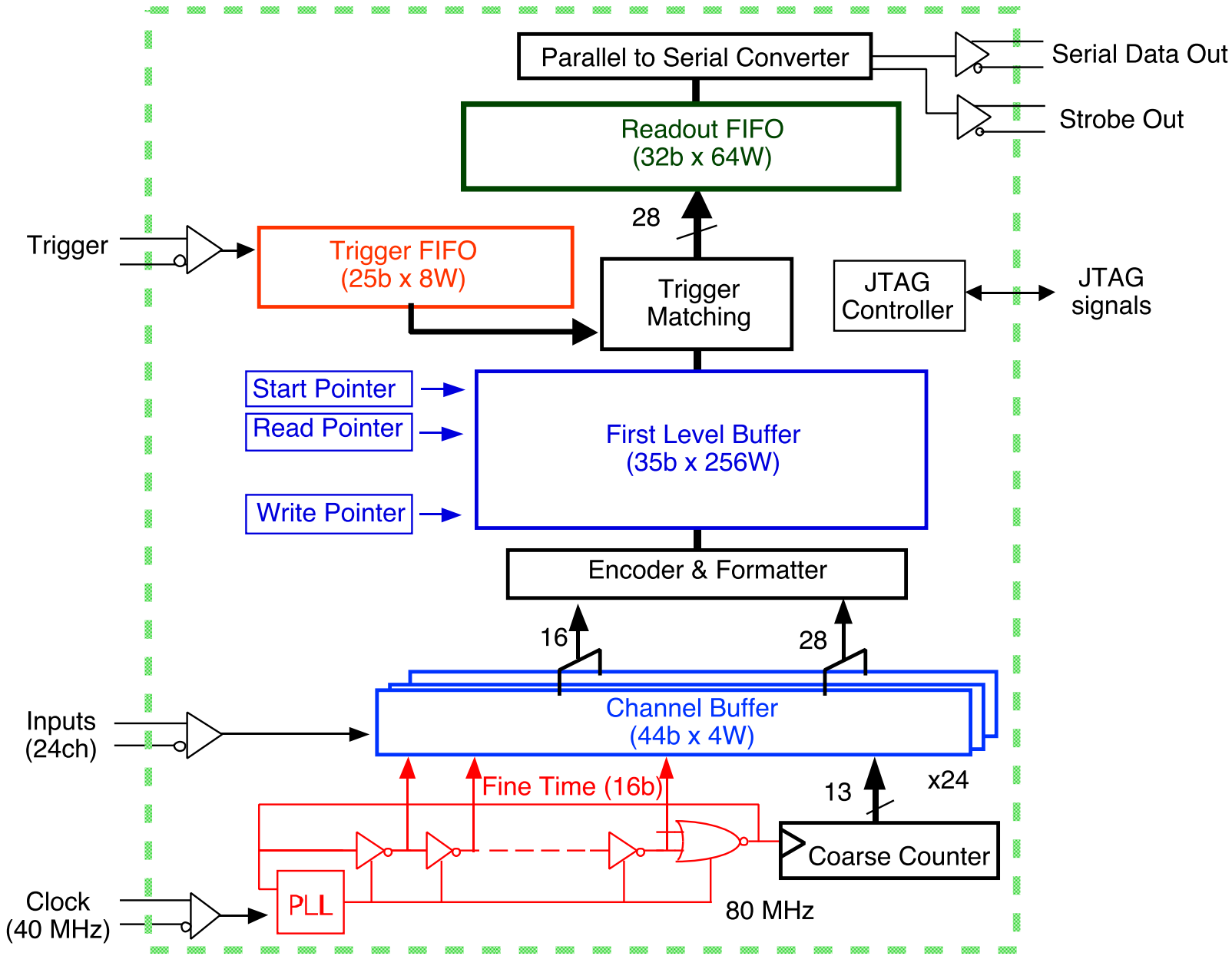
1996 Design study (Y.Arai & J.Christiansen).

1998 (CERN) AMT-0

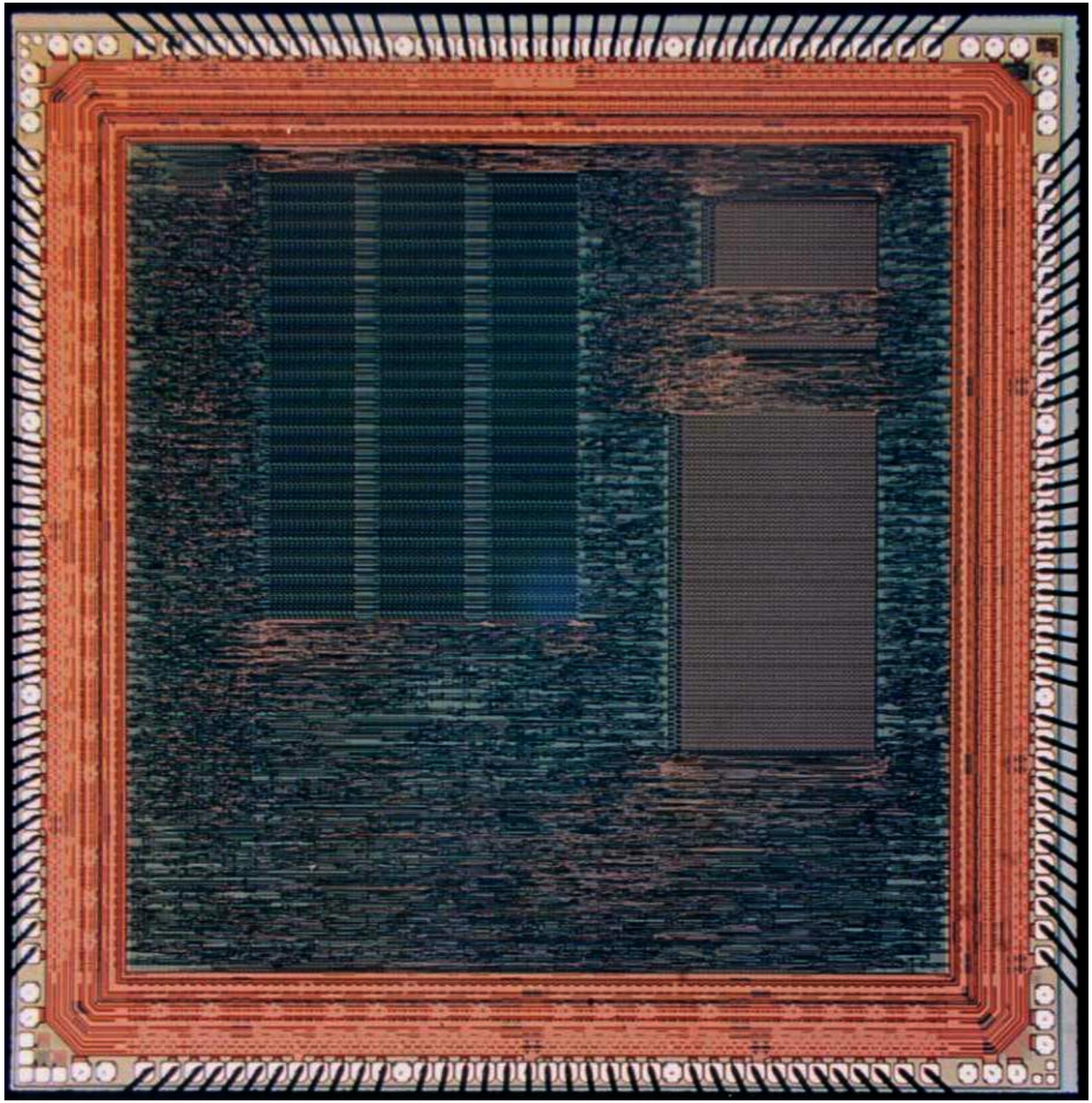
1999 (KEK) AMT-TEG

2000 AMT-1

2001 *(AMT-2)*

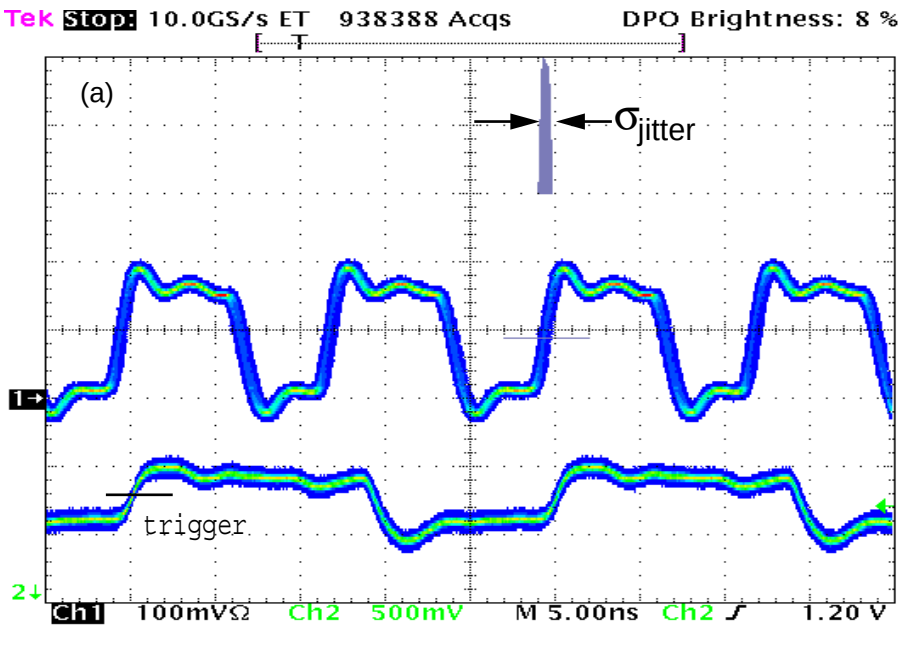


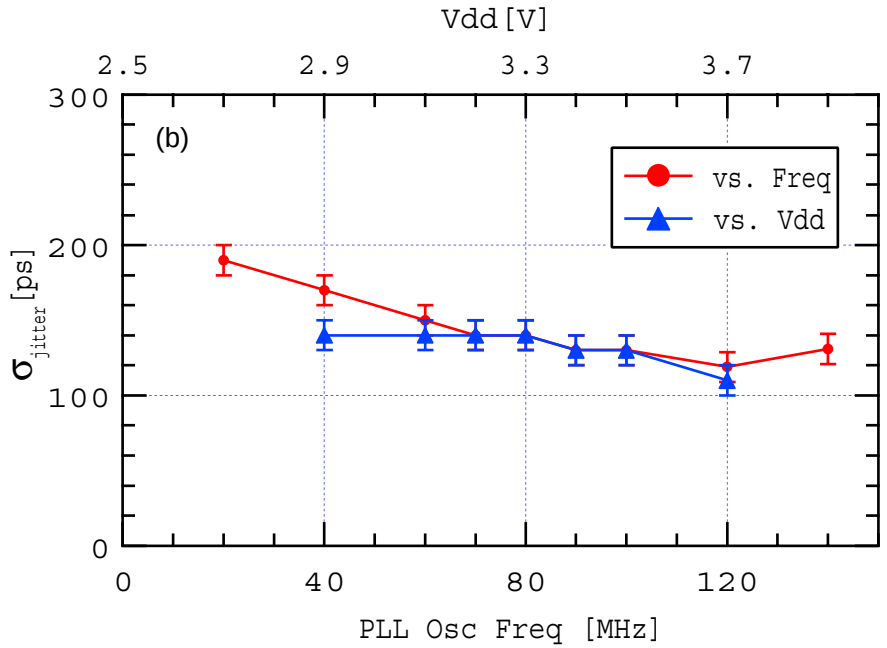
Block Diagram of the AMT



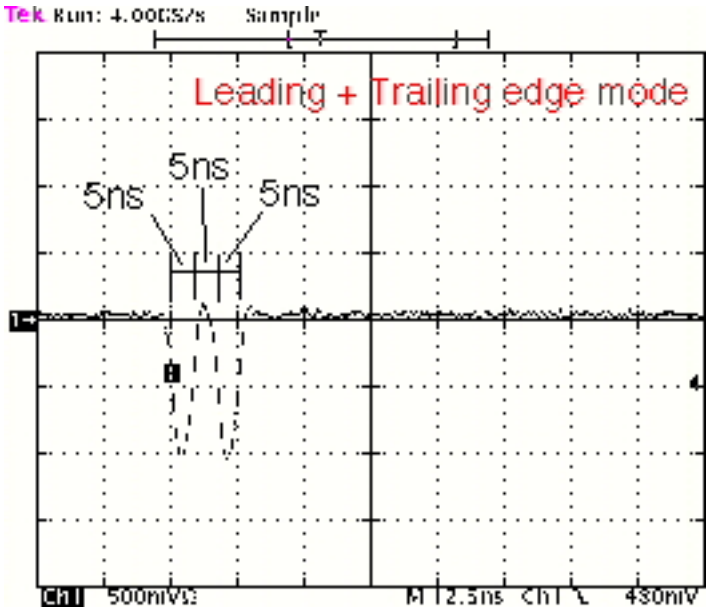
AMT-1 chip (0.3µm Toshiba CMOS Gate-Array, 6 mm x 6mm)

PLL Stability

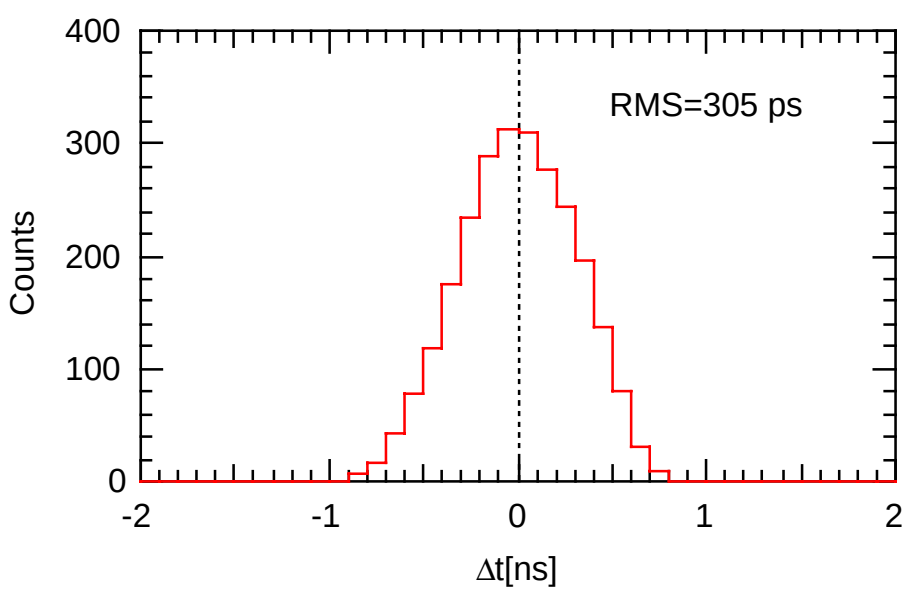




Double Pulse Resolution

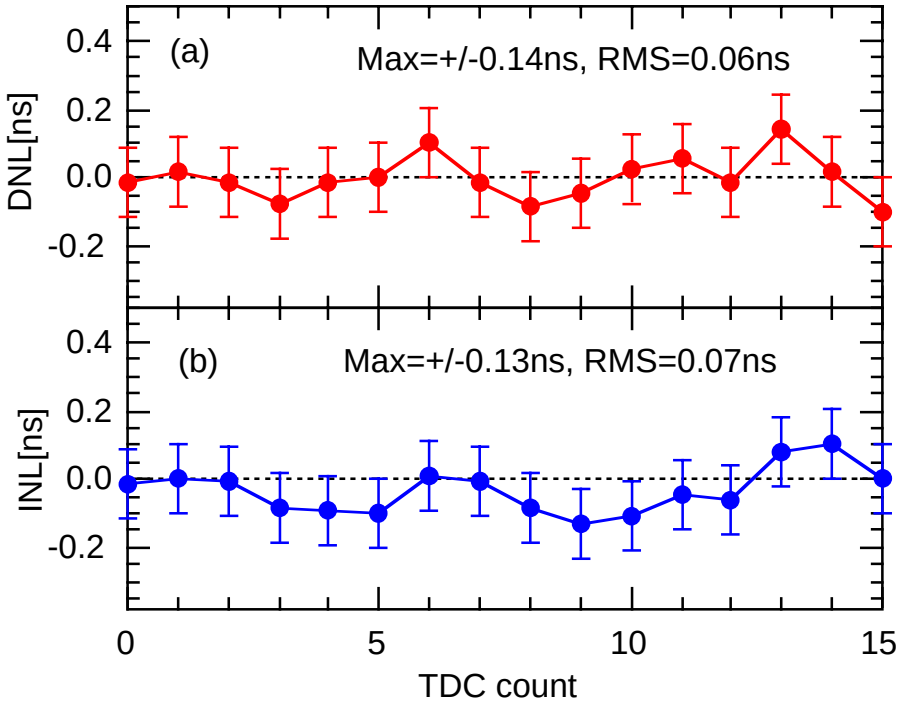


An example of pulse which recorded successfully



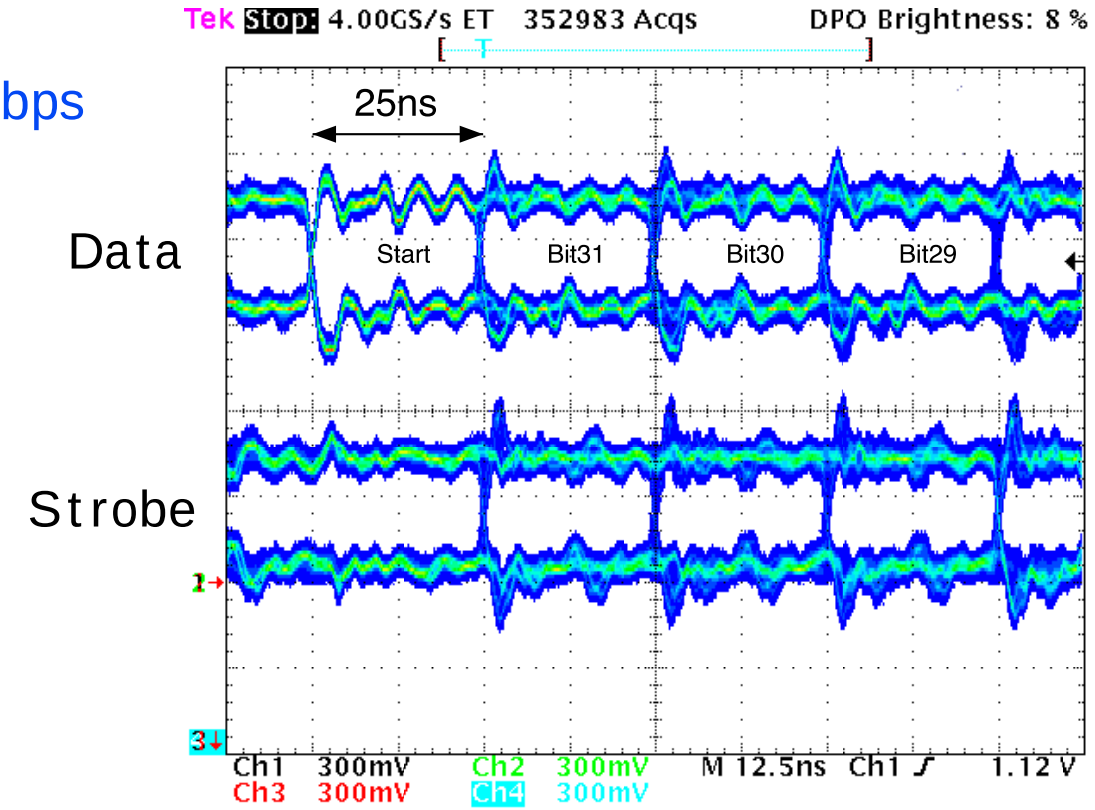
Time Resolution

Differential & Integral Non-Linearity



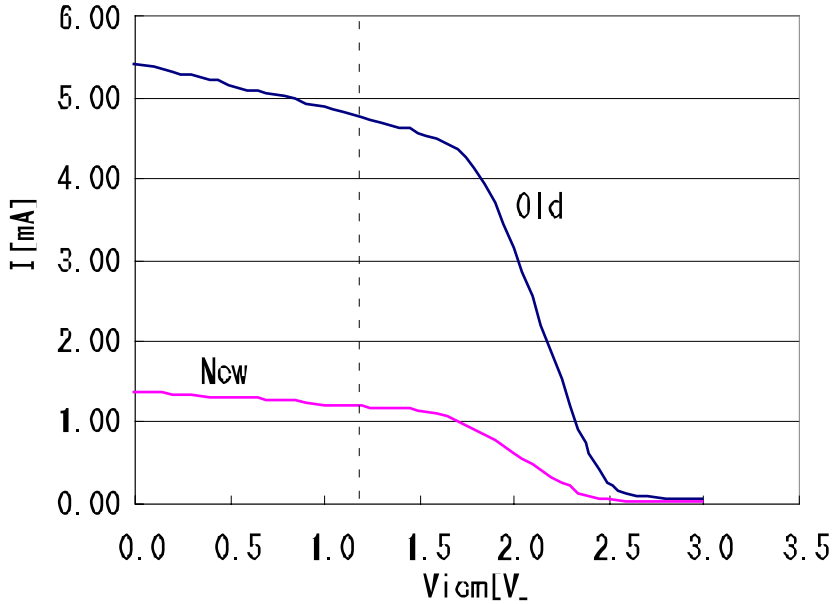
Serial Output

LVDS output
waveform at 40 Mbps



Power Consumption

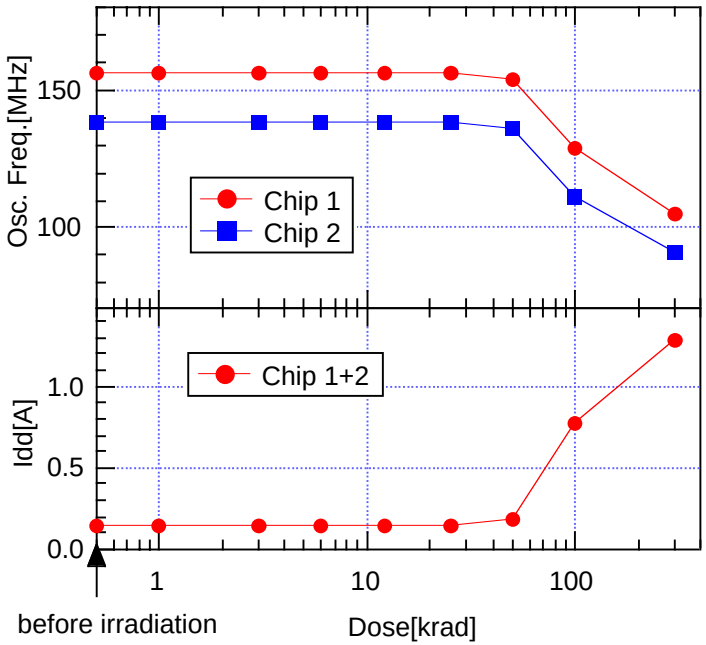
- Power consumption of the AMT-1 is ~500 mW/chip (~20mW/chan)
- Factor two larger than the target value
- Main source of the power consumption is LVDS receiver (~16 mW).
- A new LVDS receiver is under development which consumes only 1/4 of the present receiver

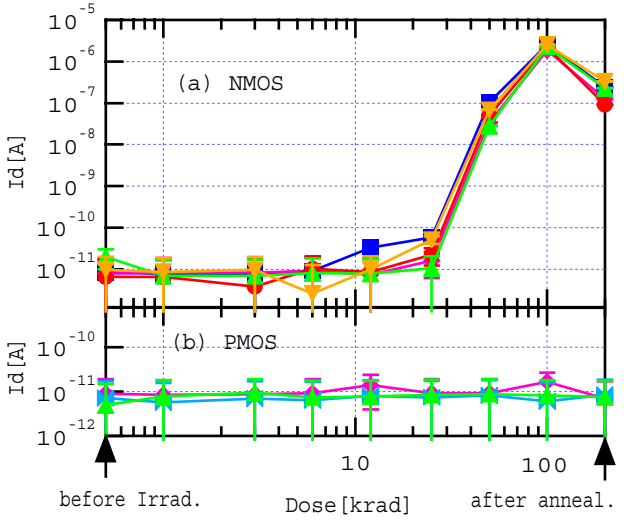


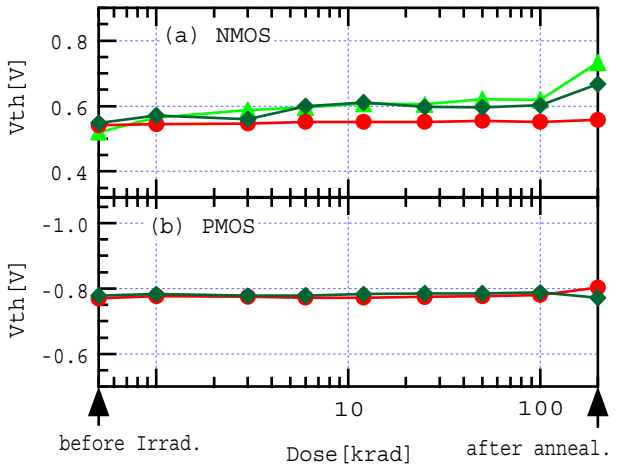
Radiation Tolerance

Total Ionizing Dose (γ)

- Source : ^{60}Co (~90 rad(Si)/sec)
- Follow MIL-STD method.
- 1 week annealing at 100 ° C
- Estimated level is <11 krad/10 year
  (@Endcap, Safety factor=4)







Radiation Tolerance (cont.)

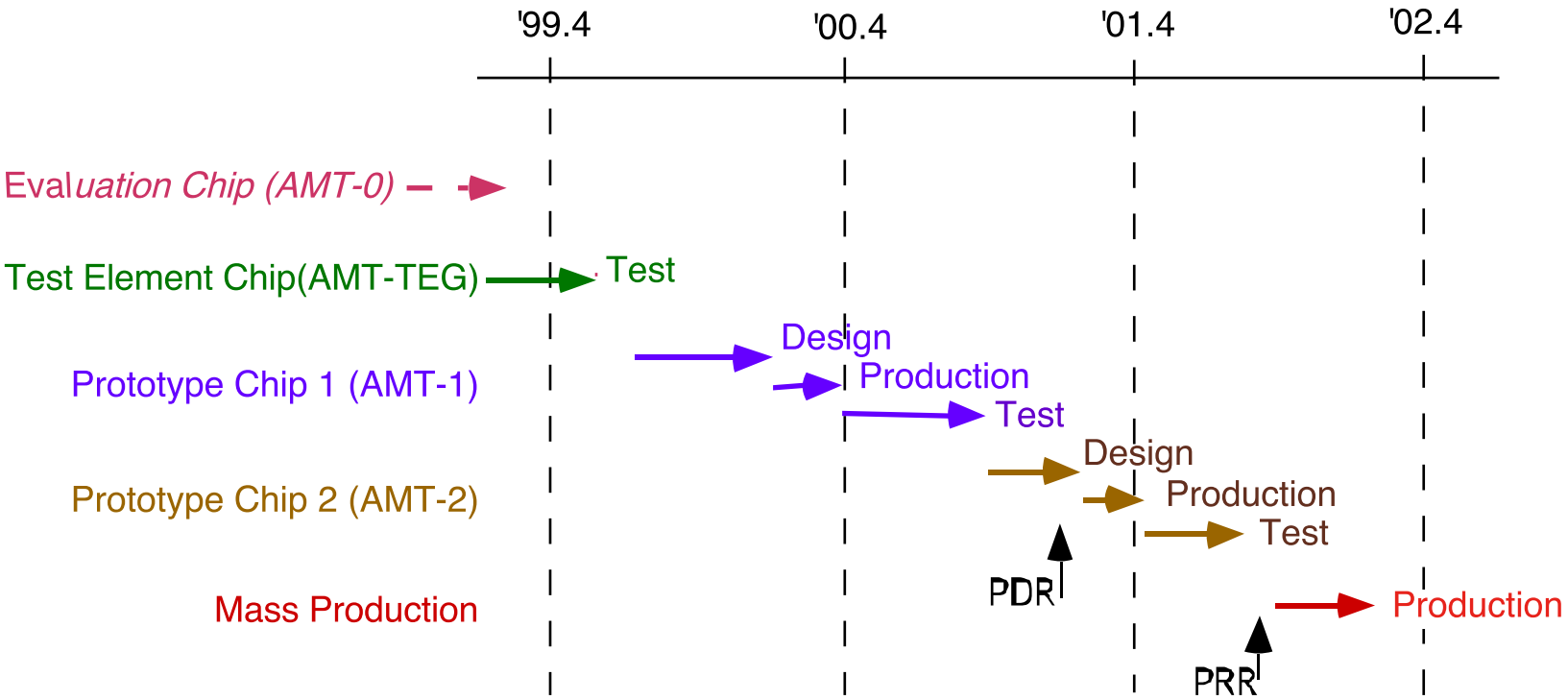
Displacement Damage (neutron)

- Irradiated at the PROSPERO reactor
- 8 chips :1.0 x 10^{13} n/cm^2, 4 chips : 1.6 x 10^{13} n/cm^2
- Expected neutron flux is <1.2 x 10^{13} n/cm^2/10 years
- Any damage was not observed

Single Event Effect (hadrons)

- No Measurment yet for Single Event Effect (SEE)
- Estimated fluence is <10^{10} h/cm^2/10years.
- Assume a SEU cross section of 10^{-13}/cm^2/bit,
  => 1.5 SEU/day/MDT for the contents of CSR.
- AMT can detect 1 bit SEU and report by an error word
- Even AMT is stacked, the effect is only for 24 ch
- SEE test will be done in Japan

Schedule


'99.4
'00.4
'01.4
'02.4
Evaluation Chip (AMT-0)
Test Element Chip(AMT-TEG)
Test
Design
Prototype Chip 1 (AMT-1)
Production
Test
Design
Prototype Chip 2 (AMT-2)
Production
Test
PDR
Mass Production
Production
PRR

Summary

- A prototype TDC chip (AMT-1) was successfully developed.
- AMT-1 fulfils most of requirements.
- ~400 AMT-1 chips will be used in the 10 kch test.
- New LVDS receiver has been developed to reduce power consumption.
- SEE test is planned in Japan.
- AMT-2 is now under development, and will be submitted in March.
- Mass production wiil be finished early next year.