AMT Status

Yasuo Arai (KEK)
yasuo.arai@kek.jp
http://atlas.kek.jp/~araiy/

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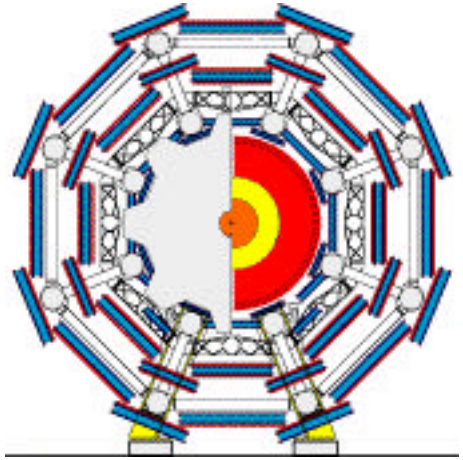
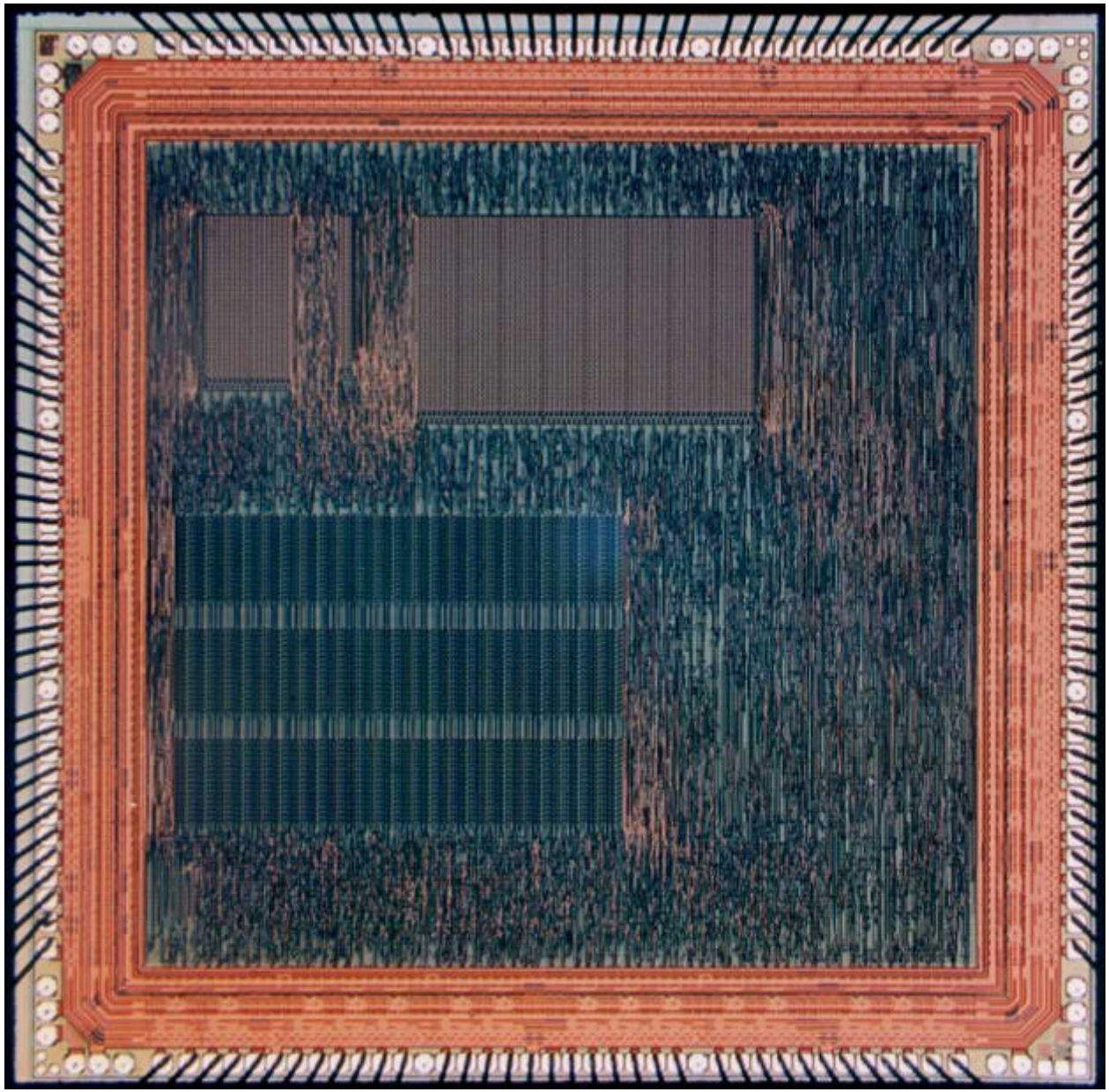
Muon Elec. W.S.@CERN

- End of Jan.:AMT-1 submitted
- End of Mar.:20 ceramic +200plastic packaged chip delivered.
- Testing
  PLL stability
  CSR read/write
  JTAG I/F
  Hit In -> Trigger -> Serial Out
  Power Consumption



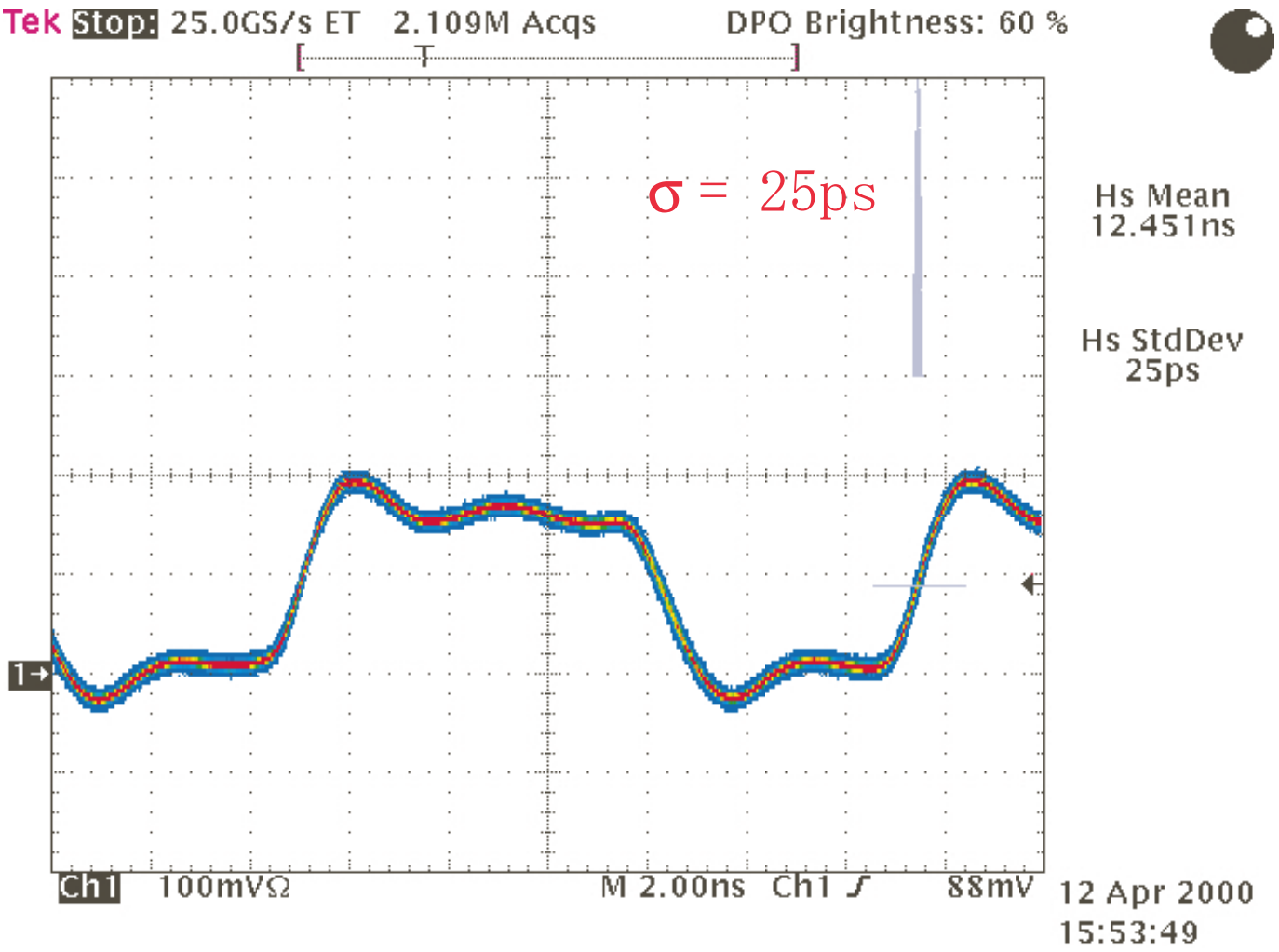
AMT-1 Specification

- ★ Process : CMOS 0.3 μm Gate Array (Toshiba TC220G)
- ★ No. of Gate Used : 106 k gates (35% of master)
- ★ Control & Status Registers : 12 bit x 21 (252 bits)
- ★ 24 channels, 0.78 ns/bit, 17 bit dynamic range
- ★ 256 word L1 Buffer, 64 word Readout FIFO
- ★ 4 word Channel buffer, 8 word Trigger FIFO
- ★ LVDS I/F, JTAG, BIST logic
- ★ Chip size : 6.4 mm x 6.4 mm
- ★ Package : 0.5 mm pitch, 144pins QFP



Photograph of the AMT-1 chip

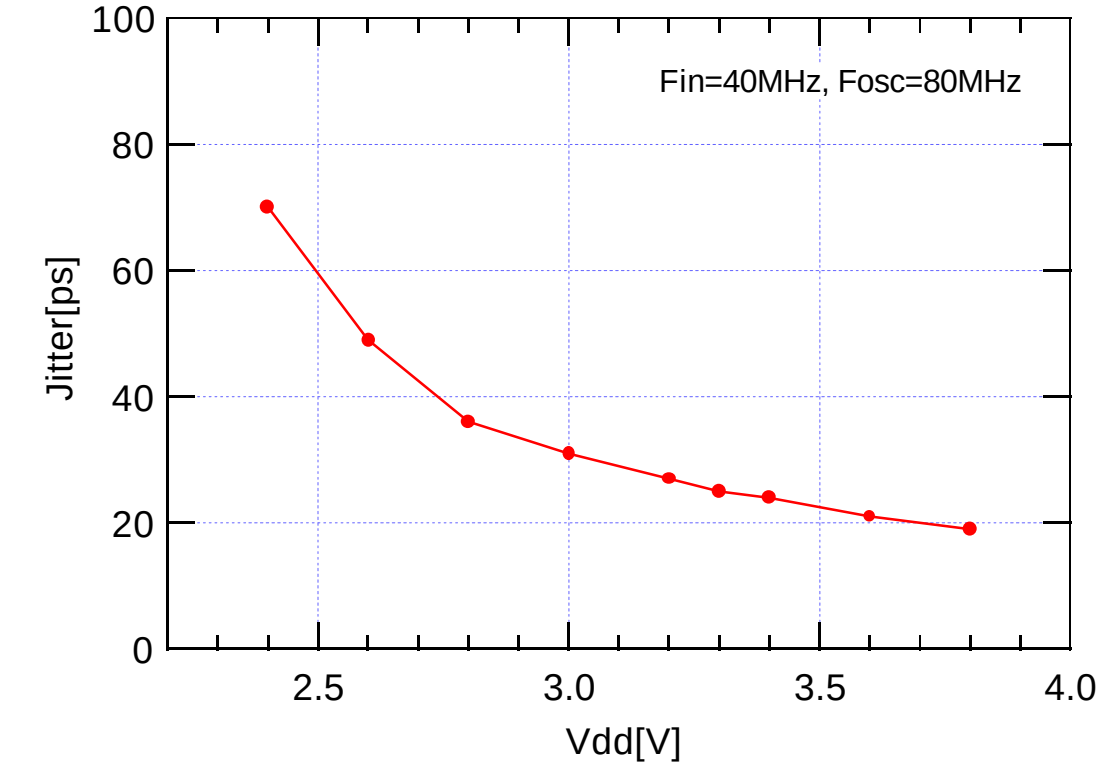
PLL Jitter

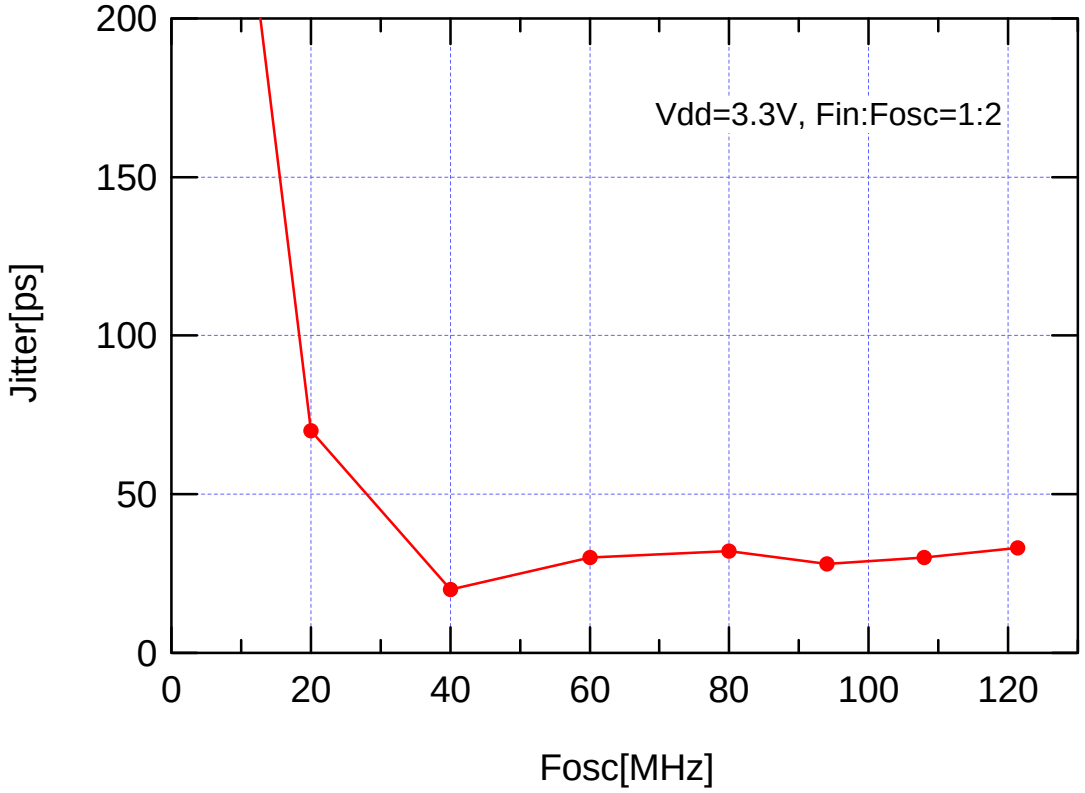


Fin = 40MHz, Fosc = 80MHz

00.05.02 Y.A.

PLL Jitter





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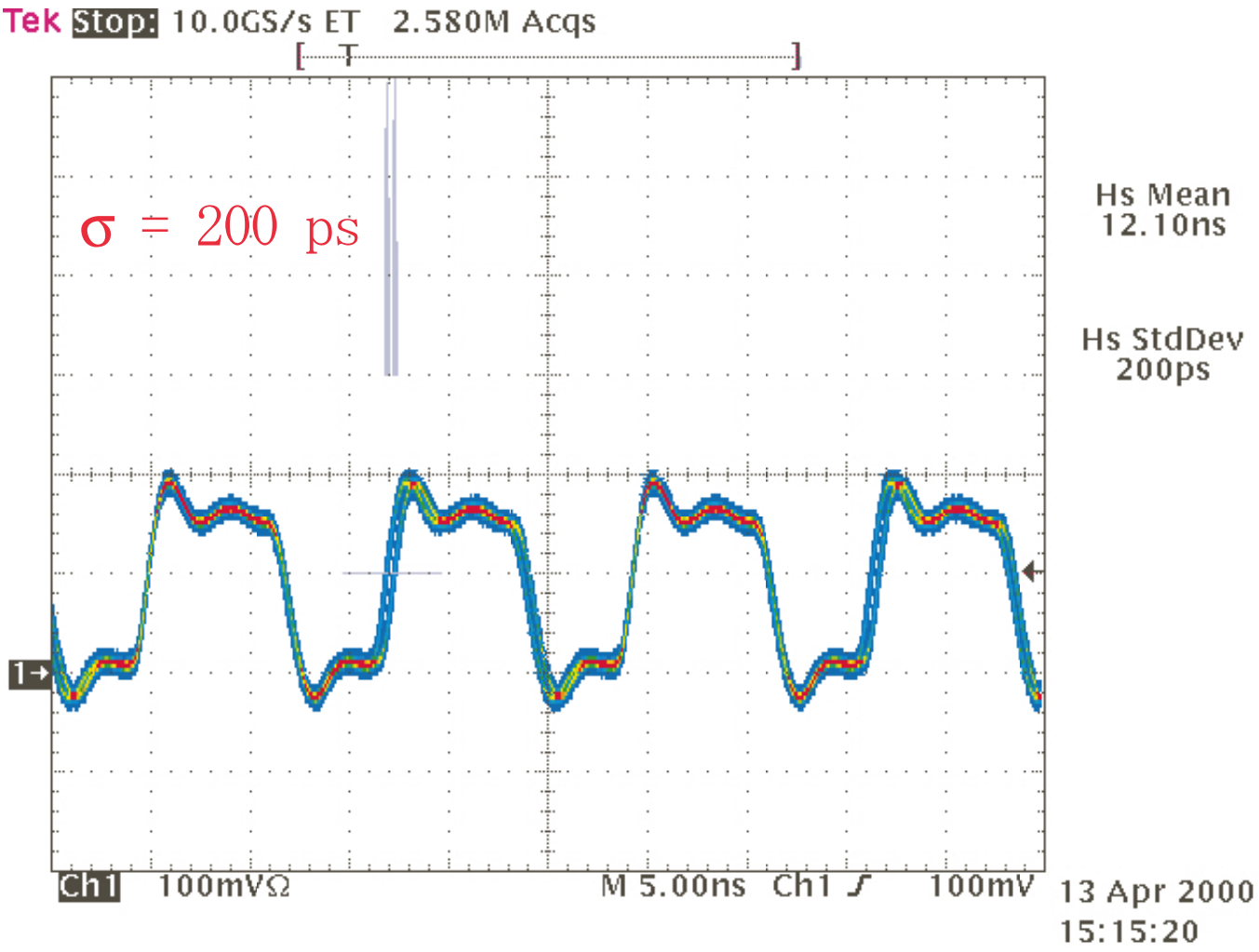
PLL Jitter (Unstable Point)



Fin = 41 MHz, Fosc = 82 MHz

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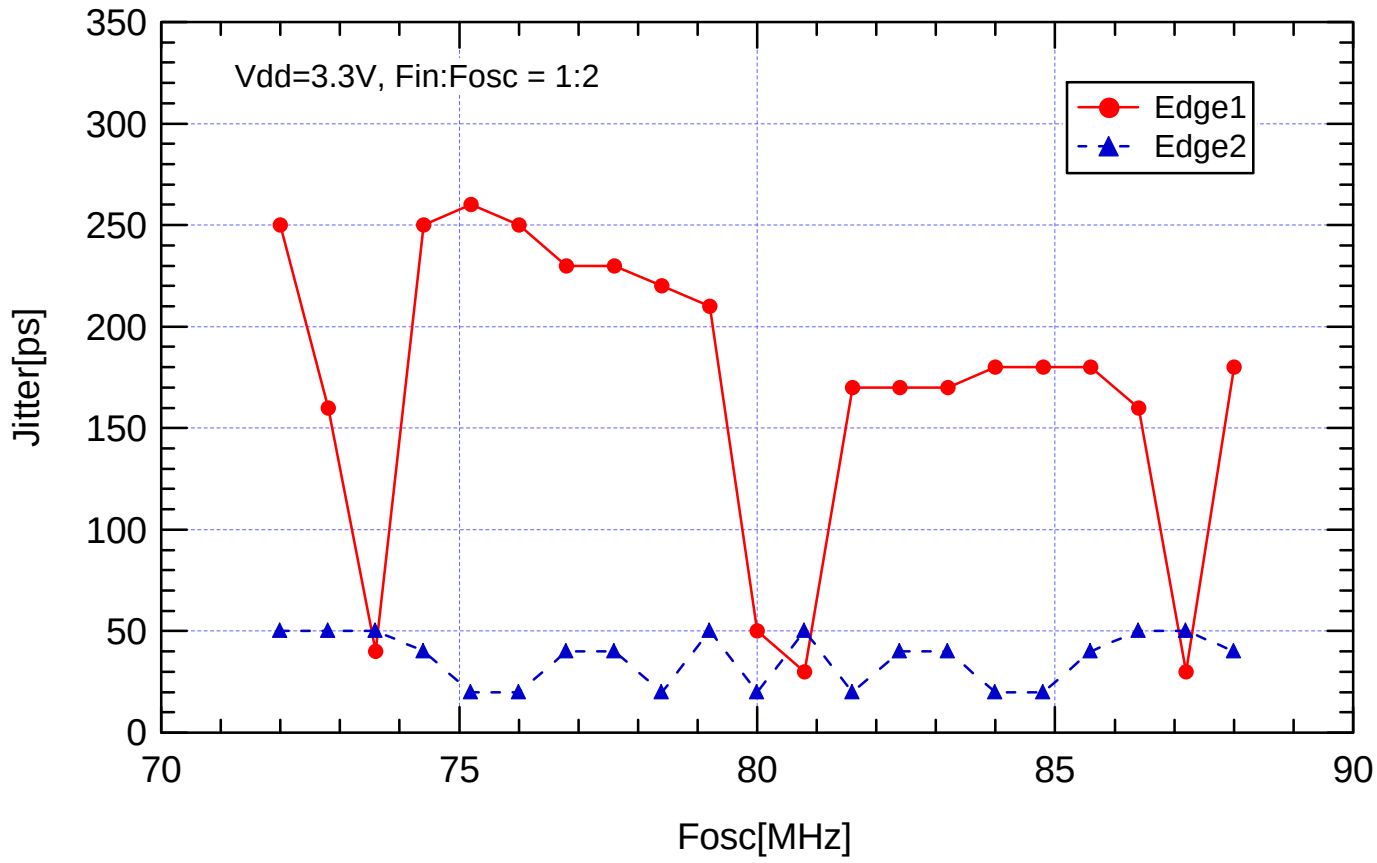
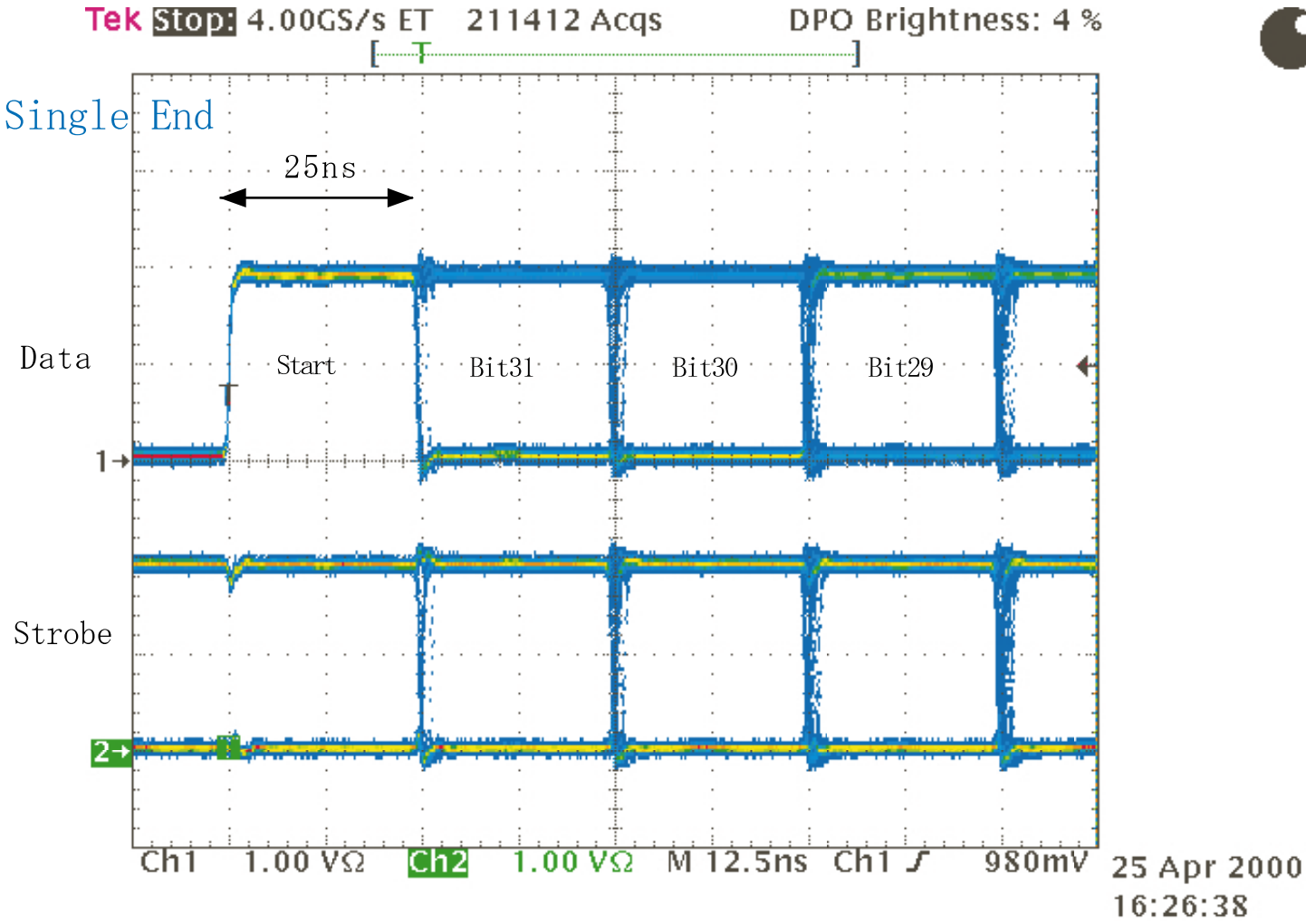
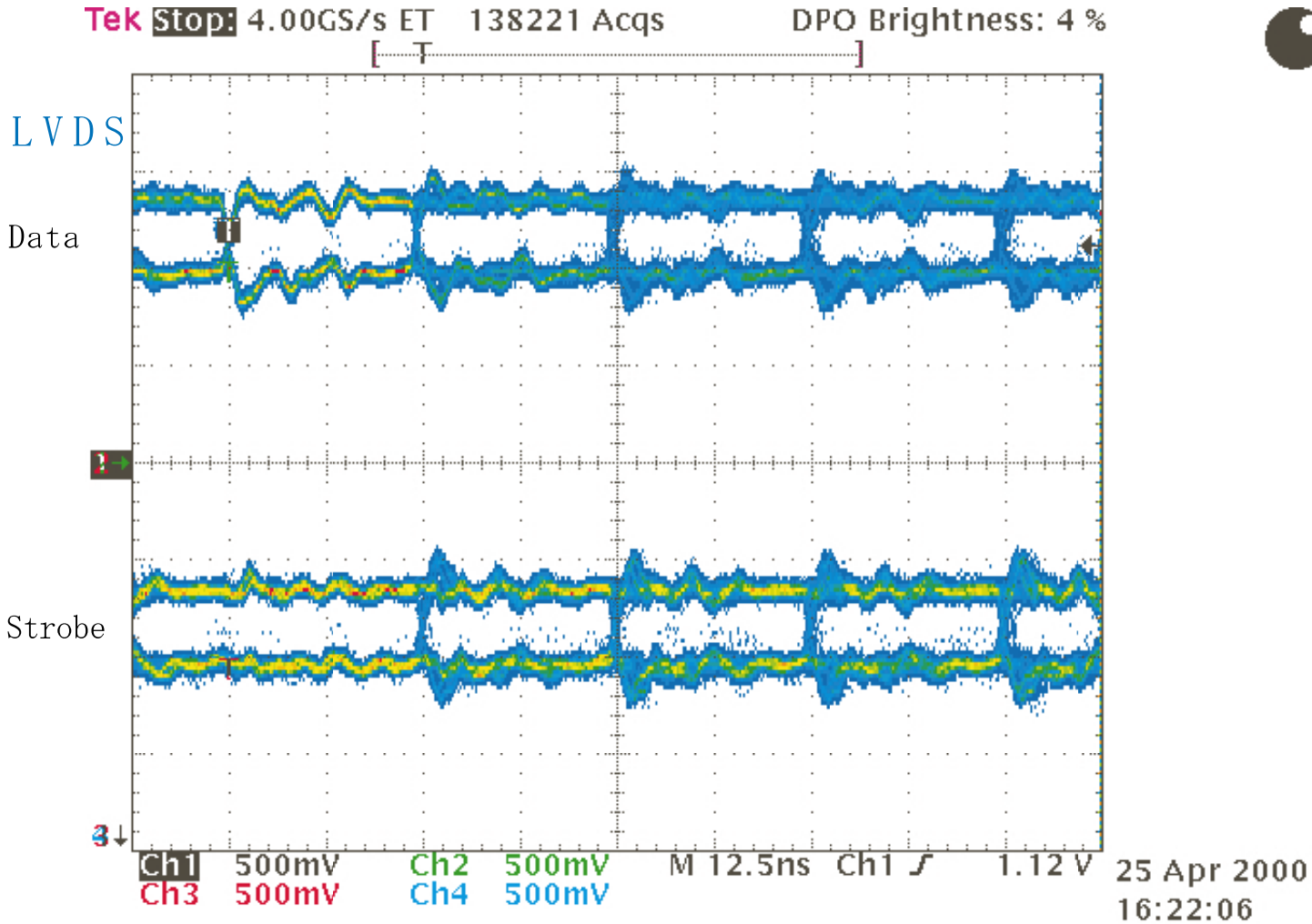
PLL Jitter (1st Edge & 2nd Edge)



σ(total)
≈ σ(digital) ⊕ (σ(edge1) + σ(edge2))/2
≈ 225 ps ⊕ (50 ps + 250 ps)/2
≈ 270 ps

LVDS Serial Output





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Power Consumption

Simulation:

400 mW (Internal Circuit)
+ 480 mW (16mW x 30 LVDS receivers)
= ~900 mW/chip

Measurement:

3.3V x 148 mA = 488 mW/chip (20mW/chan)
(@400kHz hit, 100kHz Trigger)

LVDS receiver:

New Low Power design will be designed at Toshiba.
Thus more reduction in power is expected.

AMT Schedule

- 98.12 AMT-0 (Evaluation Chip) produced (1,000 chips)
- 98.12 AMT-TEG (Test Element Chip) produced
- 99. 6 AMT-TEG Circuit & Irradiation Test End
- 00. 3 AMT-1 ES chip produced
- 00.4-8 AMT-1 Circuit Test & Radiation Test.
- Summer ASD Lite -> AMT-1 -> CSM-0 Test @Boston?
- 00. 9? Design Review
- 01. 1 AMT-2 (2nd Prototype Chip) will be submitted
- 01. 6? Production Readiness Review
- 01. 9 AMT mass production start
- 02. 1 AMT mass production end

Summary

- AMT-1 has been tested and no major problem was found yet.
- PLL jitter become large at some frequency, but still good enough for MDT (σ_{total} ~ 270ps).
- Power consumption was much lower (~20mW/ch) than simulation value. More reduction is expected in AMT-2 due to new LVDS receiver.
- Preliminary User's manual is available from http://atlas.kek.jp/~araiy/ .
- Total test with ASD and CSC will be planned.