第３回IPアワード応募書類：特徴の説明

１．タイトル：素粒子実験用時間測定チップ

２．分野：ハードVC

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８．要約：

素粒子実験で用いられるミューオン検出器用の高精度時間測定チップを開発した。使用したプロセスは0.3μmのCMOS Gate-Arrayで使用ゲート数は約11万ゲートである。サブナノ秒の時間分解能を実現するため、40MHzのシステムクロックからPLLで安定化した非対称リング発信回路という新規回路を開発しマクロライブラリー化した。80MHzで発振するこのリングオシレターからさらに16個のタップを引き出すことにより780ps/bitの分解能を実現しており、実験でRMS時間精度300psを確認した。

このチップは１チップに24の入力チャンネルを持ち、トリガー対応回路により選別されたデーターのみが読み出される。2005年からCERN研究所で行われる実験において、40万チャンネル使用される予定である。

Time measurement VLSI for High-Energy Physics Experiments

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1. INTRODUCTION

World largest proton-proton colliding-beam accelerator LHC (Large Hadron Collider) is now under construction at CERN (European Organization for Nuclear Research) in Geneva. One of the experiments at the LHC is ATLAS experiment [1] which will start to run on July 2005.

Proton beams collide at every 25 ns and generates hundreds of secondary particles in each collision. Muon detector of the ATLAS requires a high-rate (~400 kHz) time-to-digital converter (TDC) with a sub-nano second time resolution. The TDC receives detector signal and measures the time of the leading edge and its pulse width. The measured data must be kept in the chip until a trigger signal issued about 3 μsec later.

Since the number of channels used are very large (370k channels), the device must be low power, high density and low cost. In addition, the chip is attached to the detector, so it must have adequate radiation tolerance for gamma-rays, neutrons and charged particles.

We have developed several kinds of TDC LSI's called a time memory cell (TMC) [2], but the new TDC (named AMT: ATLAS Muon TDC) is more demanding [3]. In addition to the time digitizer circuit, it also includes data processing unit which selects relevant data to a trigger, LVDS input/output, a JTAG interface, and a Built-In Self-Test circuit for memories. The chip was developed by using a 0.3 μm CMOS gate-array technology (Toshiba TC220G). The number of used gate is about 110 k gates.

2. DESIGN FLOW

Although the technology is a gate-array, we have made intensive analog simulation with HSPICE and paid much attention to cell layout to achieve a sub-nano second timing resolution. Several macro cells are developed for time critical and analog parts. These layout are done manually. Careful floor planning are also done to minimize route of the time critical signals.

Other pure digital parts are written in Verilog code, and simulated in Cadence Verilog-XL. Then the circuits are synthesized by using Synopsys design compiler. Final design is confirmed with Toshiba's VSO (Verilog Sign Off System) softwares.

3. CIRCUIT DESCRIPTION

Photograph of the AMT-1 chip is shown in Fig. 1 and its block diagram is shown in Fig. 2.

Accurate timing signals are derived from an asymmetric ring oscillator [4] (Fig. 3) which is stabilized with a Phase Locked Loop (PLL) circuit. The PLL locks at 80 MHz from a LHC beam clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained (fine time). To extend timing range, there is a 13 bit counter which is counted up at 80 MHz (coarse time).

Although normal ring oscillator has odd number of stages, the asymmetric ring oscillator can generate even number of equally separated timing signals. This feature is very desirable to get a binary number by combining the fine time and the coarse time. Furthermore each stage of the oscillator is very simple and well fit to the gate-array structure (2 PMOS and 2 NMOS transistors) while attaining adequate timing resolution.

When a hit signal is arrived, the fine time and the coarse time are stored in individual channel buffers. The time of both leading and trailing edge of the hit signal can be stored. Each channel has a 4-word buffer where measurements are stored until they can be written into the common level 1 buffer. In a pulse width measurement mode, the width is calculated before storing to the level 1 buffer.

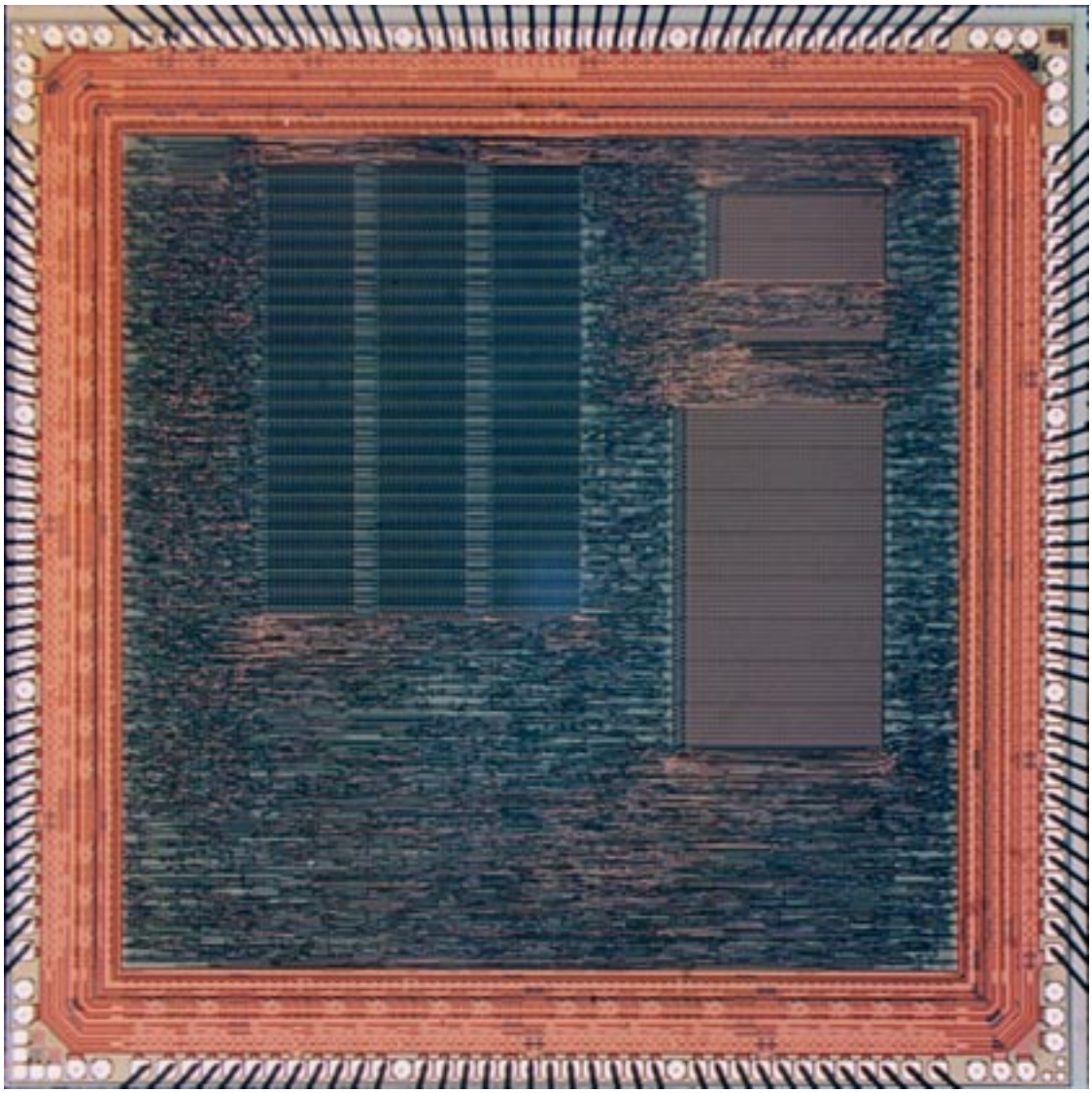

Fig. 1 Photograph of the AMT-1 chip. The die size is about 6 mm by 6 mm. Large block at upper left side is the channel buffer, and the asymmetric ring oscillator is located at upper left corner.

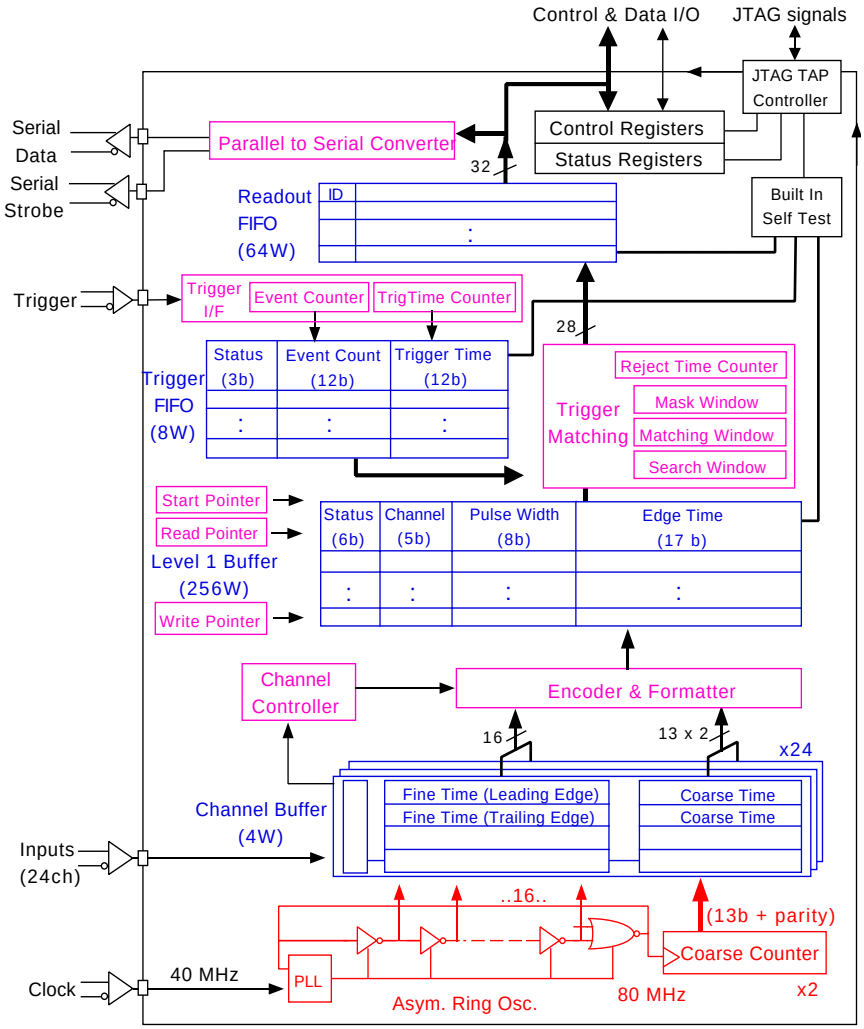

Fig. 2 Block diagram of the AMT-1 chip.

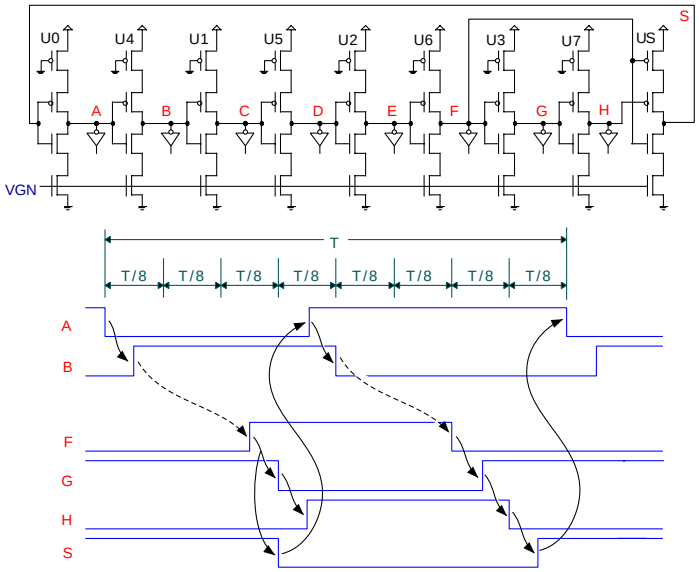

Fig. 3 Eight stages asymmetric ring oscillator. In AMT-1 16 stages are used. VGN is a delay control signal from the PLL. Falling edge timings of nodes A~H are used.

4. MEASUREMENT RESULTS

A. PLL and Ring Oscillator

We observed the jitter of the PLL circuit by measuring the time distribution of the oscillator output relative to an input clock. Standard deviation of the distributions for different frequencies and power supply voltages are plotted in Fig. 4. The jitter is about 140 ps at operating condition (80 MHz and 3.3V) and the PLL is stable in broad range (20-140 MHz, 2.9-3.7 V). This value is small enough for our purpose which requires sub-nano second resolution.

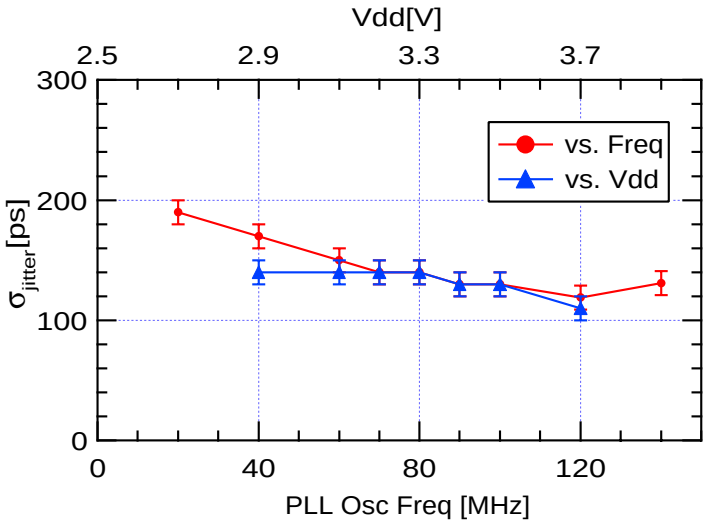

Fig. 4 PLL jitter measurement. Distributions of the jitter are measured, and their standard deviations are plotted for each oscillating frequency and supply voltage (Vdd).

B. Time Resolution and Non-Linearity

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The result is shown in . The RMS (root mean square) value of 300 ps, which includes quantization error of 780ps/√12 (=225ps), is obtained.

Non-linearity of the time measurement was also measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. Both the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are small enough (RMS < 70 ps) for our purpose.

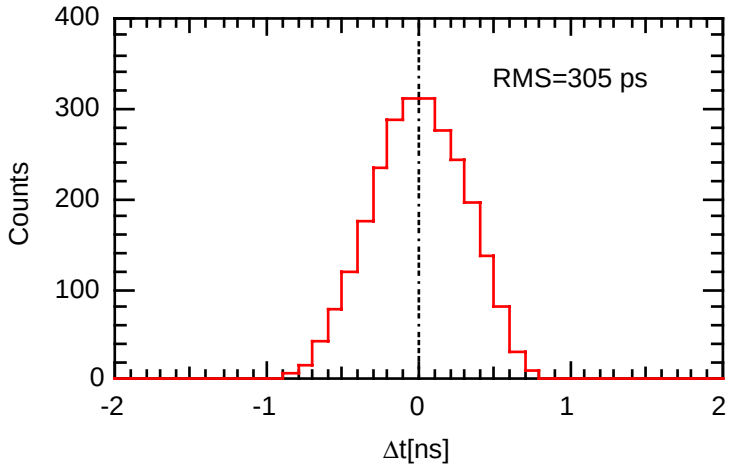

Fig. 5 Time resolution measurement. Input clock frequency is 40 MHz and time bin is 781.25 ps/bit. The data contains digitization error of 225 ps.

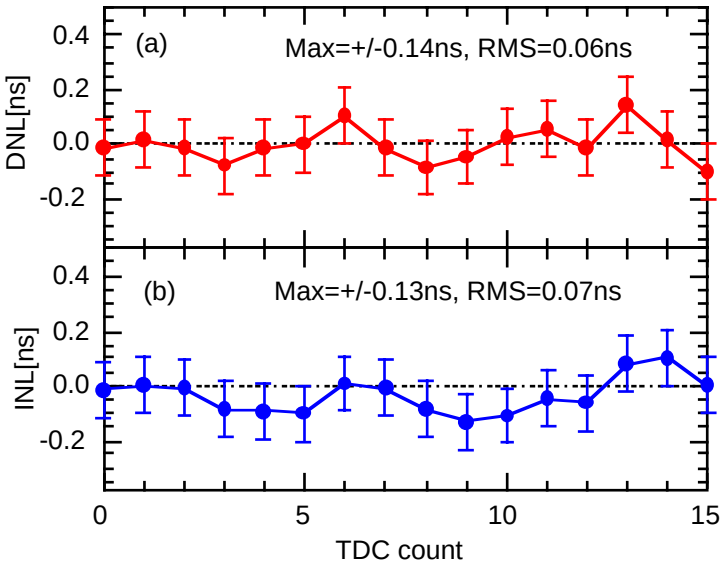

Fig. 6 (a) Differential non-linearity, and (b) integral non-linearity measurement.

5. SUMMARY

A prototype TDC chip (AMT-1) was developed for high-energy physics experiments. The chip was fully functional and 300ps RMS resolution was obtained. Total power consumption of the chip is around 500 mW. Most power consuming parts in present design is LVDS receivers (30 receivers). Reduction of the power is planned by optimizing the receiver circuit. Mass production is scheduled at the end of year 2001.

Reference

[1] http://atlasinfo.cern.ch/Atlas/, http://atlas.kek.jp/~araiy/

[2] Y. Arai and M. Ikeno, “A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution”, IEEE Journal of Solid-State Circuits, Vol. 31, No. 2, Feb. 1996, p.212-220.

[3] Y. Arai, "Development of Frontend Electronics and TDC LSI for the ATLAS MDT", Nucl. Instr. Meth. A. Vol. 453, pp. 365-371 (2000).

[4] "Voltage-Controlled Oscillating Circuit", Japanese patent No. 2663397, US patent No. 08/380,580, European Patent No. 0676863.

Table. 1 AMT-1 Specifications

(at system clock frequency of 40 MHz)

• Least Time Count	0.78 ns/bit (rising edge) 0.78-100ns/bit (falling edge)
• Time Resolution	RMS = 300 ps (rising edge) RMS = 300ps ~ 29ns (falling edges, selectable)
• Dynamic range	13 + 4 = 17 bit (102.4 μsec)
• Integral Non Linearity	Max = +/-70 ps
• Differential Non Linearity	Max = +/- 70 ps
• Difference between channels	Maximum one time bin
• Stability	< 0.1 LSB (3.0 - 3.6 V. 0 - 70 ˚C)
• Input Clock Frequency	10 - 70 MHz (@ x2 mode)
• PLL mode	x1, x2, x4 or x8
• Internal System Clock	Input Clock x (PLL mode) / 2
• No. of Channels	24 Channels
• Level 1Buffer	256 words
• Read-out Buffer	64 words
• Trigger Buffer	8 words
• Double Hit Resolution	<10 ns
• Max. Hit rate	500 kHz per channel
• Data Output	32 bit parallel port or Serial port
• Register Access	12 bit parallel or JTAG port
• Built-In Self Test	Through JTAG port
• Hit Input Level	Low Voltage Differential Signaling (LVDS) Internal 100 Ohm termination.
• Supply Voltage	3.3+-0.3V (< 200 mA)
• Temperature range	0 - 85 Deg. Cent
• Process	0.3 μm CMOS Sea-of-Gate (Toshiba TC220G) die size: 6 mm x 6 mm
• No. of Used Gates	~110k gates
• Package	0.5 mm lead pitch, 144 pin plastic QFP