AMT-VME

64Ch AMT-VME Module User's Manual

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1. General Features

64ch AMT-VME Time-to-Digital Converter Module

- 64 channels in Double-height, Single-width VME module
- High performance TDC chips (AMT-2 or -3) developed for ATLAS experiment are used.
- 0.78ns / bit least count, 380 ps RMS time resolution
- 17 bit dynamic range (50 -100 μsec full scale, expandable)
- Common stop/start, continuous operation (or both before & after with regard to trigger)
- Rising and/or Falling edge timing or Rising and Width timing measurement.
- on-board DSP(TI C5402, 100 MHz)
- RS-232C Serial I/F
- Stable operation for temperature, voltage variation.
- differential input for signal(-2~+4.4V, $\Delta V > 100$ mV)
- NIM level start / stop/trigger signal input
- NIM level general purpose output.
- 1 MB Flash Memory.
- 128 kB Dual Port Memory.
- VME Slave module (A24/A32, D16/D32)
- VME Interrupt Generation.
- VME Block Transfer.
- Power Consumption ~9W (5V x 1.8 A).

2. Block Diagram

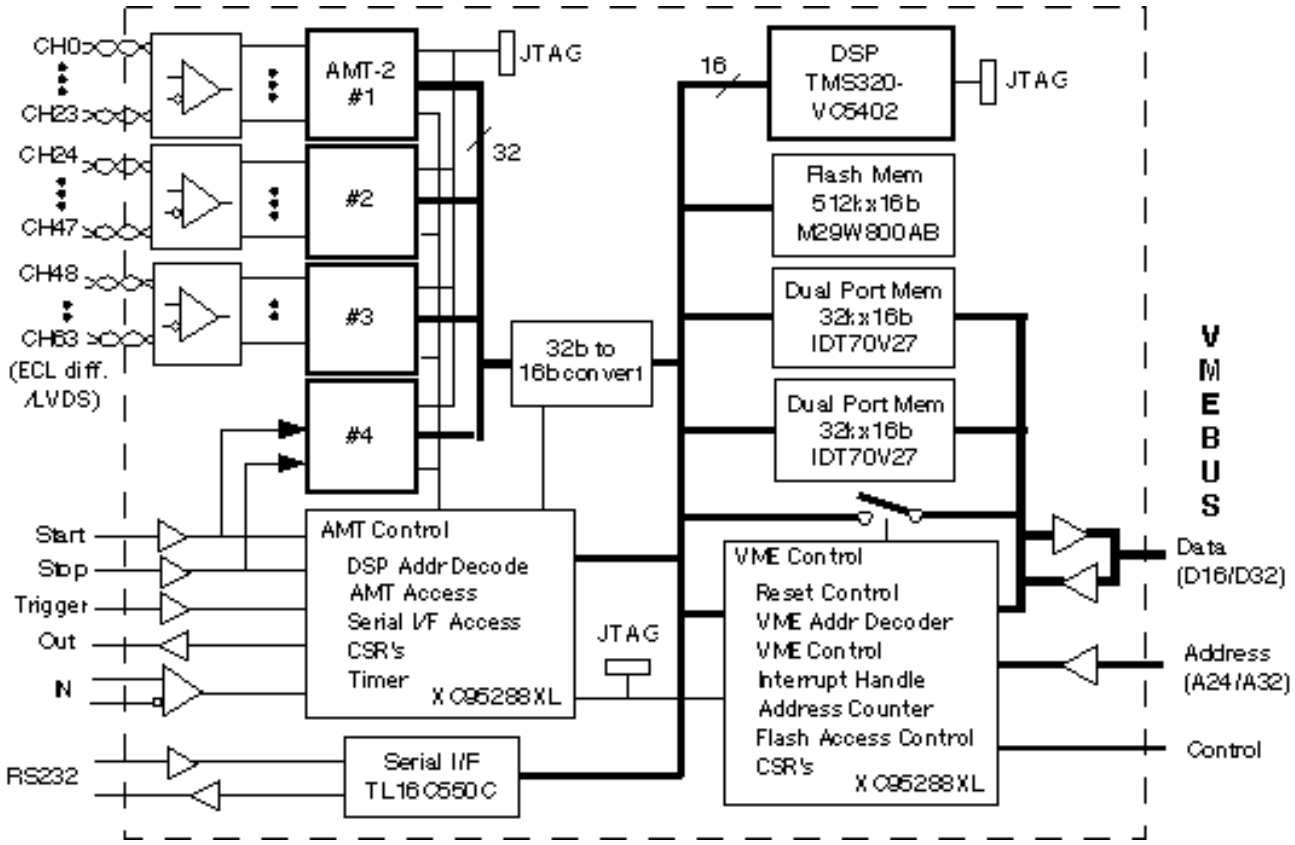


Fig. 1 Block diagram of the 64ch AMT-VME module.

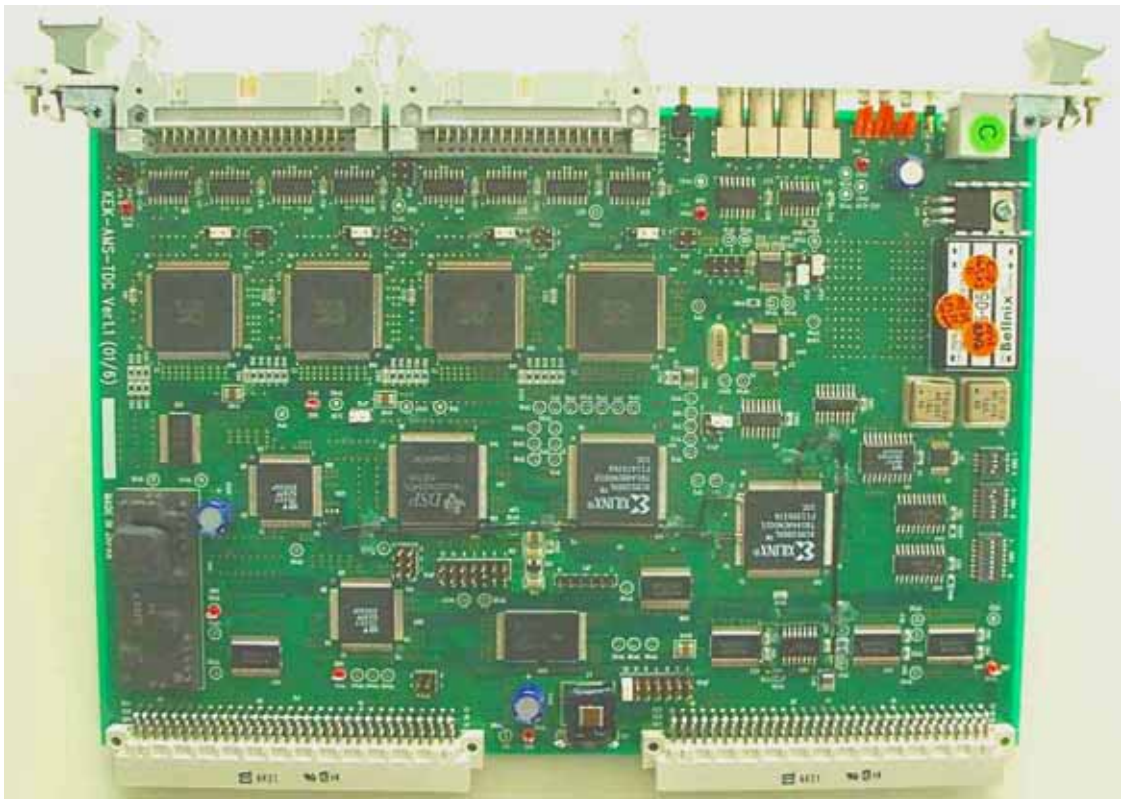
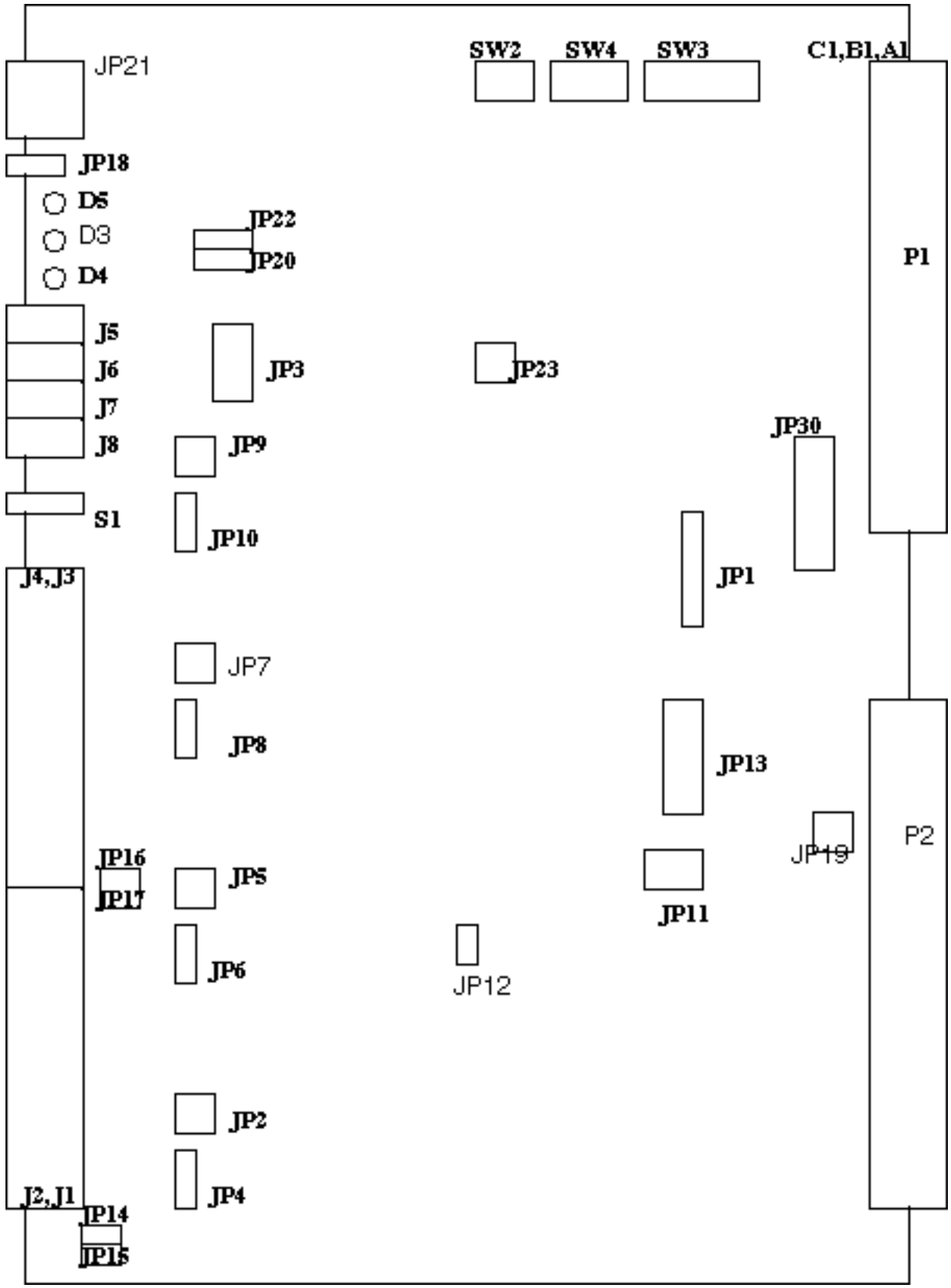


Fig. 2 Photograph of the module.

3. Specifications

Signal Inputs :	64 Channel. differential (amplitude > Δ100mV, common voltage range of -2 ~ +4.4V). Input Impedance 100 W. Four 34-pin Flat Cable Connectors.
START, STOP, TRIG Inputs :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level.
SYNC Output :	Lemo-type connector; NIM level. Used for test purpose.
Least Time Count :	0.78 ns/bit (@ 40 MHz system clock)
Time Range :	< 50 μsec (@ 40 MHz). Expandable to ....
Double Hit Resolution :	< 10 ns
Time Resolution :	Single Hit : σ = 270 ps , Time difference: σ = 380 ps
Integral Linearity Error :	< 0.5 LSB
Differential Linearity :	< 0.2 LSB
Serai Interface :	RS-232C (Front panel). RJ-11 connector.
VME I/F :	P1 connector. A16/A24/A32, D16/D32 (BLK). A16 Single word transfer(AM=$29,$2D), A24 Single word transfer(AM=$39, $3A, $3D, $3E), A32 Single word transfer(AM=$09, $0A, $0E, $0F), and A24 Block Transffer(AM=$3B,$3F) are supported. Interrupt from(to) the DSP to(from) a VME master.
DSP :	16 bit DSP (TI C5402) (@ 100 MHz)
Dual Port RAM :	16b x 64k.
Flash Memory :	16b x 512 k.
Packaging :	Double height (6U), Single width VME module.
Power Requirement :	+5 V x 1.8 A (9 W)

4. Module Settings



Connectors, jumpers etc. on the board.

4.1. Front Panel

JP18 Differential Input (reserved)

D5 DSP LED : lit on DSP running.
D3 VME LED : lit when accessed from VME master.
D4 AMT LED : lit on AMT running.

J5 START input LEMO Connecter (NIM level)
J6 STOP input LEMO Connecter (NIM Level)
J7 TRG input LEMO Connecter (NIM level, reserved)
J8 SYNC output LEMO Connecter (NIM level, reserved)

S1 External Reset : reset all circuit in the module.

J1, J2, J3, J4 : Input Connector Pin Assignment

J4 : Upper-Left Connector

Pin	Assignment	Pin	Assignment
1	GND(*)	2	GND(*)
3	Ch 48 +	4	Ch 48 -
5	Ch 49 +	6	Ch 49 -
7	Ch 50 +	8	Ch 50 -
9	Ch 51 +	10	Ch 51 -
11	Ch 52 +	12	Ch 52 -
13	Ch 53 +	14	Ch 53 -
15	Ch 54 +	16	Ch 54 -
17	Ch 55 +	18	Ch 55 -
19	Ch 56 +	20	Ch 56 -
21	Ch 57 +	22	Ch 57 -
23	Ch 58 +	24	Ch 58 -
25	Ch 59 +	26	Ch 59 -
27	Ch 60 +	28	Ch 60 -
29	Ch 61 +	30	Ch 61 -
31	Ch 62 +	32	Ch 62 -
33	Ch 63 +	34	Ch 63 -

J3 : Upper-Right Connector

Pin	Assignment	Pin	Assignment
1	GND(*)	2	GND(*)
3	Ch 32 +	4	Ch 32 -
5	Ch 33 +	6	Ch 33 -
7	Ch 34 +	8	Ch 34 -
9	Ch 35 +	10	Ch 35 -
11	Ch 36 +	12	Ch 36 -
13	Ch 37 +	14	Ch 37 -
15	Ch 38 +	16	Ch 38 -
17	Ch 39 +	18	Ch 39 -
19	Ch 40 +	20	Ch 40 -
21	Ch 41 +	22	Ch 41 -
23	Ch 42 +	24	Ch 42 -
25	Ch 43 +	26	Ch 43 -
27	Ch 44 +	28	Ch 44 -
29	Ch 45 +	30	Ch 45 -
31	Ch 46 +	32	Ch 46 -
33	Ch 47 +	34	Ch 47 -

J2 : Lower-Left Connector

Pin	Assignment	Pin	Assignment
1	GND(*)	2	GND(*)
3	Ch 16 +	4	Ch 16 -
5	Ch 17 +	6	Ch 17 -
7	Ch 18 +	8	Ch 18 -
9	Ch 19 +	10	Ch 19 -
11	Ch 20 +	12	Ch 20 -
13	Ch 21 +	14	Ch 21 -
15	Ch 22 +	16	Ch 22 -
17	Ch 23 +	18	Ch 23 -
19	Ch 24 +	20	Ch 24 -
21	Ch 25 +	22	Ch 25 -
23	Ch 26 +	24	Ch 26 -
25	Ch 27 +	26	Ch 27 -
27	Ch 28 +	28	Ch 28 -
29	Ch 29 +	30	Ch 29 -
31	Ch 30 +	32	Ch 30 -
33	Ch 31 +	34	Ch 31 -

J1 : Lower-Right Connector

Pin	Assignment	Pin	Assignment
1	GND(*)	2	GND(*)
3	Ch 0 +	4	Ch 0 -
5	Ch 1 +	6	Ch 1 -
7	Ch 2 +	8	Ch 2 -
9	Ch 3 +	10	Ch 3 -
11	Ch 4 +	12	Ch 4 -
13	Ch 5 +	14	Ch 5 -
15	Ch 6 +	16	Ch 6 -
17	Ch 7 +	18	Ch 7 -
19	Ch 8 +	20	Ch 8 -
21	Ch 9 +	22	Ch 9 -
23	Ch 10 +	24	Ch 10 -
25	Ch 11 +	26	Ch 11 -
27	Ch 12 +	28	Ch 12 -
29	Ch 13 +	30	Ch 13 -
31	Ch 14 +	32	Ch 14 -
33	Ch 15 +	34	Ch 15 -

(*) can be disconnected from GND by jumper pins.

4.2. Backplane Connector Pin Assignment

VME P1 connector

Pin	ROW A	ROW B	ROW C
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*(a)	D11
5	D04	BG0OUT*(a)	D12
6	D05	BG1IN*(b)	D13
7	D06	BG1OUT*(b)	D14
8	D07	BG2IN*(c)	D15
9	GND	BG2OUT*(c)	GND
10	SYSCLK	BG3IN*(d)	(SYSFAIL*)
11	GND	BG3OUT*(d)	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12 V)	(+5 V STDBY)	(+12 V)
32	+5 V	+5 V	+5 V

VME P2 connector

Pin	ROW A	ROW B	ROW C
1	-	+5V	-
2	-	GND	-
3	-	-	-
4	-	A24	-
5	-	A25	-
6	-	A26	-
7	-	A27	-
8	-	A28	-
9	-	A29	-
10	-	A30	-
11	-	A31	-
12	-	GND	-
13	-	+5V	-
14	-	D16	-
15	-	D17	-
16	-	D18	-
17	-	D19	-
18	-	D20	-
19	-	D21	-
20	-	D22	-
21	-	D23	-
22	-	GND	-
23	-	D24	-
24	-	D25	-
25	-	D26	-
26	-	D27	-
27	-	D28	-
28	-	D29	-
29	-	D30	-
30	-	D31	-
31	-	GND	-
32	-	+5V	-

( ) --- These signals are not used in this module.
(a, b, c, d) --- connected each pin respectively.

4.3. Jumper Switch Settings

[ ] -- default setting

SW2, SW3, SW4 VME Base Address

SW2	SW4					SW3								Comment
1	2	3	4	5	6	1	2	3	4	5	6	7	8	
OFF	X	X	X	X	X	A31	A30	A29	A28	A27	A26	A25	A24	A32 address mode
ON	A23	A22	A21	A20	A19	X	X	X	X	X	X	X	X	A24 address mode

A31-A19 : ON=0, OFF=1

JP30, SW2 : VME Bus IRQ Level Select

Select only 1 level for the VME IRQ level

IRQ Level	SW2 bit.2	bit.3	bit.4	JP30 short	
1	ON	ON	OFF	13-14	default
2	ON	OFF	ON	11-12	
3	ON	OFF	OFF	9-10	
4	OFF	ON	ON	7-8	
5	OFF	ON	OFF	5-6	
6	OFF	OFF	ON	3-4	
7	OFF	OFF	OFF	1-2	

JP13 : DSP JTAG Connection

Pin	Signal
1	TMS
3	TDI
5	+3.3V
7	TDO
9	TCK
11	TCK
13	EMU0

Pin	Signal
2	TRST*
4	GND
6	-
8	GND
10	GND
12	GND
14	EMU1

JP12 : Microprocessor/microcomputer mode select. [short]

If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 4K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/MC bit of the processor mode status (PMST) register can override the mode that is selected at reset.

Short / Open = 0 / 1

JP11 : DSP CLK Mode Select (short / open = 0 / 1)

Initial DSP Clock mode is selected with JP11 setting at reset. After the reset DSP program can change clock mode by modifying a register.

Clk mode	1-2	3-4	5-6	
Pll x 15	0	0	0	
Pll x 10	1	0	0	
Pll x 5	0	1	0	
Pll x 2	0	0	1	
Pll x 1	0	1	1	
1/2(pll disabled)	1	1	1	default
1/4(pll disabled)	1	0	1	

JP4, 6, 8, 10 : AMT ASD mode select [2-3]

1-2 short : ASD mode

2-3 short : parallel data output (default)

JP2, 5, 7, 9 : AMT serial data connectors (reserved)

pin 1	pin 2	pin 3	pin4
STROBEP	SERIOUTP	SERIOUTM	STROBEM

JP3 : AMT JTAG connector

Pin	Signal
1	TDI
2	TDO
3	TCK
4	+3.3V

Pin	Signal
8	GND
7	TMS
6	TRST*
5	GND

JP20, 21, 22 : Serial interface signal selection

	JP20	JP22	JP21 (Modular Jack)			
			1	2	3	4
Straight Cable	1-2	2-3	GND	TxOut	RxIn	GND
Cross Cable	2-3	1-2	GND	RxIn	TxOut	GND

(Default setting: 9600 baud, 8 bit, No parity, XON/XOFF control)

JP1 : U1 and U45 Xilinx CPLD ISP connector

Pin	Signal
1	+3.3V
2	GND
3	TCK
4	TDO
5	TDI
6	TMS

JP23 : DSP boot program select (short / open = 0 / 1) [Program No. 3]

Program in the selected location are copied to program space of $0200-$7FFF and executed after boot.

JP23		User	Program location		
2-3	1-4	Program No.	DSP address	*VME address*	
0	0	0	$18200～$1FFFF	$xxx30400~$xxx3FFFE	
0	1	1	$28200～$2FFFF	(not accessible)	
1	0	2	$38200～$3FFFF	(not accessible)	
1	1	3(AVrun)	$48200～$4FFFF	(not accessible)	default

JP19 : Dual Port RAM Master/Slave select

1-4	U35	
open	master	busy output (default)
short	slave	busy input

2-3	U37	
open	master	busy output (default)
short	slave	busy input

JP14,15,16,17 : Signal Input (J1,2,3,4) GND connection

a).JP14 short : J1-1,2 connected to GND

b).JP15 short : J2-1,2 connected to GND

c).JP16 short : J3-1,2 connected to GND

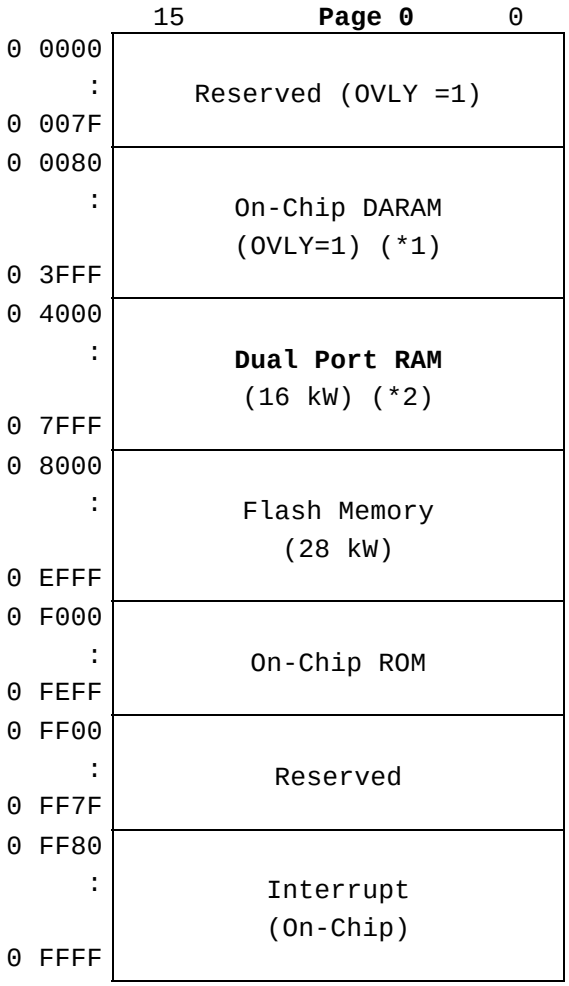
d).JP17 short : J4-1,2 connected to GND

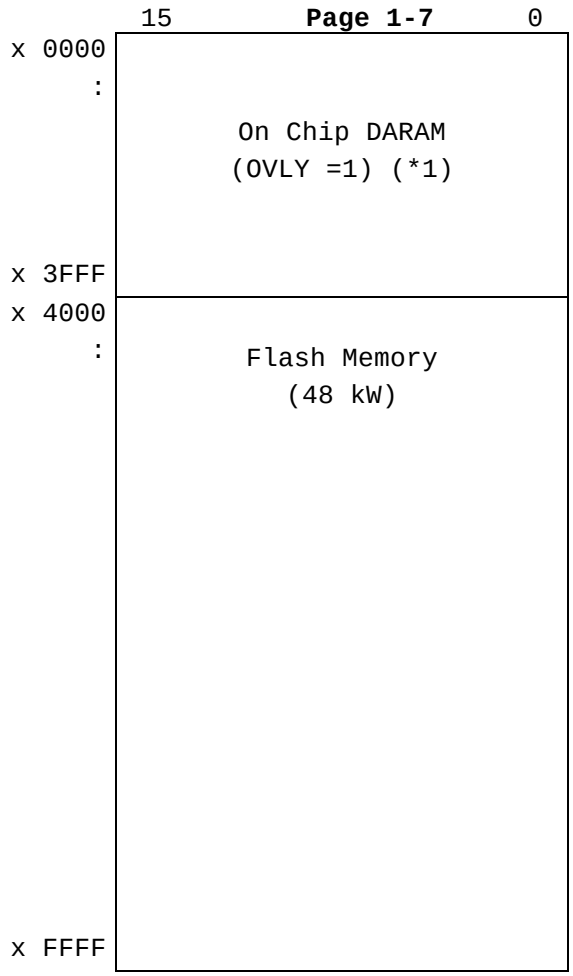
F1 : Fuse : 5V power, 10A fuse.

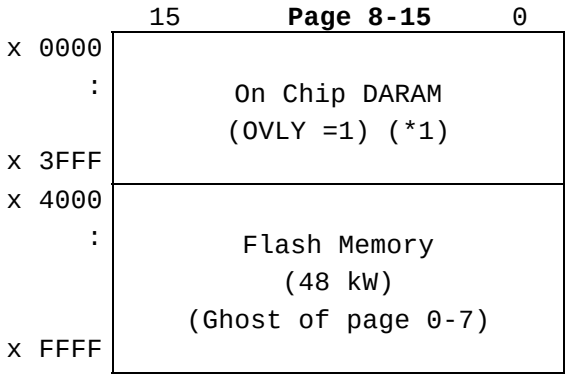
5. Address Map

5.1. DSP Space Address Map

Program Space (MP/MC*=0: Microcontroller Mode)

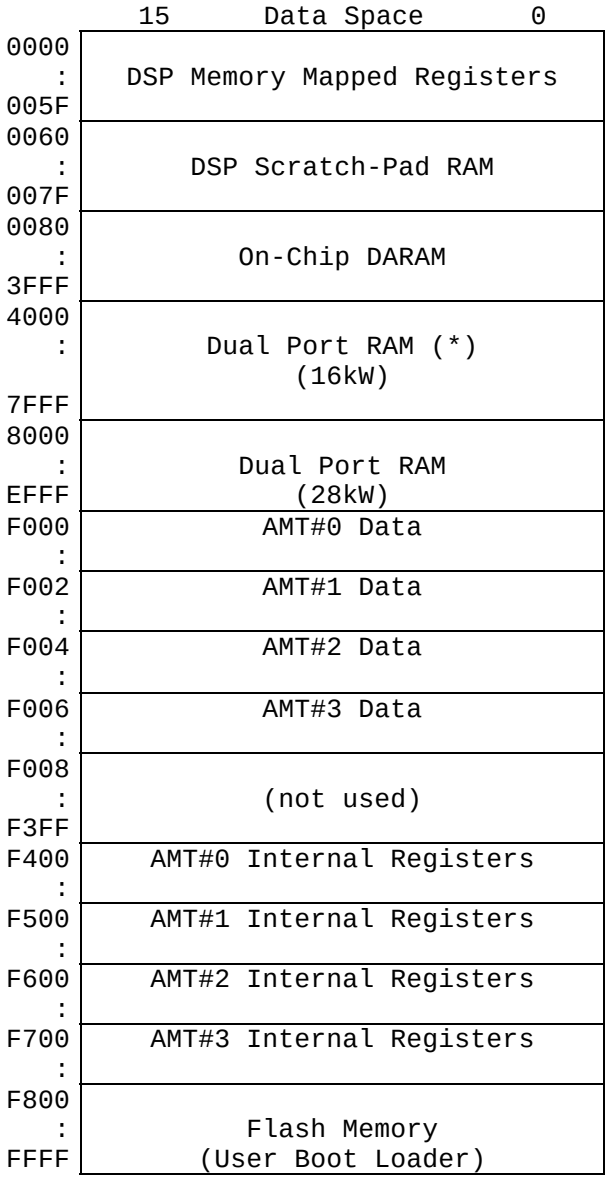






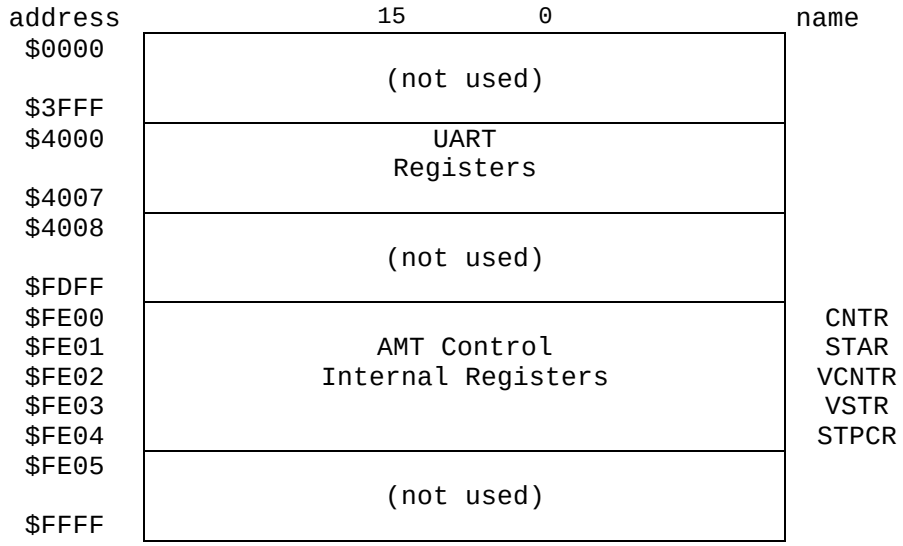
(*1) Same locations are mapped for all pages.
(*2) Same locations are shared with Data space.

Data Space



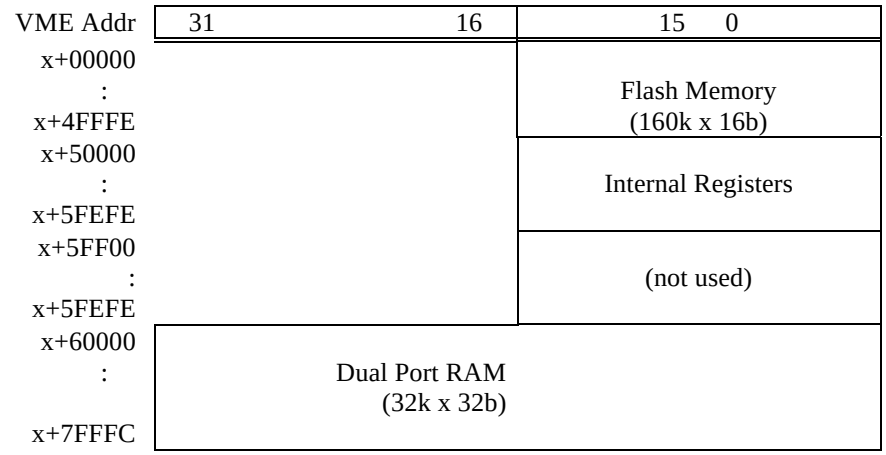
(*) Same location are mapped to Program Space

IO Space Address Map



5.2. VME Address Map

Single word transfer(AM=$29,$2D,$39..$3F), and Block Transffer (AM=$3E,$3F).



5.3. Flash Memory Address Map

512k x 16b, word access only.If accessed in byte or long word mode, time out error will occur.

Address	Flash Memory 15 0	Mapped Addr Prog Space	Mapped Addr Data Space	VME Addr
0 0000		-	-	x+00000
:	User Area	-	-	:
0 3FFF		-	-	:
0 4000		0 4000	4000	x+8000
:	User Area	:	:	:
0 7FFF		0 7FFF	7FFF	x+FFFE
:	User Area	-	-	:
0 F800		0 F800	F800	x+1F000
:	User Boot Loader	:	:	:
0 FFFF		0 FFFF	FFFF	x+1FFFE
:	User Area	-	-	:
1 4000		1 4000	-	:
:	User Area	:	-	:
1 81FF		1 81FF	-	:
1 8200		1 8200	-	:
:	1st User Prog	:	-	:
1 FFFF		1 FFFF	-	:
:	User Area	-	-	:
2 4000		2 4000	-	:
:	User Area	:	-	:
2 8000		:	-	x+50000
2 81FF		2 81FF	-	-
2 8200		2 8200	-	-
:	2nd User Prog	:	-	-
2 FFFF		2 FFFF	-	-
:	(not used)	-	-	-
3 4000		3 4000	-	-
:	User Area	:	-	-
3 81FF		3 81FF	-	-
3 8200		3 8200	-	-
:	3rd User Prog	:	-	-
3 FFFF		3 FFFF	-	-
:	(not used)	-	-	-
4 4000		4 4000	-	-
:	User Area	:	-	-
4 81FF		4 81FF	-	-
4 8200		4 8200	-	-
:	4th User Prog	:	-	-
4 FFFF	(AVrun)	4 FFFF	-	-
:	(not used)	-	-	-
5-7 4000		5-7 4000	-	-
:	User Area	:	-	-
5-7 FFFF		5-7 FFFF	-	-

(-) not accessible

5.4. Module Internal Register Address Map

DSP IO	VME Addr	name	bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE00	-	CNTR	Control Register															
FE01	-	STAR	Status Register															
	5FF00	VECR	0	0	0	0	0	0	0	0	Interrupt Vector							
	5FF02	VCNTR	0	0	0	0	0	0	0	0	FWE	HE	RE	VEN	HOLD	IRQ	IEN	BRST
FE02			0	0	0	0	0	0	0	0	-	-	-	-	HOLD	IRQ	IEN	BRST
FE03	5FF04	VSTR	0	0	0	0	0	0	0	0	0	0	0	0	IRQ	VEN	RST	HACK
	5FF06	ADCNTR	0	0	0	0	0	0	0	0	Start Address							
	5FF08	DCNTR	0	0	0	0	0	0	0	0	Data Size							
FE04	-	STPCR	Measurement Timer															

• Control Register (CNTR) (R/W)

bit 15	DSP control	enable／disable ＝ 1／0
bit 14	ENCNT enable	enable／disable ＝ 1／0
bit 13	(not use)	
bit 12	(not use)	
bit 11	INT0 enable	enable／disable ＝ 1／0
bit 10	(not use)	
bit 9	INT1 enable	enable／disable ＝ 1／0
bit 8	100us output enable	enable／disable ＝ 1／0
bit 7	Measurement Mode	COMSTOP/COMSTART ＝ 1／0
bit 6	Start Measurement	START／STOP ＝ 1／0
bit 5	Trigger mode	TRG／normal ＝ 1／0 [1] (not used now)
bit 4	CLKO enable	enable／disable ＝ 1／0
bit 3	BUNCHRST	enable／disable ＝ 1／0 Output pulse of 25ns width, then automatically cleared. Status is kept in STAR[9].
bit 2	EVENTRST	enable／disable ＝ 1／0 Output pulse of 25ns width, then automatically cleared. Status is kept in STAR[8].
bit 1	UART RST	enable／disable ＝ 1／0 Output pulse of 25ns width, then automatically cleared.
bit 0	AMTRESET	enable／disable ＝ 1／0 Output pulse of 25ns width, then automatically cleared. Status is kept in STAR[7].

 Status Register(STAR). (Read only)

bit 15	Measurement mode	START/STOP = 1 / 0
bit 14	External stop status	hit/not hit = 1 / 0 cleared after read
bit 13	External start status	hit/not hit = 1 / 0 cleared after read
bit 12	External trg status	hit/not hit = 1 / 0 cleared after read
bit 11	JP231-4 status	
bit 10	JP23 2-3 status	
bit 9	BUNCHRESET status	reset/not reset = 1 / 0 cleared after read
bit 8	EVENTRESET status	reset/not reset = 1 / 0 cleared after read
bit 7	AMTRESET status	reset/not reset = 1 / 0 cleared after read
bit 6	AMT1 Error	ERR/not ERR = 1 / 0 cleared after read
bit 5	DSP LED	ON/OFF = 1 / 0
bit 4	AMT LED	ON/OFF = 1 / 0
bit 3	AMT1_3 data HIT	HIT/Empty = 1/0
bit 2	AMT1_2 data HIT	HIT/Empty = 1/0
bit 1	AMT1_1 dataHIT	HIT/Empty = 1/0
bit 0	AMT1_0 data HIT	HIT/Empty = 1/0

• Vector register(VECR) R/W

Vector code for interrupt

• VME control Register(VCNTR) R/W

FWE	bit7: Flash access enable	enable/ disable = 1 / 0
HE	bit6: HOLD enable	enable/ disable = 1 / 0
RE	bit5: Board reset enable	enable/ disable = 1 / 0
VEN	bit4: VME action	enable/ disable = 1 / 0
HOLD	bit3: DSP HOLD	enable/ disable = 1 / 0
IRQ	bit2: Interrupt enable	enable/ disable = 1 / 0
IEN	bit1: Interrupt signal from DSP to VME	enable/ disable = 1 / 0
	Not automatically disabled. Please clear after IACK disable	
BRST	bit0: Board Reset	enable/ disable = 1 / 0
	Not automatically disabled. Please write 0 after reset.	

• VME Status Register(VSTR) Read only

bit3: Interrupt status	generated/none = 1 / 0 (cleared after read)
bit2: VME action status	on/off= 1 / 0, VME LED staus
bit1: board reset status	reset/not reset = 1 / 0 (cleared after read)
bit0: DSP HOLD acknowledge	hold/not hold = 1 / 0

• STOP Counter Register(STPCR) R/W

12bit Counter, measurement time 0ns-50us, resolution 25ns

5.5. Dual Port Memory Address Map

32k x 32 b, word or long word access.

DPM Addr	31 . . . 0	Prog Sp.	Data Sp.	VME Addr	
0				x+60000	
:	User Area			:	
0 3FFF				x+67FFC	
0 4000		0 4000	4000	x+68000	
:	Program Area	:	:	:	
0 7FFF		0 7FFF	:	x+6FFFC	
0 8000			:	x+70000	
:	User Area		:	:	
0 8F7F			:	:	
0 8F80			:	X+7DF00	DPtop
:	Module Control Parameters		:	:	
0 8FFF			:	:	
0 9000			:	:	
:	Data Buffer		:	:	
0 EFFF			EFFF	x+7DFFC	
0 F000				x+7E000	
:	User Area			:	
1 FFFF				x+7FFFC	

X :Base Address

A32 mode : x = $0000 0000 - $FF00 0000 (upper 8 bit base address is switch selectable)

A24 mode : x = $00 0000 - $F8 0000 (upper 5 bit base address is switch selectable)

5.5.1. Module Control Parameters

DSP Addr	VME add	Contents 31 . . . 16 15 . . . 0	Direction
$8F80	DPtop	(*1) / Pcount （Parameter counter:16bit）	VME =>
$ 8F82	+$0004	Run Status	
$ 8F84	+$0008	0 / Time range count (dcount 12bit) (Rec time = 25ns x dcount)	
$ 8F86	+$000C	0 / Module ID (5bit)	
$ 8F88	+$0010	CH_Enable(#31(MSB)－#0(LSB))	
$ 8F8A	+$0014	CH_Enable(#63(MSB)－#32(LSB))	
$ 8F8C	+$0016	NPAT: # of partitions (12bit)	
$ 8F8E	+$0018	Icount (Input counter: 16bit)	
$ 8F90	+$0020	(*2) / Mask Window (12 bit)	
$ 8F92	+$0024	(*2) / Search Window (12 bit)	
$ 8F94	+$0028	(*2) / Match Window (12 bit)	
$ 8F96	+$002C	(*2) / Reject Count Offset (12 bit)	
$ 8F98	+$0030	(*2) / Event Count Offset (12 bit)	
$ 8F9A	+$0034	(*2) / Bunch Count Offset (12 bit)	
$ 8F9C	+$0038	(*2) / Coarse Count Offset (12 bit)	
$ 8F9E	+$003C	(*2) / Count Roll Over (12 bit)	
$8FA0	+$0040	Offset ch#0 16bit signed / Offset ch#1 16bit signed	VME=>
$8FA2	+$0044	Offset ch#2 16bit signed / Offset ch#3 16bit signed	VME=>
:	:	(*1) : / :	:
$8FDE	+$00BC	Offset ch#62 16bit signed / Offset ch#63 16bit signed	VME=>
$8FE0	+$00C0	(reserved)	
$ 8FF0	+$00E0	EchoPcount （16bit Copy of Parameter counter）	<= AMT
$ 8FF2	+$00E4	AMT Status 0: wait 1: running 2: end -1: error	<= AMT
$ 8FF4	+$00E8	Scount (Save counter: 16bit)	<= AMT
$8FF6	+$00EC	Continuous Mode Control	
:	:	:	
$8FFE	+$00FC	(reserved)	

Dptop = VME_BASE + $7DF00
*1) When serial I/F is host, DSP also can write.
*2) 2004.10 added

PCOUNT

Increment 1 when new parameters are written to the module control parameter are to reflect the parameters to next measurement.

Run Status ([]---initial value)

Bit0: (reserved)[0]
Bit1: start measurement [0]
Bit2: Common start/stop (=0 start, =1:stop mode) [1]
Bit3－4: Edge detection(dedge) [0]
=0 rising
=1 rising and falling
=2 falling
=3 rising and width
Bit5－6: Subtract offset(dsuboff) [0]
=0 don't subtract
=2 subtract offset
Bit7: measurement control(obsolete) [1]
=0 TRG, =1 Nomal
Bit8：EXTRG mode (2004.10 added) [0]

=0 EXTRG mode disable
=1 EXTRG mode enable
Bit 9-27: (reserved)[0]
Bit28－30: width_select(0～7) [0]

Offset table

When RunStatus[6:5]=2 is selected, these offset values are subtracted from measured data for each channel. Initial value of the offset equals 0.

Continuous Mode Control

Bit 0-15 : DSIZE. Remaining data size in the data buffer (written by DSP) [0]
Bit 16 : FULL. Full flag of the data buffer. [0]
Bit 17 : EMPTY. Empty flag of the data buffer. [1]
Bit 18 : OVR. Overflow flag of the data buffer. [0]
Bit 19-21 : RCOUNT. Incremented when this register is renewed. [0]
Bit 22-30 : (reserved)
Bit 31 : FOEV. Data measurement range. [0]
FOEV=0: less than 12.8ms 。
FOEV=1: more than 12.8ms (see section XX)

5.5.2. Data buffer

Data buffer is divided into N blocks (partitions) as shown below. The number N is defined in NPAT of the Module Control Parameter. Handshake of the Read/Write control of the data block is done using Scount and Icount register.

DSP addr	VME addr	31 . . . 0
$ 9000	Dptop +$0100	Data Block(0)
		Data Block(1)
		:
		Data Block(N-1)
$EFFF	$BFFC	

Each Data Block has format show below.

VME addr	31 . . . 0
+0	Recording data Status
+4	Common start/stop time
+8	Hit data #0
:	:
+4m+8	Hit data #m
	Error Report (if exists)
	End of data

Contents in the data block are shown below.

Recording data Status

D31			D28												D16
1	0	1	Total # of recording data (tntotal) (include header & footer unit:DWord)												

D15															D0
Event #															

Common start/stop time

D31			D28				D24	D23	D22－D20	D19－D18	D17	D16
1	1	0	Module ID					0	Width_select	Edge detection	MC (*1)	Common start/stop time

D15																D0
Common start/stop time (17bit)																

(*1)・・・・measurement control

Hit data

D31			D28			D25					D20	D19			D16
0	0	0	F/R			CH#(6bit 0-63)						HIT time data			

F/R: Edge direction Falling (=1)/Rising (=0)

D15																D0
HIT time data (20bit offset from common start/stop timing)																

Error Report

D31			D28				D24							D17	D16
0	1	1	Module ID					Unused						OVR	ERR

D15		D13													D0
AMT#	AMT Error Flag (Refer AMT1&2 User's Manual § 2.10)														

End of data

D31															D16
End of data ($5555)															

D15															D0
Event #															

5.6. AMT CSR Registers

See AMT User's Manual (http://atlas.kek.jp/tdc/) for detailed explanation.

Table. 1. Bit assignment of the control registers.

	BIT											
	11	10	9	8	7	6	5	4	3	2	1	0
CSR0	global_reset (0) {11}	error_reset (0) {10}	disable_encode (0) {9}	enable_errrst_bcrevr (0) {8}	test_mode (0) {7}	test_invert (0) {6}	enable_direct (0) {5}	disable_ringosc (0) {4}	clkout_mode (0) {3:2}		pll_multi (0) {1:0}	
CSR1	mask_window (0) {23:12}											
CSR2	search_window (0) {35:24}											
CSR3	match_window (0) {47:36}											
CSR4	reject_count_offset (0) {59:48}											
CSR5	event_count_offset (0) {71:60}											
CSR6	bunch_count_offset (0) {83:72}											
CSR7	coarse_time_offset (0) {95:84}											
CSR8	count_roll_over (FFF) {107:96}											
CSR9	strobe_select (1/0) {119:118}		readout_speed (0) {117:116}		width_select (0) {:115:113}			error_test (0) {112}	tdc_id (0) {111:108}			
CSR10	enable_auto_reject (1) {131}	enable_l1occup_readout (0) {130}	enable_match (1) {129}	enable_mask (0) {128}	enable_relative (0) {127}	enable_serial (0) {126}	enable_header (0) {125}	enable_trailer (0) {124}	enable_rejected (0) {123}	enable_pair (0) {122}	enable_trailing (0) {121}	enable_leading (1) {120}
CSR11	enable_rofull_reject (0) {143}	enable_l1full_reject (0) {142}	enable_trfull_reject (0) {141}	enable_errmark (0) {140}	inclk_boost (0) {139}	enable_ermark_rejected (0) {138}	enable_errmark_ovr (0) {137}	enable_l1ovr_detect (0) {136}	enable_mreset_code (0) {135}	enable_resetcb_sepa (0) {134}	enable_mreset_evrst (0) {133}	enable_setcount_bcrst (0) {132}
CSR12	enable_sepa_readout (0) {155}	enable_sepa_bcrst (0) {154}	enable_sepa_evrst (0) {153}	enable_error [8:0] (1FF) {152:144}								
CSR13	enable_channel[11:0] (FFF) {167:156}											
CSR14	enable_channel[23:12] (FFF) {179:168}											
CSR15	general_out[11:0] (0)											

() -- initial value at reset. {} – JTAG bit No.

Table. 2. Bit assignment of the status registers (all these registers are read only).

	11	10	9	8	7	6	5	4	3	2	1	0
CSR16	rfifo_ empty (1) {11}	rfifo_ full (0) {10}	control_ parity (1) {9}	error_ flags (0) {8:0}								
CSR17	l1_ empty (1) {23}	l1_ nearly_ full (0) {22}	l1_ over_ recover (1) {21}	l1_ over flow (0) {20}	l1_ write_address (0) {19:12}							
CSR18	tfifo_ empty (1) {35}	tfifo_ nearly_ full (0) {34}	tfifo_ full (0) {33}	running (0) {32}	l1_ read_address (0) {31:24}							
CSR19	coarse_ counter [0] (0) {47}	tfifo_ occupancy (0) {46:44}			l1_ start_address (0) {43:36}							
CSR20	coarse_counter[12:1] (0) {59:48}											
CSR21	general_ in[3:0] (DIO27~24) {71:68}				0 (0) {67}	0 (0) {66}	rfifo_ occupancy[5:0} (0) {65:60}					

() -- initial value at reset. {} --- JTAG bit No.

5.7. UART Registers

See TL16C550C data sheet of Texas Instruments (http://www.ti.com) for detailed explanation.

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location

6. Boot Procedure

Operation	Relevant Part
Reset Release	
Execute from $FF80 of the on-chip-ROM	DSP ROM
Branch to Boot Loader ($F800 - $FBFF)	DSP ROM
Set up the CPU status registers before initiating the bootload. Interrupts are globally disabled (INTM = 1) and internal dual-access and single-access RAMs are mapped into program/data space (OVLY = 1). Seven wait states are initialized for all the program and data spaces. The size of the external memory bank is set to 4K words.	
Read BRS(Boot Routine Selection) from IO address $FFFF	DSP ROM
BRS=$4000 (16bit parallel EPROM mode, Sorce address(SRC)=$4000)	CPLD
Read $4000 (=$10AA)	Flash Memory
Go to 16-bit Boot Mode	Flash Memory
Read $4001 and set to SWWSR ($7FFF)	Flash Memory
Read $4002 and set to BSCR ($F800)	Flash Memory
Read $4003 and set XPC value of entry point ($0000)	Flash Memory
Read $4004 and set the entry point	Flash Memory
Read $4005 and set the size of the section ($0741)	Flash Memory
Read $4006 and set XPC value of destination address ($0000)	Flash Memory
Read $4007 and set to destination address	Flash Memory
Copy $4008 - $4xxx to the destination address	Flash Memory
Go to the entry point ($????)	Program Space

* 'hex500 hex.cmd' command make above format from assembler object.