TMC Test Module 3 (TTM3) Manual

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1.Introduction

TTM3 module was developed for testing custom LSI's. By changing a sub-board, which is attached in front of a main-board, many kind of LSI's can be mounted. It is a very simple module which has only 1 CPLD, several buffers and a VME interface, but has much of flexibility. Some of the CPLD (ALTERA EP20K300E) pins can interface to both single end and LVDS differential signals.

The CPLD configuration can be selected from 2 flash memory sets and internal RAM.

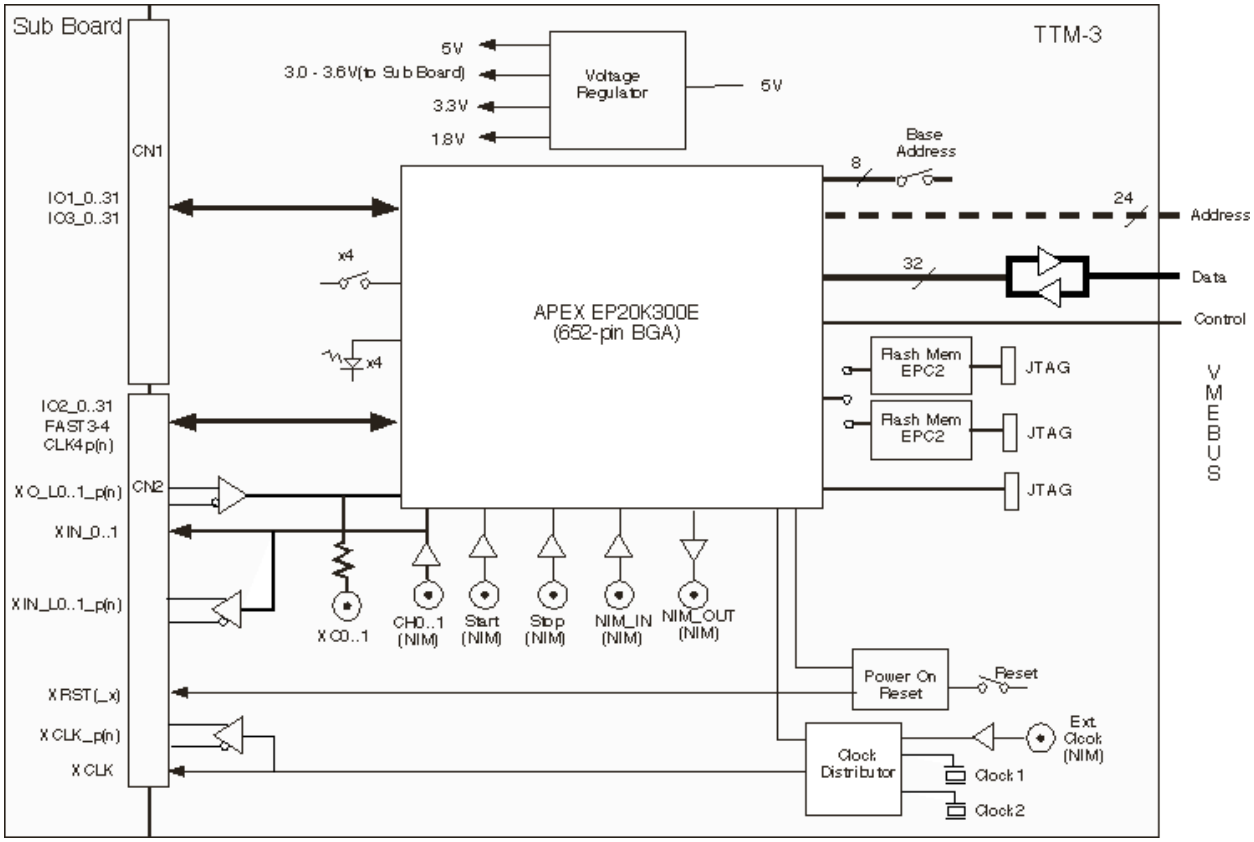


Fig. 1 TTM3 Board Block Diagram

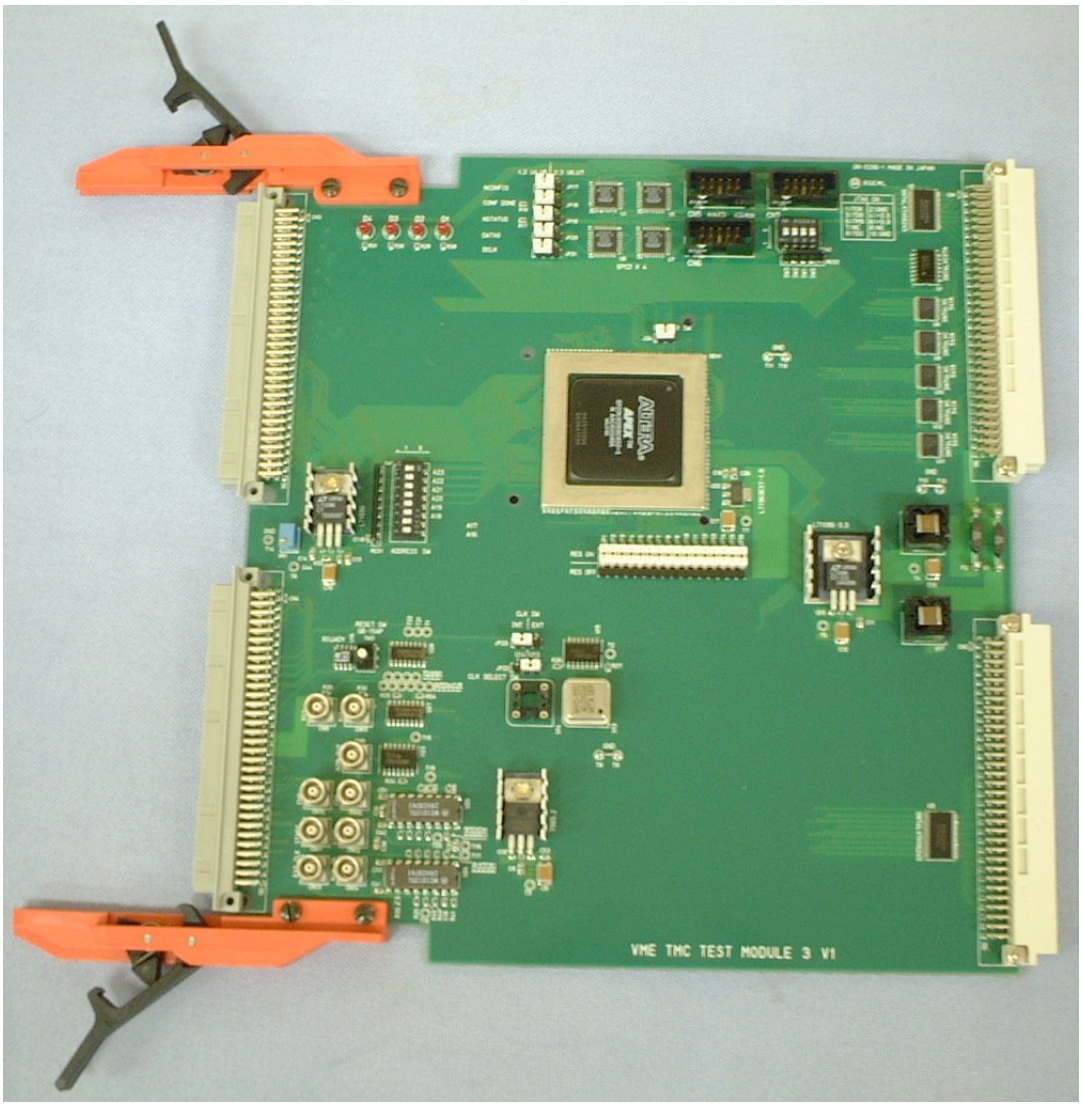


Fig. 1 Photograph of the TTM3 Main Board.

Table. 1 TTM-3 基本仕様

FPGA	ALTERA　APEXEP20K300E EP20K300E　(652-PIN　BGA)
FPGA へのダウンロード方法	JTAG
入力クロック	内部クロック　(40MHz　x2) 外部クロック　(NIM 入力)
VME バス	データバス 32bit(標準転送) アドレスバス 24bit(標準転送)
VME コネクタ	J1, J2
サブボードコネクタ	DIN 32pins x 3 rows x 2
NIM 入力	LEMO connectors x6 START、STOP、NIM_IN EXT_CLK、CH0、CH1
NIM 出力	LEMO 型コネクタ　x3 NIM_OUT、XO0、XO1
コンフィギュレーション デバイス	ALTERA 社　フラッシュメモリ EPC2 x4
LVDS ドライバ	TEXAS INSTRUMENTS 社　SN65LVDS31
LVDS レシーバ	TEXAS INSTRUMENTS 社　SN65LVDS32
LED	汎用 LED　x4
スイッチ	スタンディング ON-OFF 切り替えスイッチ　x5
Power	+5.0 V x ? A

·APEX EP20K300E

・652 ピン　BGA

・Multi Volt インターフェイス。

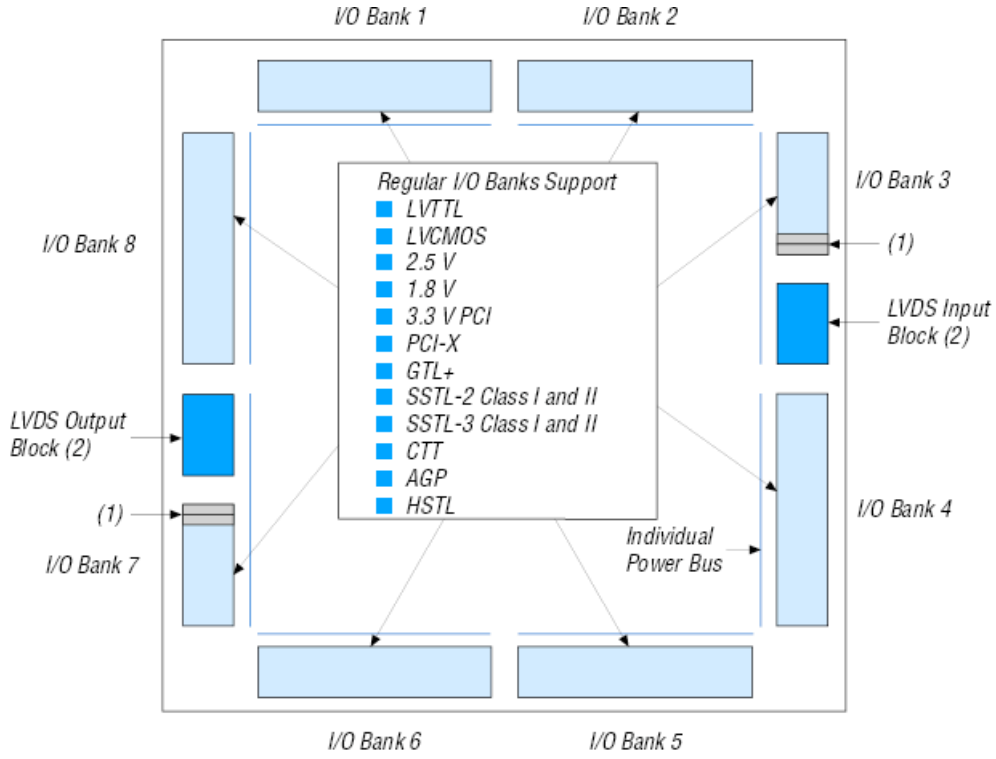
・最大 73 万ゲート

・125MHz のシステムパフォーマンス

・デュアルポートエンベデット RAM 標準装備

・広帯域 True-LVDS のサポート。

・4 個の PLL(Phase-Locked Loops)を内臓。それにより ClockLock,ClockBoost,ClockShift の各回路が提供される。ClockLock 回路はデバイス内のクロックのスキューと遅延を減少させる。ClockBoost 回路はクロック周波数の乗算機能を提供していて、ボード上に低速クロックを分配してデバイス内で周波数を逓倍して使用することが可能である。ClockShift 回路はプログラマブルにクロックの遅延と位相シフトを調整できる機能を提供している。



APEX 20KE I/O Blocks

Note:

(1) The first two I/O pins that border the LVDS blocks can only be used for input to maintain an acceptable noise level on the V_{CCIO} supply.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Fig. 2

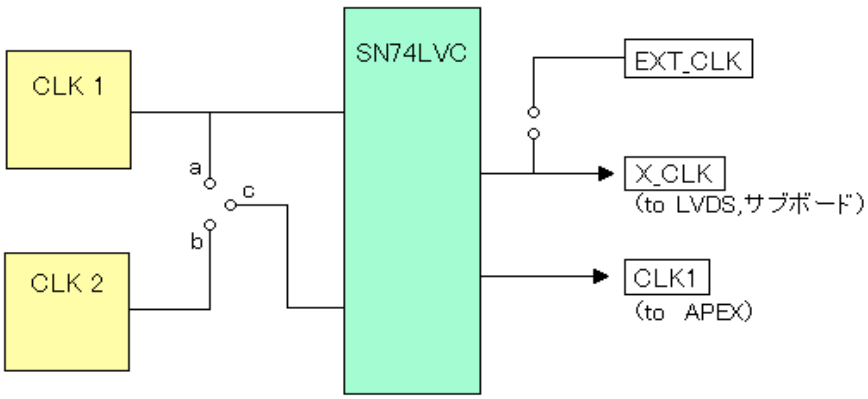


Fig. 3

2.VME Address Map

[General Map] ([A23:A16] = Base Address, AM = 39, 3A, 3D or 3E)

Address	31 0
0000 : FEFC	sub-board internal address
FF00 : FF10 : FFFC	MCSR0 : TCSR0 : :

3.Main Board Control & Status Registers

[MCSR0]

bit	Read/Write	Name	Comment
0	R/W	TMCRESET	TMC chip reset
1	R/W	-	
2	R/W	-	
3	R/W	-	
4	R/W	-	
5	R/W	ALL RESET	All reset
6	R/W	VSTART	Start TMC recording
7	R/W	VSTOP	Stop TMC recording
8	R/W	EXTDIN_0	
9	R/W	EXTDIN_1	
10	R/W	-	
11	R/W	-	
12	R/W	-	
13	R/W	-	
14	R/W	-	
15	R/W	-	
16	R	parity_error	Serial In parity error
17	R	full	Serial In FIFO full
18	R	empty	Serial In FIFO empty
19..31			

[MCSR1]

	31	30	29 . . . 0
R/W	0	0	<-- Encoded Signal (3 bit x 10 set) <--

[MCSR2]

	31 . . . 0
R	Serial In FIFO (256 words)

4. Sub Board Signal Registers

4.1.TMC-PHX1

[TMC-PHX1 sub-board map]

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000	TMC CSR0	R/W
0002	TMC CSR1	R/W
0004	TMC CSR2	R/W
0006	TMC CSR3	R/W
0008	TMC CSR4	R/W
000A	TMC CSR5	R/W
000C	TMC CSR6	R/W
000E	TMC CSR7	R/W
0010 : FEFE	not used	

[TMC-PHX1 TCSR0]

TCSR0[31:15]	TCSR0 [15:0]
-	IO2_[15:0] (XIO[15:0])

bit	Read/Write	Name	Comment
0	R/W	OCLK	TMC data Output Clock
1	R/W	TRIG	TMC Trigger signal
2	R/W	-	
3	R/W	CSTART	Comm Start(=1)/Comm Stop(=0) mode
4	R/W	WSTART	TMC WSTART signal
5	R/W	SYNCMOD	Sync(=1)/Async(=0) readout mode
6	R/W	RE	TMC data Read Enable
7	R/W	OE	TMC data Output Enable
8	R	EMPFLG	TMC data Empty Flag
9	R	EVEND	TMC data Event End Flag
10	R	DVALID	TMC data Valid signal
11	R	ERR	TMC Error Flag
12	R/W	DCH0	TMC data read channel 0
13	R/W	DCH1	TMC data read channel 1
14	R/W	RPUP	TMC Read Pointer Up
15	R/W	-	

4.2.AMT-TEG1

[AMT-TEG1 sub-board map]

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000	TMC CSR0	R/W
0002	TMC CSR1	R/W
0004	TMC CSR2	R/W
0006	TMC CSR3	R/W
0008	TMC CSR4	R/W
000A	TMC CSR5	R/W
000C	TMC CSR6	R/W
000E	TMC CSR7	R/W
0010 : FEFE	not used	

[AMT-TEG1 TCSR0]

bit	Read/Write	Name	Comment
0	R/W	L1BRCLK	L1B Read Clock
1	R/W	LOADFIFO	
2	R/W	ENOUT	Enable Output
3	R/W	-	
4	R/W	-	
5	R/W	-	
6	R/W	-	
7	R/W	-	
8	R	L1BEMPTY	L1B Empty Flag
9	R	L1BFULL	L1B Full Flag
10	R	ERROR	Error
11	R	-	
12	R/W	-	
13	R/W	-	
14	R/W	-	
15	R/W	-	

[AMT-TEG1 TCSR1]

bit	Read/Write	Name	Comment
0	R	-	
1	R	-	
2	R	ENOUT	Enable Output(=TCSR0_2)
3	R	-	
4	R	-	
5	R	-	
6	R	-	
7	R	VME_WRITE*	
8	R	WR*	
9	R	CS*	
10	R	-	
11	R	-	
12	R	-	
13	R	-	
14	R	0	
15	R	0	

[AMT-TEG1 TCSR2]

15 ..0	
DIO15 .. 0	R/W

* Caution : These signals are 5V device output!

[AMT-TEG1 TCSR3]

15 ..0	
DIO31 .. 16	R/W

* Caution : These signals are 5V device output!

4.3.AMT-1

[AMT-1 sub-board map]

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000	TMC CSR0	R/W
0002	TMC CSR1	R/W
:	:	:
001C	TMC CSR14	R/W
001E	(TMC CSR15)	R/W
0020	TMC CSR16	R
:	:	:
002A	TMC CSR21	R
002C : 003E	not used	
0040	DSPACE[15:0]	R
0042	DSPACE[31:16]	R
0044 : FEFE	not used	

Caution!: Remove FIFO1(U15) and Level Converters (U1 and U10) when AMT-1 sub board is used.

[AMT-1 TCSR0]

bit	Read/Write	Name	Comment
0	R/W	TRIG	
1	R/W	EVENTRST	
2	R/W	BUNCHRST	
3	R/W	START	
4	R/W	GETDATA	
5	R/W	-	
6	R/W	-	
7	R/W	-	
8	R	DREADY	
9	R	CLKOUT	
10	R	ERROR	
11	R	TDO	
12	R/W	TRSTB	
13	R/W	TDI	
14	R/W	TMS	
15	R/W	TCK	

4.4.AMT-2&3

[AMT-2&3 sub-board map]

Address	31 . . . 16	15 0	Read/Write
0000	not used	TMC CSR0	R/W
0002	not used	TMC CSR1	R/W
0004	not used	TMC CSR2	R/W
0006	not used	TMC CSR3	R/W
0008	not used	TMC CSR4	R/W
000A	not used	TMC CSR5	R/W
000C	not used	TMC CSR6	R/W
000E	not used	TMC CSR7	R/W
0010	not used	TMC CSR8	R/W
0012	not used	TMC CSR9	R/W
0014	not used	TMC CSR10	R/W
0016	not used	TMC CSR11	R/W
0018	not used	TMC CSR12	R/W
001A	not used	TMC CSR13	R/W
001C	not used	TMC CSR14	R/W
001E	not used	TMC CSR15	R/W
0020	not used	TMC CSR16	R
0022	not used	TMC CSR17	R
0024	not used	TMC CSR18	R
0026	not used	TMC CSR19	R
0028	not used	TMC CSR20	R
002A	not used	TMC CSR21	R
002C : 003E		not used	
0040 0044 : FEFE	DSPACE[31:16]	DSPACE[15:0] : not used :	R/W

[AMT-2&3 TCSR0]

bit	Read/Write	Name	Comment
0	R/W	TRIG	
1	R/W	EVENTRSTB	
2	R/W	BUNCHRSTB	
3	R/W	START	
4	R/W	GETDATA	
5	R/W	ASDMOD	
6	R/W	TEST1	proton irradiation
7	R/W	ENCLK	proton irradiation
8	R	DREADY	
9	R	CLKOUT	
10	R	ERROR	
11	R	TDO	
12	R/W	TRST	
13	R/W	TDI	
14	R/W	TMS	
15	R/W	TCK	

4.5.TMC-X1

[TMC-X1 sub-board map]

Address	31 . . . 16	23 . . . 16	15 0	Read/Write
0000	0		FT15..FT0	R
0004	0	SFT23..SFT0		R
0008 : FEFE	not used : not used			

[TMC-X1 TCSR0]

bit	Read/Write	Name	Comment
0	R/W	SDIN	
1	R/W	SCLK	
2	R/W	SRST	
3	R	SDOUT	
4	R/W	ERST	
5	R/W	RST	
6	R		
7	R		
8	R		
9	R		
10	R		
11	R		
12	R		
13	R		
14	R		
15	R		

5.Board Layout

5.1.TTM3 main board

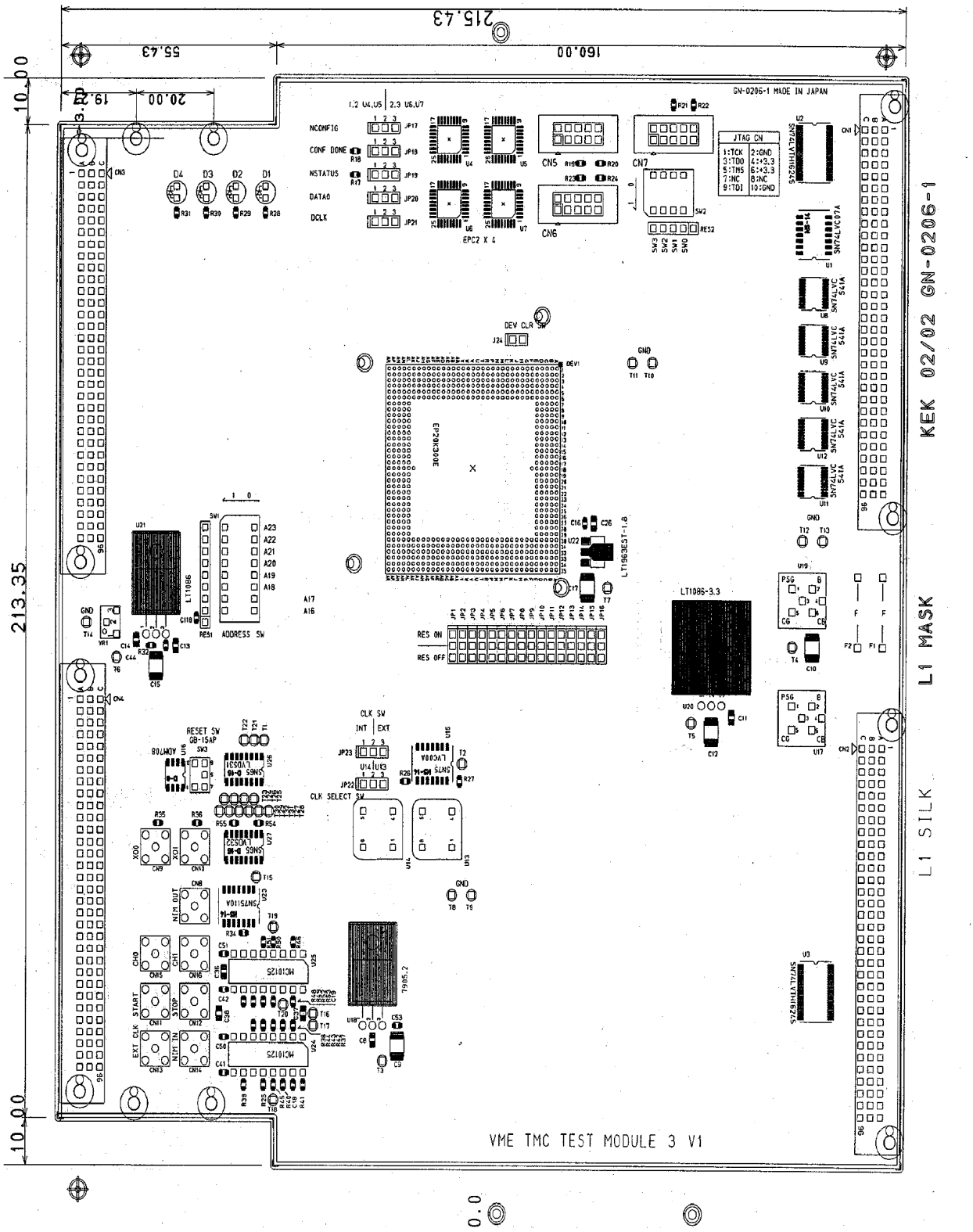


Fig. 4 TTM-3 Board Layout

TTM-3 board Connections

[Upper:CN3-RowA]

RowA	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3 Sub	TMC-X1 Sub
1	gnd	gnd					
2	XIO_D0	IO1_0	7	LVDSTX01p	AA5	DIO0	SFT0
3	XIO_D1	IO1_1	7	LVDSTX01n	AA6	DIO1	SFT1
4	XIO_D2	IO1_2	7	LVDSTX02p	AB3	DIO2	SFT2
5	XIO_D3	IO1_3	7	LVDSTX02n	AB2	DIO3	SFT3
6	gnd	gnd					
7	XIO_D4	IO1_4	7	LVDSTX03p	AB4	DIO4	SFT4
8	XIO_D5	IO1_5	7	LVDSTX03n	AB5	DIO5	SFT5
9	XIO_D6	IO1_6	7	LVDSTX04p	AC2	DIO6	SFT6
10	XIO_D7	IO1_7	7	LVDSTX04n	AC1	DIO7	SFT7
11	gnd	gnd					
12	TMC_WS*						
13	-	1.8V					
14	-5.2V	-5.2V					
15	gnd	gnd					
16	3.3V	3.0-3.6V					
17	3.3V	3.0-3.6V					
18	3.3V	3.0-3.6V					
19	gnd	gnd					
20	-	IO3_0	8	I/O	AR16		
21	-5.2V	-5.2V					
22	-5.2V	-5.2V					
23	gnd	gnd					
24	XIN_A1	IO3_1	8	I/O	AP16	RA0	
25	XIN_A2	IO3_2	8	I/O	AN16	RA1	
26	XIN_A3	IO3_3	8	I/O	AM16	RA2	
27	gnd	gnd					
28	XIN_A4	IO3_4	8	I/O	AR15	RA3	
29	XIN_A5	IO3_5	8	I/O	AP15	RA4	
30	XIN_A6	IO3_6	8	I/O	AL11	DSPACE	
31	XIN_A7	IO3_7	8	I/O	AL13		
32	5V	5V					

[Upper:CN3-RowB]

RowB	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3 Sub	TMC-X1 Sub
1	gnd	gnd					
2	XFIFO_D0	IO1_8	7	LVDSTX05p	AC4		SFT8
3	XFIFO_D1	IO1_9	7	LVDSTX05n	AC5		SFT9
4	XFIFO_D2	IO1_10	7	LVDSTX06p	AD2	ENCCONT	SFT10
5	XFIFO_D3	IO1_11	7	LVDSTX06n	AD1	ENCCONT(n)	SFT11
6	gnd	gnd					
7	XFIFO_D4	IO1_12	7	LVDSTX07p	AD3		SFT12
8	XFIFO_D5	IO1_13	7	LVDSTX07n	AD4		SFT13
9	XFIFO_D6	IO1_14	7	LVDSTX08p	AE1		SFT14
10	XFIFO_D7	IO1_15	7	LVDSTX08n	AD6		SFT15
11	XFIFO_D8	-					
12	gnd	gnd					
13	OUT_0	IO1_16	7	LVDSTX09p	AE3	DIO0	SFT16
14	OUT_1	IO1_17	7	LVDSTX09n	AE4	DIO1	SFT17
15	OUT_2	IO1_18	7	LVDSTX10p	AF1	DIO2	SFT18
16	OUT_3	IO1_19	7	LVDSTX10n	AE6	DIO3	SFT19
17	gnd	gnd					
18	OUT_4	IO3_8	7	LVDSTX11p	AL14	DIO4	SFT20
19	OUT_5	IO3_9	7	LVDSTX11n	AM1	DIO5	SFT21
20	OUT_6	IO3_10	7	LVDSTX12p	AM1	DIO6	SFT22
21	OUT_7	IO3_11	7	LVDSTX12n	AM1	DIO7	SFT23
22	gnd	gnd					
23	OUT_8	IO3_12	7	LVDSTX13p	AM1	DIO8	
24	OUT_9	IO3_13	7	LVDSTX13n	AN9	DIO9	
25	OUT_10	IO3_14	7	LVDSTX14p	AN1	DIO10	
26	OUT_11	IO3_15	7	LVDSTX14n	AN1	DIO11	
27	gnd	gnd					
28	OUT_12	IO3_16	7	LVDSTX15p	AN1	DIO12	FT0
29	OUT_13	IO3_17	7	LVDSTX15n	AN1	DIO13	FT1
30	OUT_14	IO3_18	7	LVDSTX16p	AP7	DIO14	FT2
31	OUT_15	IO3_19	7	LVDSTX16n	AP8	DIO15	FT3
32	5V	5V					

[Upper:CN3-RowC]

RowC	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3	TMC-X1 Sub
1	XIO_D8	IO1_20	8	I/O	AF2	DIO8	
2	XIO_D9	IO1_21	8	I/O	AF3	DIO9	
3	XIO_D10	IO1_22	8	I/O	AF6	DIO10	
4	XIO_D11	IO1_23	8	I/O	AF5	DIO11	
5	gnd	gnd					
6	XIO_D12	IO1_24	8	I/O	AH1		
7	XIO_D13	IO1_25	8	I/O	AG2		
8	XIO_D14	IO1_26	8	I/O	AG5		
9	XIO_D15	IO1_27	8	I/O	AG4		
10	gnd	gnd					
11	OUT_16	IO1_28	8	I/O	AG6	DIO16	
12	OUT_17	IO1_29	8	I/O	AJ1	DIO17	
13	OUT_18	IO1_30	8	I/O	AH3	DIO18	
14	OUT_19	IO1_31	8	I/O	AK1	DIO19	
15	gnd	gnd					
16	OUT_20	IO3_20	8	I/O	AR1	DIO20	FT4
17	OUT_21	IO3_21	8	I/O	AP14	DIO21	FT5
18	OUT_22	IO3_22	8	I/O	AL16	DIO22	FT6
19	OUT_23	IO3_23	8	I/O	AN1	DIO23	FT7
20	gnd	gnd					
21	OUT_24	IO3_24	8	I/O	AM1	DIO24	FT8
22	OUT_25	IO3_25	8	I/O	AR1	DIO25	FT9
23	OUT_26	IO3_26	8	I/O	AR1	DIO26	FT10
24	OUT_27	IO3_27	8	I/O	AP13	DIO27	FT11
25	gnd	gnd					
26	OUT_28	IO3_28	8	I/O	AN1	DIO28	FT12
27	OUT_29	IO3_29	8	I/O	AL15	DIO29	FT13
28	OUT_30	IO3_30	8	I/O	AP9	DIO30	FT14
29	OUT_31	IO3_31	8	I/O	AP10	DIO31	FT15
30	gnd	gnd					
31	5V	5V					
32	5V	5V					

[Lower:CN4-RowA]

RowA	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3 Sub	TMX-X1 Sub
1	gnd	gnd					
2	XIO_0	IO2_0	3	LVDSRX01p	R33	TRIGGER	SDIN
3	XIO_1	IO2_1	3	LVDSRX01n	R32	EVENTRSTB	SCLK
4	XIO_2	IO2_2	3	LVDSRX02p	P35	BUNCHRSTB	SRST
5	XIO_3	IO2_3	3	LVDSRX02n	R30	START	SDOUT
6	gnd	gnd					
7	XIO_4	IO2_4	3	LVDSRX03p	P34	GETDATA	ERST
8	XIO_5	IO2_5	3	LVDSRX03n	P33	ASDMOD	RST
9	XIO_6	IO2_6	3	LVDSRX04p	P30		
10	XIO_7	IO2_7	3	LVDSRX04n	P31		
11	gnd	gnd					
12	XCLK	X_CLK				XCLK	CLK
13	gnd	gnd					
14	−	XRST					
15	gnd	gnd					
16	3.3V	3.0-3.6V					
17	3.3V	3.0-3.6V					
18	3.3V	3.0-3.6V					
19	gnd	gnd					
20	XIN_0	XIN_0				XIN_0	HITIN
21	XIN_1	XIN_1				XIN_1	
22	XIN_2	-					
23	XIN_3	-					
24	3.0-3.6V	3.0-3.6V					
25	XIN_4	XIN_L0_p					
26	XIN_5	XIN_L0_n					
27	XIN_6	XIN_L1_p					
28	XIN_7	XIN_L1_n					
29	gnd	gnd					
30	3.3V	3.0-3.6V					
31	5V	5V					
32	5V	5V					

[Lower:CN4-RowB]

RowB	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3 Sub
1	gnd	gnd				
2	CS*	IO2_8	3	LVDSRX05p	N34	CS
3	WR*	IO2_9	3	LVDSRX05n	N33	WR
4	XTMC_RST*	IO2_10	3	LVDSRX06p	N30	RESETB
5	-	IO2_11	3	LVDSRX06n	N31	
6	gnd	gnd				
7	5V	5V				
8	XIO_8	IO2_12	3	LVDSRX07p	M35	DREADY
9	XIO_9	IO2_13	3	LVDSRX07n	M34	CLKOUT
10	XIO_10	IO2_14	3	LVDSRX08p	M31	ERRORB
11	XIO_11	IO2_15	3	LVDSRX08n	M32	(TDO)
12	gnd	gnd				
13	XIO_12	IO2_16	3	LVDSRX09p	L35	(TRSTB)
14	XIO_13	IO2_17	3	LVDSRX09n	L34	(TDI)
15	XIO_14	IO2_18	3	LVDSRX10p	L31	(TMS)
16	XIO_15	IO2_19	3	LVDSRX10n	L32	(TCK)
17	gnd	gnd				
18	—	-				
19	-	-				
20	gnd	gnd				
21	-5.2V	-5.2V				
22	3.3V	3.0-3.6V				
23	3.3V	3.0-3.6V				
24	3.3V	3.0-3.6V				
25	gnd	gnd				
26	XIO_16	IO2_20	3	LVDSRX11p	L30	
27	XIO_17	IO2_21	3	LVDSRX11n	K35	
28	XIO_18	IO2_22	3	LVDSRX12p	K32	
29	XIO_19	IO2_23	3	LVDSRX12n	K33	
30	gnd	gnd				
31	5V	5V				
32	5V	5V				

[Lower:CN4-RowC]

RowC	TTM-2	TTM-3	Bank	Cell	Pin#	AMT2&3 Sub
1	XIO_20	IO2_24	3	LVDSRX13p	K30	SERIOUT
2	XIO_21	IO2_25	3	LVDSRX13n	J35	
3	XIO_22	IO2_26	3	LVDSRX14p	J33	STROBE
4	XIO_23	IO2_27	3	LVDSRX14n	J34	
5	gnd	gnd				
6	XIO_24	IO2_28	3	LVDSRX15p	J32	
7	XIO_25	IO2_29	3	LVDSRX15n	J31	
8	XIO_26	IO2_30	3	LVDSRX16p	H34	
9	XIO_27	IO2_31	3	LVDSRX16n	G35	
10	gnd	gnd				
11	XIO_28	FAST3	5	FAST3	AP19	
12	XIO_29	FAST4	5	FAST4	AP17	
13		1.8V				
14		1.8V				
15	gnd	gnd				
16		3.3V				
17		3.3V				
18		3.3V				
19	gnd	gnd				
20	AI_8	XCLK_p		direct		
21	AI_9	XCLK_n		direct		
22	AI_10	CLK4p	8	CLK4p	T2	
23	AI_11	CLK4n	8	CLK4n	T3	
24	3.3V	3.0-3.6V				
25	AI_12	XO_L0_p		direct		
26	AI_13	XO_L0_n		direct		
27	AI_14	XO_L1_p		direct		
28	AI_15	XO_L1_n		direct		
29	gnd	gnd				
30	-5.2V	-5.2V				
31	-5.2V	-5.2V				
32	5V	5V				

		TTM-3	Bank	Cell	Pin#	
		NIM_OUT	8	I/O	R6	