TMC Test Module 2 (TTM2) Manual

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Y.Arai (yasuo.arai@kek.jp) and M. Ikeno
KEK, National High Energy Accelerator Research Organization
(http://atlas.kek.jp/~araiy/)
and
M. Sagara and T. Emura
Tokyo A & T

1.Introduction

TTM2 module was developed for testing custom LSI's. By changing a sub-board, which is attached in front of a main-board, many kind of LSI's can be mounted. In addition, the module contains 3 CPLD chips and 2 FIFO buffers, so this makes the module very flexible

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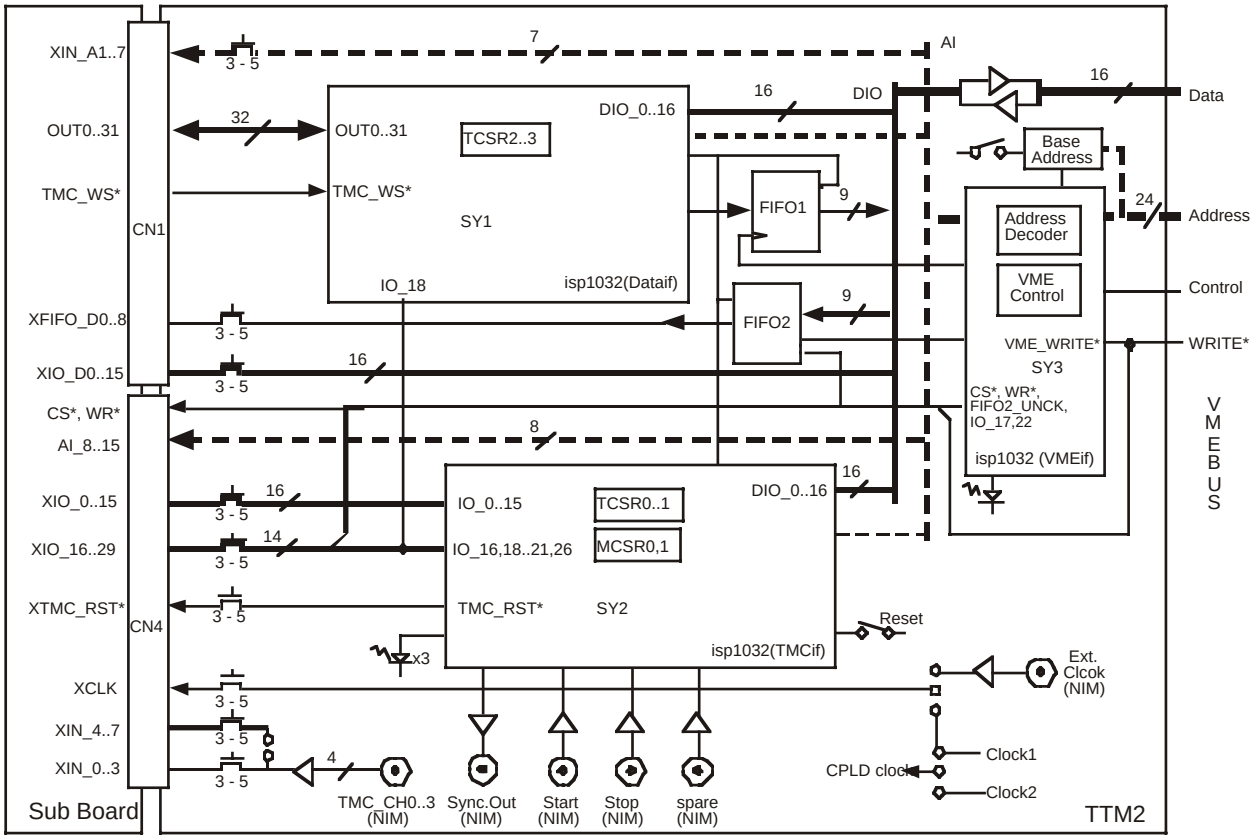


Fig. 1 TTM2 Board Block Diagram

2.VME Address Map

[General Map] ([A23:A16] = Base Address, AM = 39, 3A, 3D or 3E)

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000 : FEFE	sub-board internal address	R/W
FF00	MCSR0	R/W
FF02	MCSR1	R/W
FF04 : FF0E	reserved	
FF10	TCSR0	R/W
FF12	TCSR1	R/W
FF14	TCSR2	R/W
FF16	TCSR3	R/W
FF18 : FFEE	reserved	
FFF0	| FIFO1	R
FFF2	| FIFO2	W
FFF4 : FFFE	reserved	

[TMC-PHX1, AMT-TEG1 sub-board map]

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000	TMC CSR0	R/W
0002	TMC CSR1	R/W
0004	TMC CSR2	R/W
0006	TMC CSR3	R/W
0008	TMC CSR4	R/W
000A	TMC CSR5	R/W
000C	TMC CSR6	R/W
000E	TMC CSR7	R/W
0010 : FEFE	not used	

[AMT-1 sub-board map]

Address	15 . . . 8 | 7 . . . 0	Read/Write
0000	TMC CSR0	R/W
0002	TMC CSR1	R/W
0004	TMC CSR2	R/W
0006	TMC CSR3	R/W
0008	TMC CSR4	R/W
000A	TMC CSR5	R/W
000C	TMC CSR6	R/W
000E	TMC CSR7	R/W
0010	TMC CSR8	R/W
0012	TMC CSR9	R/W
0014	TMC CSR10	R/W
0016	TMC CSR11	R/W
0018	TMC CSR12	R/W
001A	TMC CSR13	R/W
001C	TMC CSR14	R/W
001E	(TMC CSR15)	R/W
0020	TMC CSR16	R/W
0022	TMC CSR17	R/W
0024	TMC CSR18	R/W
0026	TMC CSR19	R/W
0028	TMC CSR20	R/W
002A	TMC CSR21	R/W
002C : 003E	not used	
0040	DSPACE[15:0]	R
0042	DSPACE[31:16]	R
0044 : FEFE	not used	

Caution!: Remove FIFO1(U15) and Level Converters (U1 and U10) when AMT-1 sub board is used.

3.Main Board Control & Status Registers

[MCSR0]

bit	Read/Write	Name	Comment
0	R/W	TMCRESET	TMC chip reset
1	R/W	OTHERRESET	Sub-board reset (reserved)
2	R/W	FIFO1 RESET	FIFO1 reset
3	R/W	FOFO2 RESET	FIFO2 reset
4	R/W	SCNT RESET	Stop Counter reset
5	R/W	ALL RESET	All reset
6	R/W	VSTART	Start TMC recording
7	R/W	VSTOP	Stop TMC recording
8	R	FIFO1 EMPTY	FIFO1 Empty
9	R	FIFO1 AF/AE	FIFO1 Allmost Full/Allmost Empty
10	R	FIFO1 HF	FIFO1 Harf Full
11	R	FIFO1 FULL	FIFO1 Full
12	R	FIFO2 EMPTY	FIFO2 Empty
13	R	FIFO2 AF/AE	FIFO2 Allmost Full/Allmost Empty
14	R	FIFO2 HF	FIFO2 Harf Full
15	R	FIFO2 FULL	FIFO2 Full

[MCSR1]

15 .. 0	7 .. 0
0	SCNT Counter (8bit)

4.Sub Board Signal Registers

[General Map]

TCSR1[15..0]	TCSR0 [15..0]
| 0 | 0 | XIO_29 .. 16	XIO_15 .. 0

TCSR3[15..0]	TCSR2 [15..0]
OUT_31 .. 16	OUT_15 .. 0

[TMC-PHX1 sub-board map]

[TCSR0]

bit	Read/Write	Name	Comment
0	R/W	OCLK	TMC data Output Clock
1	R/W	TRIG	TMC Trigger signal
2	R/W	-	
3	R/W	CSTART	Comm Start(=1)/Comm Stop(=0) mode
4	R/W	WSTART	TMC WSTART signal
5	R/W	SYNCMOD	Sync(=1)/Async(=0) readout mode
6	R/W	RE	TMC data Read Enable
7	R/W	OE	TMC data Output Enable
8	R	EMPFLG	TMC data Empty Flag
9	R	EVEND	TMC data Event End Flag
10	R	DVALID	TMC data Valid signal
11	R	ERR	TMC Error Flag
12	R/W	DCH0	TMC data read channel 0
13	R/W	DCH1	TMC data read channel 1
14	R/W	RPUP	TMC Read Pointer Up
15	R/W	-	

[TCSR1]

bit	Read/Write	Name	Comment
0	R	-	
1	R	-	
2	R	-	(=TCSR0_2)
3	R	-	
4	R	-	
5	R	-	
6	R	-	
7	R	VME_WRITE*	
8	R	WR*	
9	R	CS*	
10	R	-	
11	R	-	
12	R	FIFO2_UNCK	
13	R	-	
14	R	0	
15	R	0	

[TCSR2]

15 ..0

[TCSR3]

15 ..0

[AMT-TEG1 sub-board map]

[TCSR0]

bit	Read/Write	Name	Comment
0	R/W	L1BRCLK	L1B Read Clock
1	R/W	LOADFIFO	
2	R/W	ENOUT	Enable Output
3	R/W	-	
4	R/W	-	
5	R/W	-	
6	R/W	-	
7	R/W	-	
8	R	L1BEMPTY	L1B Empty Flag
9	R	L1BFULL	L1B Full Flag
10	R	ERROR	Error
11	R	-	
12	R/W	-	
13	R/W	-	
14	R/W	-	
15	R/W	-	

[TCSR1]

bit	Read/Write	Name	Comment
0	R	-	
1	R	-	
2	R	ENOUT	Enable Output(=TCSR0_2)
3	R	-	
4	R	-	
5	R	-	
6	R	-	
7	R	VME_WRITE*	
8	R	WR*	
9	R	CS*	
10	R	-	
11	R	-	
12	R	FIFO2_UNCK	
13	R	-	
14	R	0	
15	R	0	

[TCSR2]

15 ..0	
DIO15 .. 0	R/W

* Caution : These signals are 5V device output!

[TCSR3]

15 ..0	
DIO31 .. 16	R/W

* Caution : These signals are 5V device output!

[AMT-1 sub-board map]

[TCSR0]

bit	Read/Write	Name	Comment
0	R/W	TRIG	
1	R/W	EVENTRST	
2	R/W	BUNCHRST	
3	R/W	START	
4	R/W	GETDATA	
5	R/W	-	
6	R/W	-	
7	R/W	-	
8	R	DREADY	
9	R	CLKOUT	
10	R	ERROR	
11	R	TDO	
12	R/W	TRSTB	
13	R/W	TDI	
14	R/W	TMS	
15	R/W	TCK	

[TCSR1]

15 ..0
not used

[TCSR2]

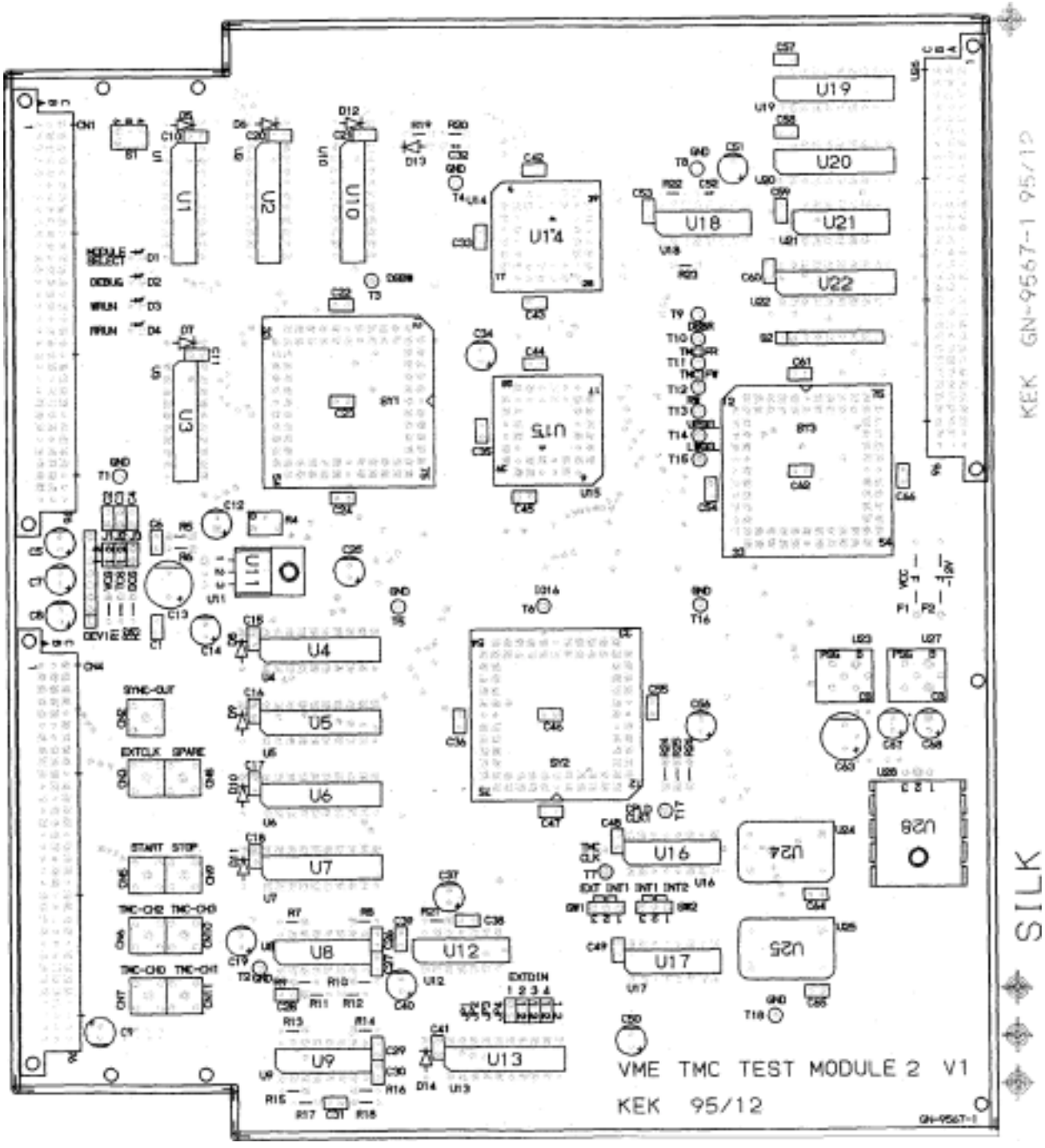
15 ..0
not used

[TCSR3]

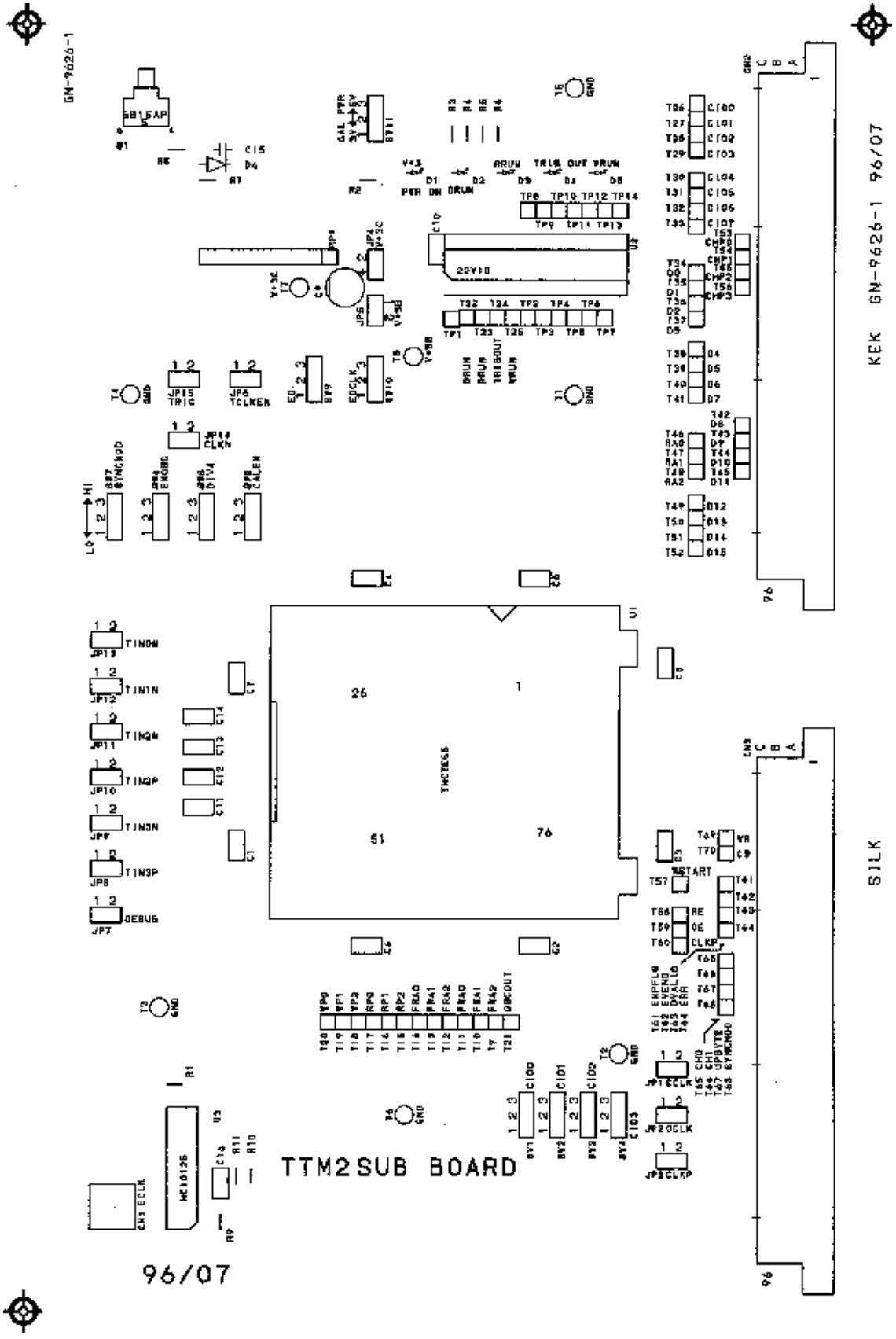
15 ..0
not used

5 .Board Layout

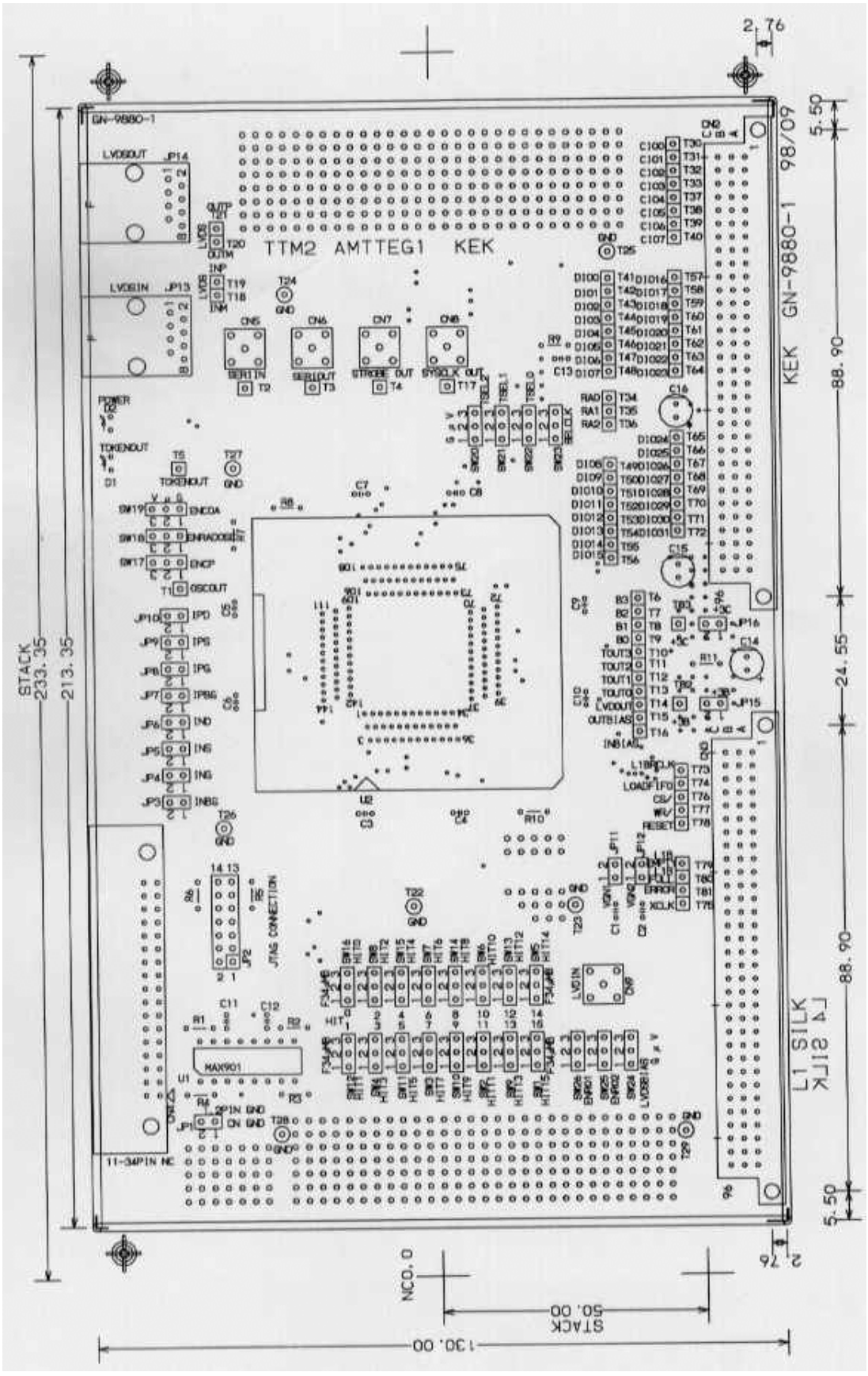
5.1.TTM2 main board



5.2.TMC-PHX1 Sub-Board Layout



5.3.AMT-TEG Sub Board



5.4.AMT-1 Sub Board