TMC1004 Specification

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Rev 1.0 Mar. 24, 1989
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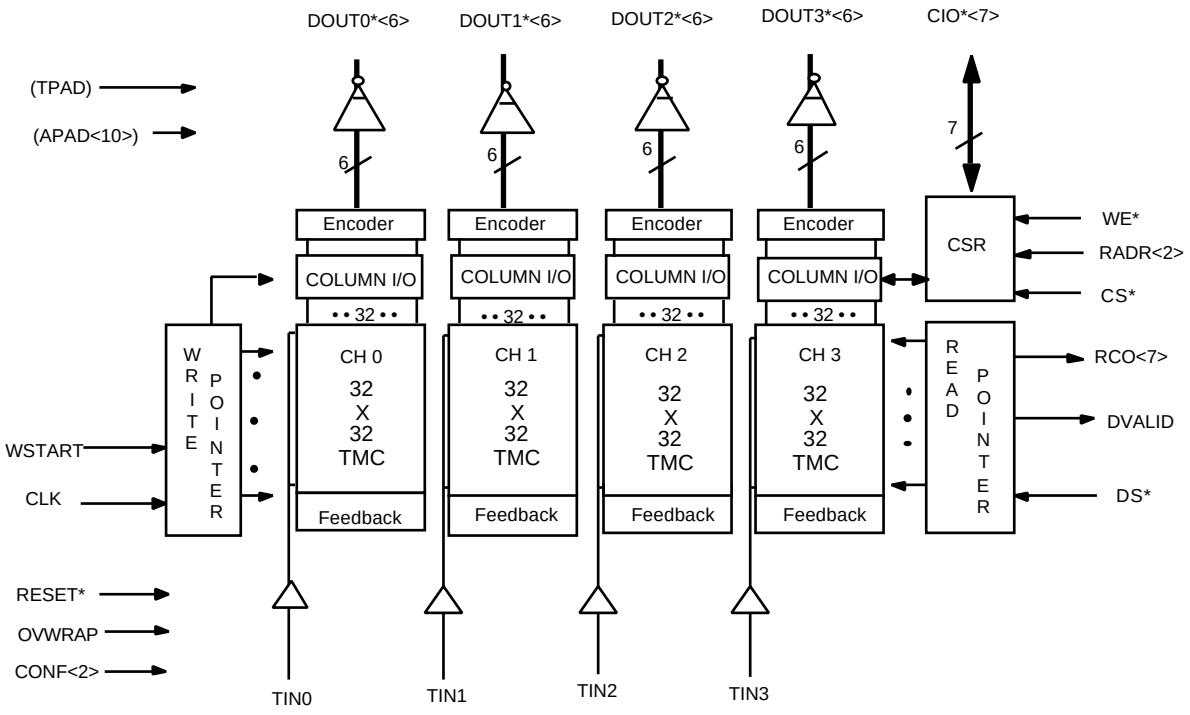
TMC1004 is a low-power and high-resolution Multi-hit Time to Digital Converter chip. It has special kind of memories which record input pulses in 1 ns time resolution. The recorded data can be read out through encoder logic. TMC1004 chip has 4 channels of circuit and each channel has 1024 bits of memories. Thus each channel records signal of 1 μsec period. The chip also can be configured to 2 channels times 2 k bits or 1 channel times 4 k bits.

MAIN FEATURES

- Least Time Count : 1 ns/bit (0.6 ~ 1.3 ns/bit depending on clock frequency)
- Time Resolution : σ = 0.52 ns
- Integral Linearity Error : σ = 0.3 ns
- Differential Linearity Error in a row : σ = 0.04 ns (< 0.2 bit)
- row-to-row Discontinuity : < 0.5 bit
- TMC array-to-array Discontinuity : < 1 bit
- Variation of Slope (time-to-digital conversion factor) : < 0.1 % (2.6 - 3.4 V)
  < 0.1 % (15 - 55 ˚C)
  < 0.1 % (chip to chip)
- Clock Frequency : 31.25 MHz (50~ 25 MHz)
- No. of Channels : 4 Channel
- No. of Row : 32 Row/Channel
- No. of Bit : 32 bit/Row
- Time Range : 1.024 μs (4 ch)
  2.048 μs (2 ch)
  4.096 μs (1 ch)
- I/O mode : (i) stand alone mode
  • Time recording
  • Encoded Readout (synchronous to write timing)
  (ii) slave mode
  • Time recording
  • Asynchronous readout after stopping the time recording.
  (iii) serial read/write mode
  • 1 bit/ch serial read/write through CSR register
  (iv) test pad mode
  • Address input from test pads and serial i/o.
- Read cycle time : Synchronous to write cycle (stand alone mode),
  or ~100ns asynchronous readout (slave mode)
- Read pointer offset : programable (1 ~ 128)
- Read count : programable (1 ~ 128)
- Data format : 6 bit encoded data for each channel
- Additional pads for test : 10 direct address pads + 1 control pad
- Total No. of pin : 88 pins = 54 (I/O) + 34 (Power/GND)
- Supply Voltage : 3 V
- I/O Level : CMOS Level
- Bare Chip Size : 5 mm x 5.6 mm
- Power Dissipation : 7 mW/CH (@100kHz read trigger rate)
- Package : 88pin PGA



TMC1004 Block Diagram

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PIN DESCRIPTION

[I = Input, O = Normal Output, TO = Three State Output; * = negative logic]

• TIN0 ~ TIN3 [I] : Timing Signal Input.

• DOUT0~3*<6> [TO] : Data out line.

• CIO*<7> [I/TO] : CSR register I/O line.

• CLK [I] : System clock input.

• WSTART [I] : Start write cycle.

• DS* [I] : Data strobe signal to read out data. In stand alone mode, several rows are read out synchronous to the WCLK until negating this signal.

• CS* [I] : CSR register select signal.

• CONF<2> [I] : Configuration bit. CONF=0 --- 4 ch x 1k bits, CONF=1 --- 2 ch x 2k bits, CONF=2 --- 1 ch x 4k bits, CONF=3 --- not used.

• RCO<7> [O] : Read counter value output.

• DVALID [O]: Data valid signal. This signal is used as timing signal to write outside buffer.

• RESET* [I] : Reset internal circuits. When this signal asserted, MODE (CSR0) is set to "0", RC(CSR1) is set to "2", and WC(CSR2) is set to "0".

• RADR<2> [I] : CSR register address line.

• WE* [I] : Read/Write control line for CSR access.

• OVR [I] : Overlap control bit. This bit selects the length of the reference cell in the feedback circuit, that is, total delay time of a row memory is changed.This ensure the last bit of each row will overlap to the first bit of the next row. (Default = High).

PAD description

Signals described below are used as test purpose only. There are no connections to package pins and these signals are pulled down to GND through a resistor.

• APAD<10> [I] : Direct memory address lines in TPAD mode.

• TPAD [I] : Mode is set to "3" when this signal is set to "1".

CSR Registers

bit	6	5	4	3	2	1	0
CSR0		MOD1	MOD0	SIO3	SIO2	SIO1	SIO0
CSR1	Read Counter Value [RC]						
CSR2	Write Counter Value [WC]						
CSR3	-						

* CSR0
  • SIO3 ~ 0 : Serial I/O bits. These bits are valid only in the serial i/o mode. One bit data for each channel is read/written through this bit from/to the address pointed by the read counter(row position) and the write counter(column position). (read/write)
  • MOD0,1 : MODE = [MOD1,MOD0]. MODE = 0 --- Stand alone mode, MODE = 1 --- Slave mode, MODE = 2 --- Serial i/o mode., MODE = 3 Test Pad mode. [read/write]

* CSR1
  • RC : Read counter value. The contents of the read counter are set through this register. The value read back indicates present value of the read counter. In Slave mode, the contents of the counter are incremented after the read/write operation. This register also works as a row address register in the serial read/write mode. [read/write]

* CSR2
  • WC : Write counter value. The contents of the write counter are set through this register. Present value of the write counter is read back. The counter is incremented by WCLK signal during WSTART is asserted. This register also works as a column address register in the serial read/write mode. [read/write]

Mode

There are 4 modes of operations in the TMC1004. These modes are selected via bits 4 and 5 in the CSR0 register. Operations of these modes are explained below.

- MODE = 0 (Stand alone Mode) : Readout cycle will be synchronous to the write cycle (= clock cycle). Encoded data are read out through DOUTx*pins during the DS* signal is asserted.

- MODE = 1 (Slave Mode) : Readout cycle will be asynchronous to the clock and controlled by the DS* signal. Usually, this mode requires stopping write cycle before starting read cycle. Encoded data are read out through DOUTx* pins.

• MODE = 2 (Serial read/write Mode) : This mode is used mainly for testing each bit in the memory. Data are read/write from/to the address pointed by the CSR1(row address) and CSR2(column address) through bit 0 ~ 3 in the CSR0. Bit 0 corresponds to the data in the CH0 and bit 1 corresponds to CH1 and so on.
(Caution: When you change the mode to 2, you have to write $2x to CSR0. Thus the content of the memory pointed by CSR1 and CSR2 is also changed to value x.)

• MODE = 3 (Test Pad Mode): This mode is also used for test purpose but only in wafer level test. Addresses are supplied through APAD0 ~ APAD9 and data are read out through CSR0 as same manner as the Serial read/write mode. By setting the TPAD to high level, this mode is automatically selected.

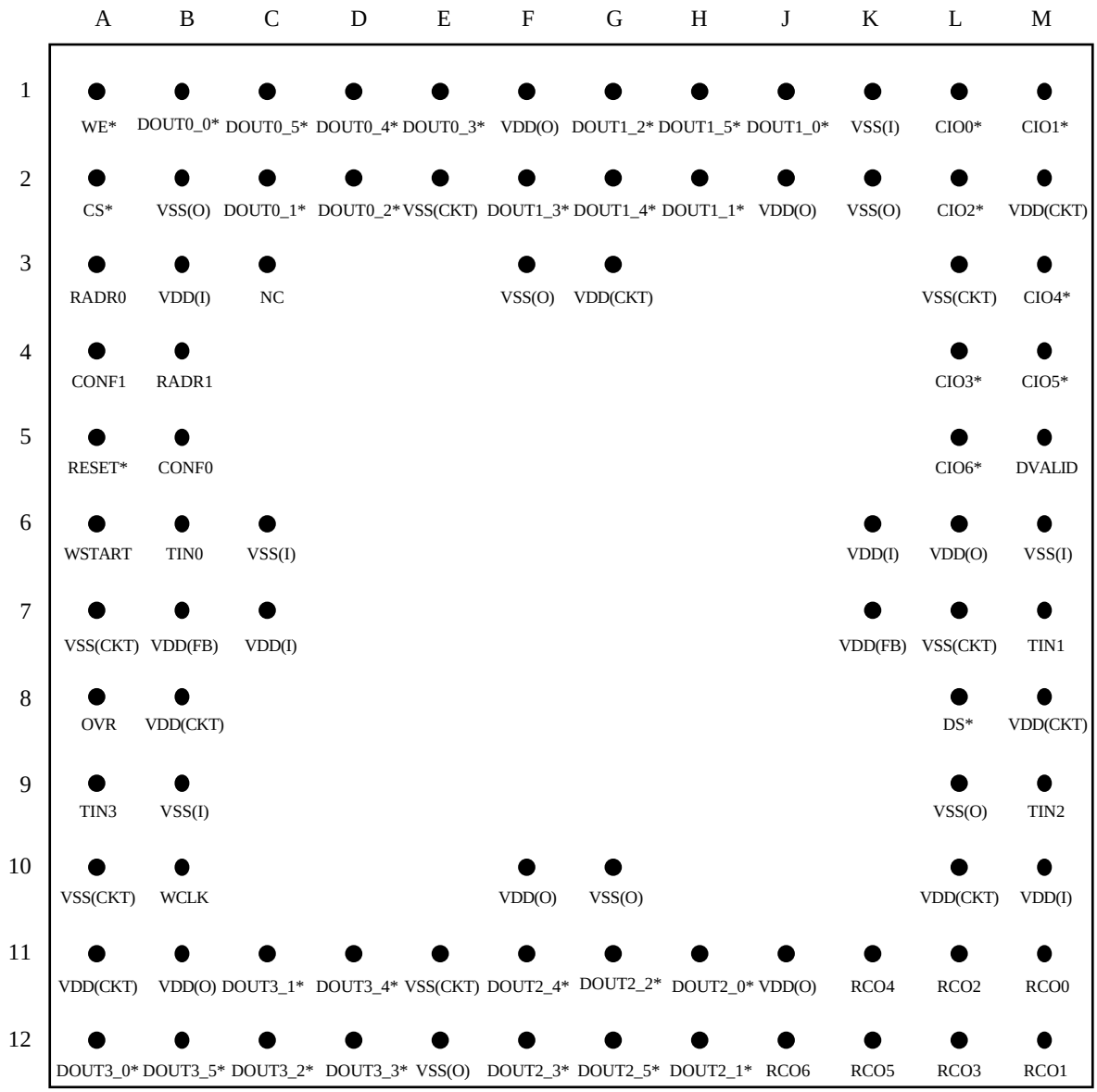
Encoded Data

Internal data of the TMC is not directly appear in the output pins. The data is encoded as shown in the Table 1. Bit position at which the data is changed from "0" to "1" is encoded in the least 5 bits. Most significant bit shows whether the first bit is "0" or "1". When the data has changed from "0" to "1" at the edge of the row, for example all the data in row N is all "0" and all data in row N+1 is all "1", you can recognize it as the encoded data in row N is "000000" and in row N+1 is "100000".

Table 1 Data Encoding

Bit Pattern*	Encoded Data					
<--------- Time 3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	5†	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0	0	0	0	0	0	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0	0	0	0	0	1	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0	0	0	0	0	1	1
x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0 0	0	0	0	1	0	0
:	:					
:	:					
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	1	1	1	1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	0	0	0	0	0
(not appear)	1	0	0	0	0	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 1	1	0	0	0	1	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x 1	1	0	0	0	1	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x x 1	1	0	0	1	0	0
:	:					
:	:					
1 0 x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1	1	1	1	1	1	1

(*) x..xx..x = 0..01..1. Only one transition from low to high is permitted. If there are more than two rising edges in a row, the encoded data will be wrong.
(†) Bit 5 of the encoded data is used for distinguish the transition between row.



TMC1004 Package (TOP View)

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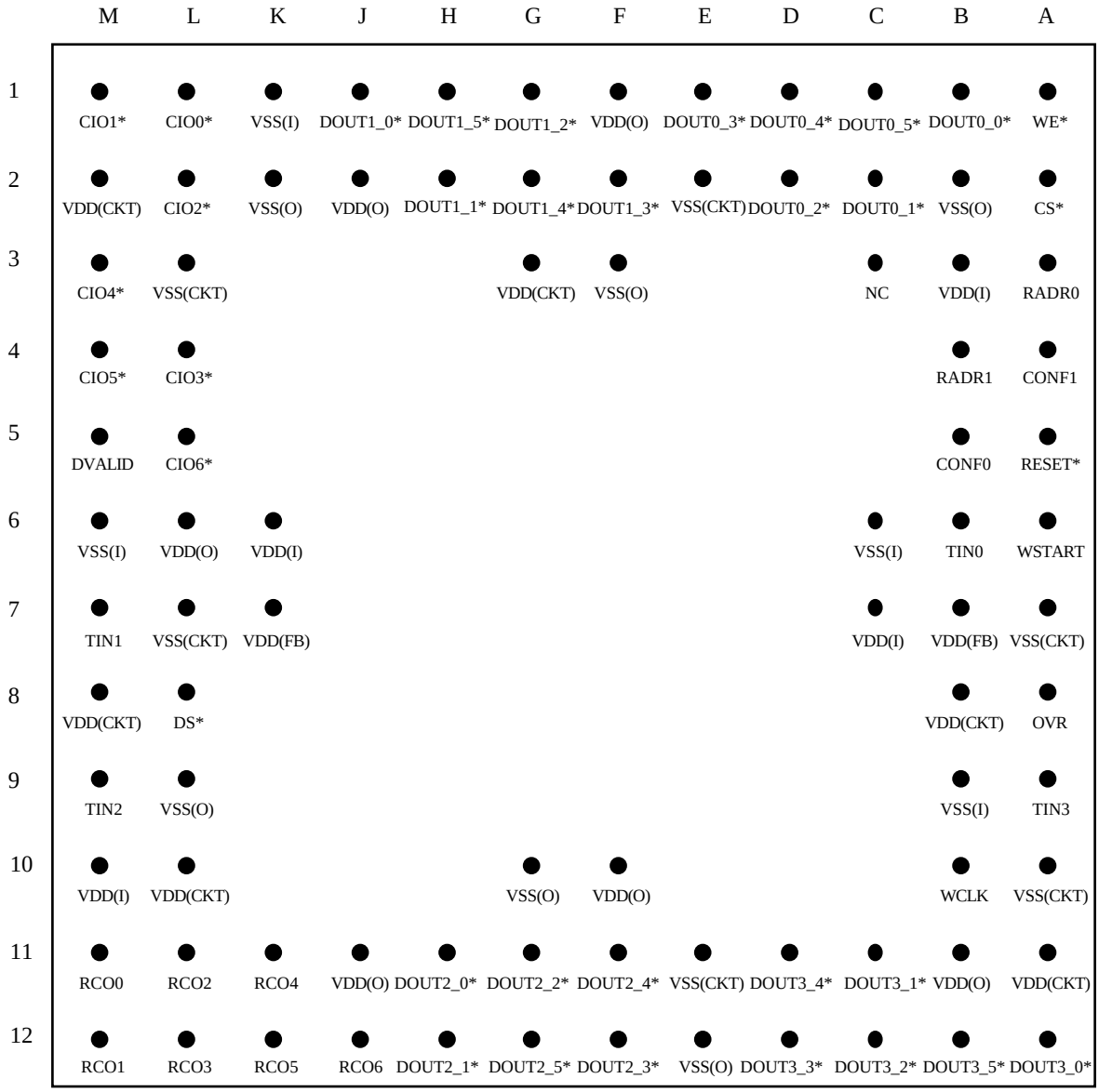

TMC1004 Package (Bottom View)

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TMC1004 Signals Pin Assignments

Signal Name	Pin	I/O
RESETN	5A	I*
WEN	1A	I*
CSN	2A	I*
RADR0	3A	I
RADR1	4B	I
WCLK	10B	I
DSN	8L	I*
WSTART	6A	I
DVALID	5M	O
TIN0	6B	I
TIN1	7M	I
TIN2	9M	I
TIN3	9A	I
CONF0	5B	I
CONF1	4A	I
OVR	8A	I
CIO0	1L	I/O*
CIO1	1M	I/O*
CIO2	2L	I/O*
CIO3	4L	I/O*
CIO4	3M	I/O*
CIO5	4M	I/O*
CIO6	5L	I/O*
DOUT00	1B	O*
DOUT01	2C	O*
DOUT02	2D	O*
DOUT03	1E	O*
DOUT04	1D	O*
DOUT05	1C	O*
DOUT10	1J	O*
DOUT11	2H	O*
DOUT12	1G	O*
DOUT13	2F	O*
DOUT14	2G	O*
DOUT15	1H	O*
DOUT20	11H	O*
DOUT21	12H	O*
DOUT22	11G	O*
DOUT23	12F	O*
DOUT24	11F	O*
DOUT25	12G	O*
DOUT30	12A	O*
DOUT31	11C	O*
DOUT32	12C	O*
DOUT33	12D	O*
DOUT34	11D	O*
DOUT35	12B	O*
RCO0	11M	O
RCO1	12M	O
RCO2	11L	O
RCO3	12L	O
RCO4	11K	O
RCO5	12K	O
RCO6	12J	O

Signal Name	Pin	I/O
VSS(CKT)	7A,10A,11E, 7L,3L,2E	GND
VSS(I)	6M,1K,9B, 6C	GND
VSS(O)	12E,2B,9L, 2K,10G,3F	GND
VDD(CKT)	11A,8M,2M, 8B,10L,3G	+3V
VDD(I)	10M,3B,7C, 6K	+3V
VDD(O)	1F,11B,11J, 6L,2J,10F	+3V
VDD(FB)	7B,7K	+3V
TPAD	N.C. (gnd)	I
APAD0	N.C. (gnd)	I
APAD1	N.C. (gnd)	I
APAD2	N.C. (gnd)	I
APAD3	N.C. (gnd)	I
APAD4	N.C. (gnd)	I
APAD5	N.C. (gnd)	I
APAD6	N.C. (gnd)	I
APAD7	N.C. (gnd)	I
APAD8	N.C. (gnd)	I
APAD9	N.C. (gnd)	I

(* -- negative logic)

TMC1004 Electrical Characteristics

Maximum Ratings

Rating	Unit	Value			Conditions
		min.	typ.	max.	
Supply Voltage (V_{DD})	V	-0.5	-	4	Ta=25℃
Input Voltage (V_I)	V	-0.5	-	V_{DD}+0.5	Ta=25℃
Output Voltage (V_O)	V	-0.5	-	V_{DD}+0.5	Ta=25℃
Storage Temperature (Tstg)	℃	-65	-	150	

Recommended Operating Conditions

Characteristics	Unit	Value			Conditions
		min.	typ.	max.	
Supply Voltage (V_{DD})	V	2.7	-	3.3	
Input High Level (V_{IH})	V	2.0	-	V_{DD}	
Input Low Level (VIL)	V	-0.5	-	0.8	
High-level Output Current (I_{OH})	mA	-1	-	-	
Low-level Output Current (I_{OL})	mA	-	-	12	
Operating Temperature (Topt)	℃	0	-	70	

DC Electrical Characteristics

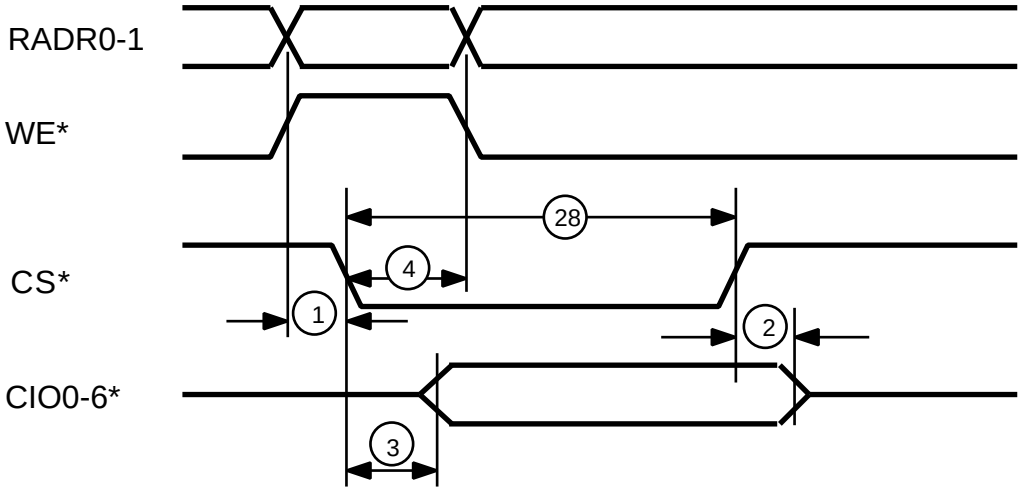
Characteristics	Unit	Value			Conditions
		min.	typ.	max.	
High-level Output Voltage (V_{OH})	V	2.4	2.6	-	V_{DD}=2.7V, I_{OH}=-1mA
Low-level Output Voltage (V_{OL})	V	-	0.2	0.4	V_{DD}=2.7V, I_{OL}=12mA
High-level Input Current (I_{IH})	μA	-10		10	V_{DD}=3.3V, V_I=2.7V
(with pull-down resistor)	μA	20		150	V_{DD}=3.3V, V_I=2.7V
Low-level Input Current (I_{IL})	μA	-10	-	10	V_{DD}=3.3V, V_I=0.4V
High-Impedance Output Current (I_{OZ})	μA	-10	-	10	V_{DD}=3.3V, V_{OH}=2.7V, V_{OL}=0.4V

AC Electrical Specifications (Preliminary) 1992.3.13

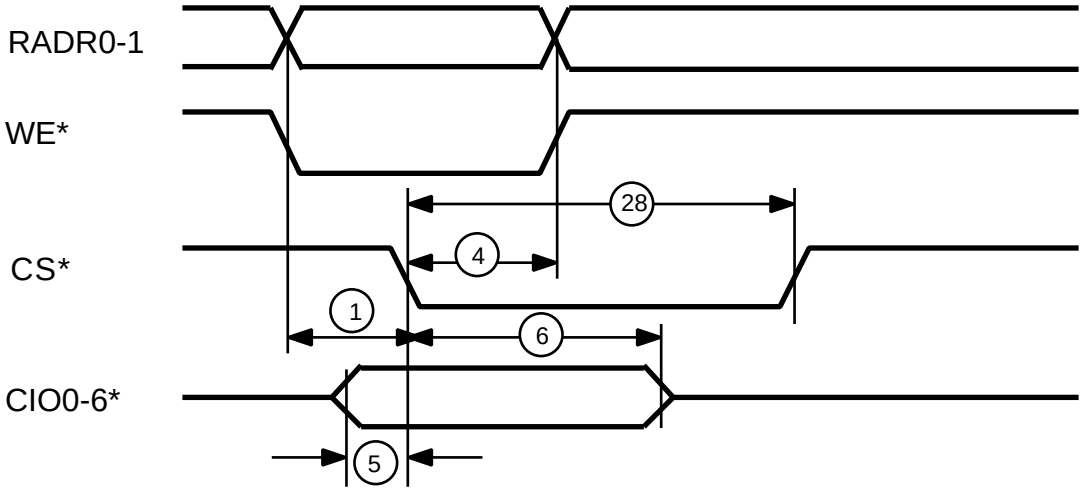
Number	Characteristic	Min.	Max.	Unit
1	RADR,WE* Setup Time	5	-	ns
2	CS* Negated to CIO* Negateed	6	14	ns
3	CS* Asserted to CIO* Asserted	9	17	ns
4	RADR,WE* Hold Time	5	-	ns
5	CIO* Setup Time	0	-	ns
6	CIO* Hold Time	20	-	ns
7	APAD Setup Time	10	-	ns
8	CS* Negated to CS* Asserted	20	-	ns
9	TPAD Setup Time	20	-	ns
10	CS* Negated to TPAD,APAD Negated	10	-	ns
11	CLK Frequency (f_{CLK})	25	50	MHz
12, 13	CLK Pulse Width	8	25	ns
14	CLK Rise and Fall Time	-	3	ns
15	TIN Rise and Fall Time	-	5	ns
16	CLK high to DS* Asserted (a)	10	-	ns
17	DS* Asserted to CLK high (a)	5	-	ns
18	CLK low to DVALID Asserted	4	12	ns
19	CLK high to DVALID Negated	8	16	ns
20	CLK low to DOUT* Impedance Change	3	11	ns
21	CLK high to WSTART Asserted (b)	5	-	ns
22	WSTART Asserted to CLK high (b)	5	-	ns
23	CLK high to TIN valid	0	5	ns
24	CLK high to TIN invalid	0	5	ns
25	TIN Cycle Time to encode valid data (c)	$1/f_{CLK}$	-	ns
26	TIN low width	2	-	ns
27	TIN high width	2	-	ns
28	CS* Width Asserted	20	-	ns
29	RESET Width Asserted	30	-	ns
30	RESET Negated to control signals valid	30	-	ns

(a) If DS* is asserted outside of these specifications, it is not guaranteed to start readout in S0 cycle. In that case, the DS* signal is accepted anyway, but the readout cycle may start in previous or next cycle.
(b) If WSTART is asserted outside of these specifications, it is not guaranteed to start record in S0 cycle. In that case, the WSTART signal is accepted anyway, but the record cycle may start in previous or next cycle.
(c) This limitation only come from encoding logic. No limitation for TIN cycle to write data in memory except number 26 and 27 conditions.

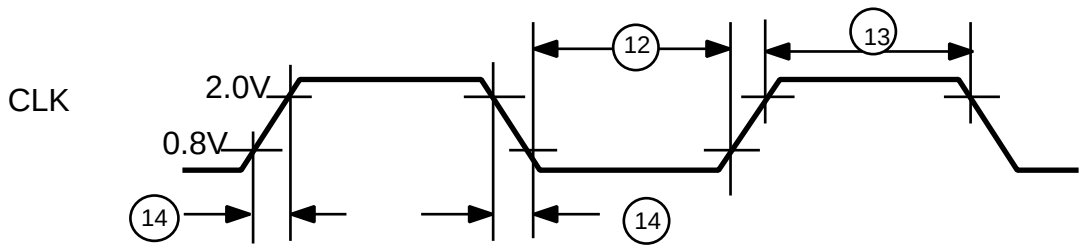
[Read-CSR Cycle Timing Diagram]



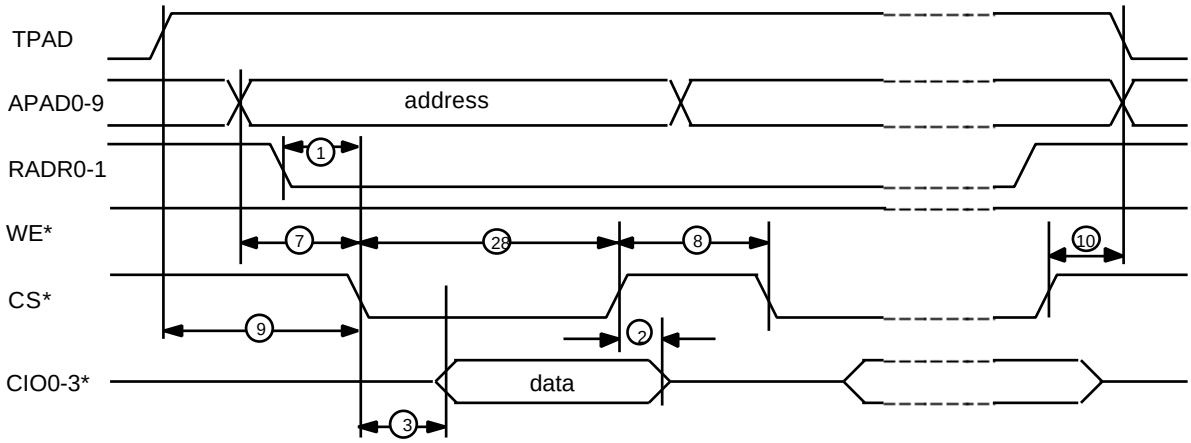
[Write-CSR Cycle Timing Diagram]



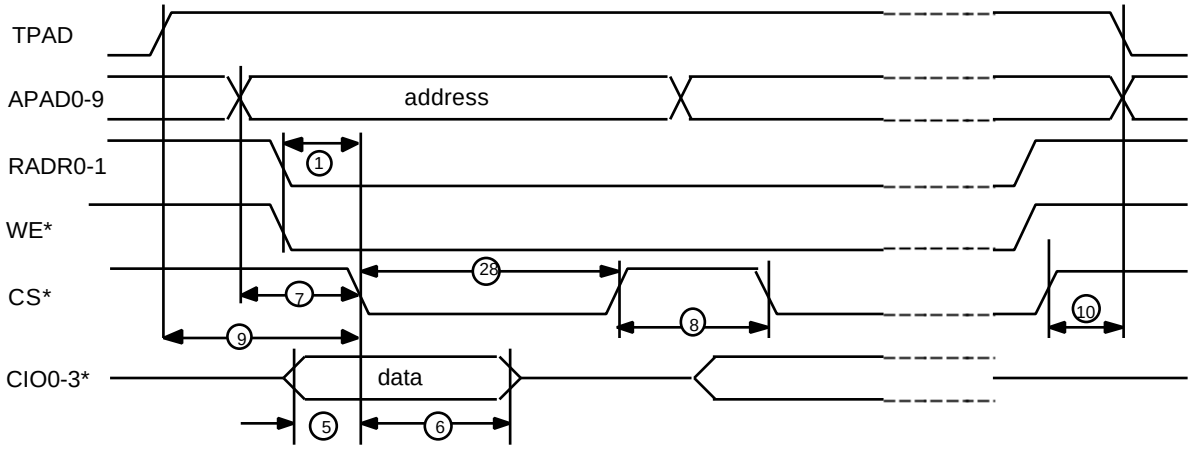
[Clock Input Timing Diagram]



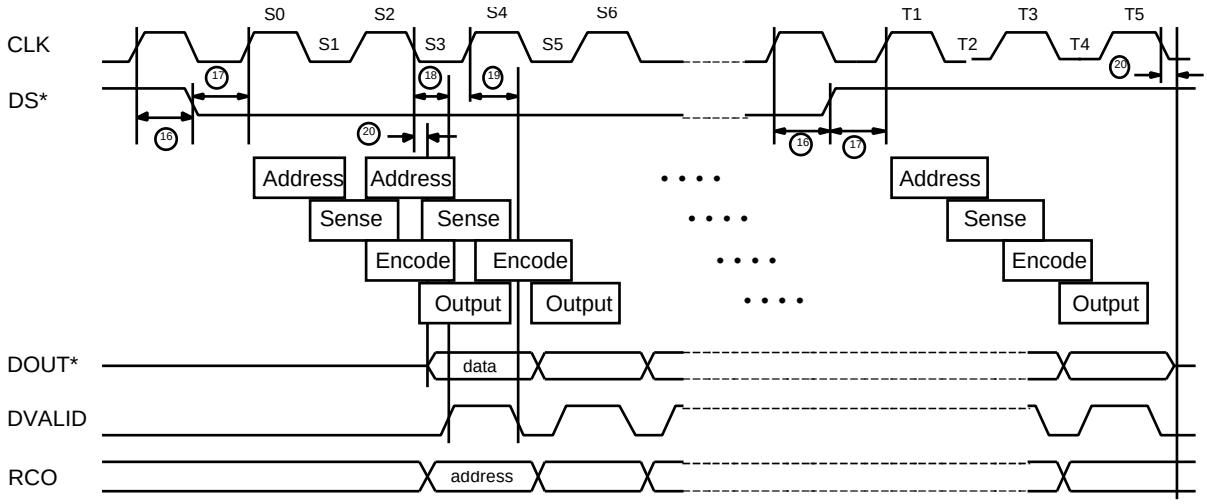
[Test PAD Read Cycle Timing]



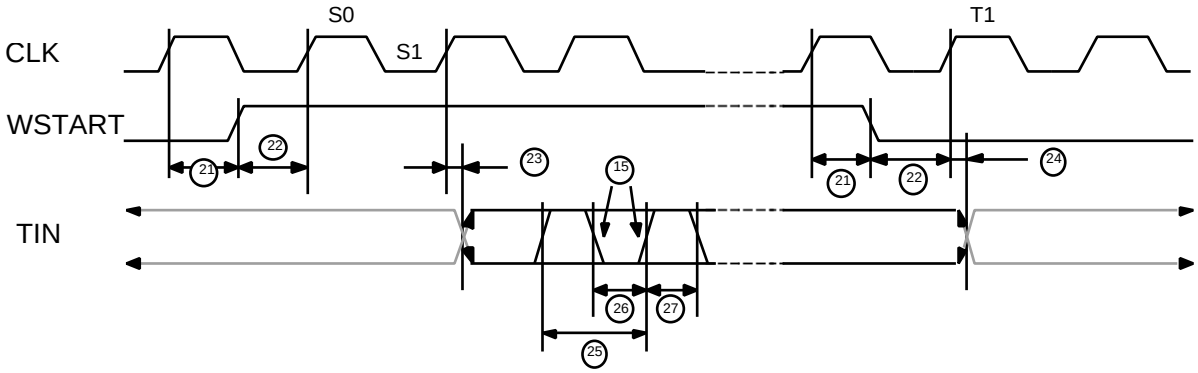
[Test PAD Write Cycle Timing]



[MOD=0 Readout Timing Diagram]



[Data Recording Timing Diagram]



[Reset Timing Diagram]