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A CMOS 4CH x 1K TIME MEMORY LSI WITH 1 NS/BIT RESOLUTION

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Abstract - A 4-channel 1024-bit Time-to-Digital Converter chip, which records input signals to memory cells at one nano second intervals, has been developed. To achieve one nano second precision, the chip incorporates a feedback stabilized delay element. The chip was fabricated on a 5.0 mm by 5.6 mm die using 0.8 μm CMOS technology. It dissipates only 7 mW/channel under typical operating conditions.

I. Introduction

Particle detectors for future high energy accelerators have demanding requirements for readout electronics. A VLSI circuit designed specifically for this application is an efficient way to meet the requirements. One of such accelerators is the SSC (Superconducting Super Collider) being built at Texas USA. In the SSC, two proton beams will collide at every 16 ns and this collision creates hundreds of particles. The energy and tracks of these particles are detected by sophisticated detectors which are instrumented with electronics of million channels. Although the data rate is very high, the amount of information we really need is much smaller than the amount that is actually stored. So, the readout system must have data buffering.

To detect the position of a particle track, we usually measure drift time of electron which is created by the particle. In this measurement, we need time-to-digital converters with 1 ns resolution. The circuit must maintain the history of the input for more than 1 μs pending receipt of a readout trigger. The readout must not create dead time. As more than 100,000 channels of the time-to-digital electronics will be mounted in the very limited space of a detector, the chip must be high density and low power. Furthermore the device must not deteriorate in the ambient flux of particles and γ rays that is present in the vicinity of the detector.

The idea of Time Memory Cell (TMC) was proposed by us and tested by making a TEG chip [1]. The cell utilizes low-power and high-density characteristics of a CMOS memory cell and short delay time of a gate. Figure 1 shows the basic operation of the TMC. As the write signal (WL) timing in each TMC cell is delayed by 1 ns, timing information of the input lines (TIN and TIN*) is recorded to memory cells sequentially. To keep the delay time constant, the

delay time of the delay element is controlled through the Vg line by a feedback circuit which refers to an external system clock period.

In an alternative approach described by Stevens et al. [2] the timing information is stored in a switched capacitor array and digitized much later. Our approach depends much less on small signal analog electronics and is therefore preferable in the detector environment where levels of radiation and electrical noise may be high.

A new TMC LSI chip (TMC1004) has been developed using an 0.8 μm CMOS process. It contains 4 channels and each channel has 1024 TMC cells (32 rows and 32 columns). The chip achieves more than 10 times the density of a 1 GHz GaAs shift register [3] while dissipating less than 1 % of the power.

II. Time Memory Cell Technique

A. Concept

A GaAs shift register clocked at 1 GHz would provide the 1 ns precision that we require, but the power dissipation of this technology is unacceptably large. Therefore we sought to accomplish our objectives in CMOS technology for which the power dissipation is intrinsically low.

In CMOS circuitry the objective of low power is further served by use of a low clock frequency and minimization of data transfers from gate to gate. The difficulty with CMOS where timing is critical is that the propagation delay of a gate may vary by around 100 % because of fluctuations in chip processing, supply voltage, temperature and so on. However, the delay time of a gate which has a same physical layout is fairly uniform within a chip. We make a feedback circuit which controls delay time of the series of gates, and eliminates the process, voltage and temperature variability.

In one channel of a TMC1004 chip, 1024 TMC cells are configured as 32 rows of 32 cells. Within a row the input is written to successive cells at intervals of approximately 1 ns. The rows are successively enabled for writing by an external clock with period 32 ns.

B. Feedback circuit

The principle of our feedback circuit is analogous to the principle of a phase locked loop (PLL). Whereas a PLL stabilizes an oscillator frequency by referencing to the phase of an external clock, the TMC feedback stabilizes a variable delay element by referencing to the period of an external clock.

Figure 2 shows the schematic of the feedback circuit. When an external clock (φ_1) sets the flip-flops F1 and F2 at its falling edge, capacitors C1 and C2 begin to charge. The charging of C1 stops at the falling edge of the pulse (φ_3) from the end of the reference row. The charging of C2 stops at the next falling edge of the clock pulse (φ_2). Hence, the voltage difference between

C1 and C2 is proportional to the time difference between the delay line and clock period. Comparator A1 checks the voltage difference and adjusts the feedback voltage (Vg). If the delay time is less than the clock period, C3 charges during a store period increasing the delay of the delay line. If the delay time is longer than the one clock period, C3 discharges reducing the delay.

C. Timing Accuracy

We give here a rough estimate of the timing accuracy attainable by the TMC circuit. The circuit essentially shows a characteristic structure in every 32 ns. Random error for each cell is accumulated in root-sum square from the first cell to the last cell in a row. On the other hand, constant error for each cell is summed lineally from the first cell to the last cell.

There are three main sources of error; the non-uniformity of the delay element, the instability of the feedback circuit, and the time jitter in the input and clock signals. Primarily, the non-uniformity and the time jitter cause random error, and the instability causes constant error.

Non-uniformity of the delay element makes difference of delay time between cells, between rows, and between reference row and actual row. The non-uniformity between cells shows up as differential linearity. Since the difference between cells is not accumulated, the differential linearity in a row is relatively good. If there is 5% non-uniformity in delay time of each delay element, error for total delay in a row will be $\sqrt{32} \times 0.05\text{ns} \approx 0.3$ ns. This error causes discontinuity in data between rows, and introduces some error in feedback circuit because it relies on the uniformity between reference row and actual row.

The errors in feedback circuit also come from sensitivity of the comparator and controllability of the feedback voltage (see Fig. 3-(a)). Since the input voltage of the comparator changes 1.5V for 32 ns period (= 50 mV/ns) and the comparator detects ±25 mV voltage difference from the reference voltage, the sensitivity of the comparator is ±0.5 ns. The adjustment of the feedback voltage is set to ~ 20mV per feedback cycle, so the corresponding delay time change is only ~10 ps / cell. However, this adjustment changes the total delay time of a row by ~0.3ns.

Time jitters of the input and the clock (write) signals may be caused by electrical and thermal noises when those signals pass through buffers (see Fig. 3-(b)). We have used about 20 buffers between input pad and a TMC cell. Assuming the time jitter of 30 ps, the total time jitter in these signals will be $\sqrt{20} \times 30\text{ ps} \approx 0.1$ ns, and the jitter at the end of write line (WL) is around 0.2 ns.

Since the delay times of buffers between input pad and a TMC cell are not controlled, those buffers have variations of delay time caused by the change of supply voltage and temperature. However, those variations are mostly cancelled each other by designing the number of buffers from input to the TMC cell to be the same.

In addition to these errors, digital conversion device has digitization error intrinsically. For 1 ns digitization step the digitization error σ_{dig} is $1 / \sqrt{12} = 0.29$ ns. In actual device, the timing error is a complex combination of errors described above. We think it is possible to make the device which has the maximum error of less than 1.5 ns and the RMS error of around 0.5 ns.

III. Circuit Description

A. Circuit Block

A Block diagram of the TMC1004 is shown in Fig. 4. The chip has four TMC arrays, each with 32 rows by 32 columns of TMC cells. Each array has a feedback circuit. For accessing the four arrays, there are two pointers Write and Read each of which consists of a 7-bit counter and decoder. The Write Pointer is incremented in each clock (CLK) cycle which initiates a pulse in the write line of the designated row. The Read Pointer selects a row for readout and is incremented by the same clock (CLK). This scheme with two pointers and dual port cells enables read and write operations to proceed simultaneously. The four TMC arrays can be configured as 4, 2, or 1 channels by setting external pins. The 4, 2, and 1 channel modes utilize respectively the lower 5, 6 or 7 bits of the counters and retain the input history for 1, 2 and 4 μsec.

The 32 bits of row information are encoded to 6 bits at readout time so as to reduce the data size and the required number of leads to the chip.

The chip maintains various parameters in three control and status registers (CSR) which can be read as well as written.

B. Time Memory Cell

The schematic of the TMC cell is shown in Fig. 5. Each cell has one timing-information write port (TIN and TIN*) and one data-read/write port (BL and BL*). We used static memory in the TMC cell, because it may be more stable for radiations than the dynamic one. Two PMOS transistors (M1 and M2) are added to the previous design [1]. They make the write operation insensitive to the previous contents of the cell by interrupting the feedback paths during the write pulse. Transistor parameters of the delay element were selected to obtain a gate delay time close to 1 ns/bit.

The delay time of the delay element is controlled by the PMOS transistor M3. Since the input signal is latched in memory cell at the falling edge of the signal on WL', only the falling edge is controlled via the feedback voltage Vg. The transistor M3 changes the rise time of the signal at node A. At the input to the second inverter the pulse width changes and at its output the regenerated signal edge is again sharp.

C. Feedback Circuit

The operation of the feedback circuit was described in previous section. Figure 6 shows the result of simulation of the delay element. With Vg fixed the delay varies by more than ±20% with changes in power supply voltage (2.7 V ~ 3.3 V), temperature (27 ˚C ~ 70 ˚C), and transistor threshold voltage (-10% ~ +10%). With Vg controlled by the feedback circuit (1.2 V ~ 2.3 V), the delay time is kept at 1 ns.

D. Encoder

The 32-bit row data is encoded to 6 bits. Since transition times are spaced by at least 32 ns and only the rising-edge timing of input signal is interest in our application, the encoder logic accommodates only one "0" to "1" transition in a row of memory. Thus the encoding reduces the output pin requirement and the amount of data without sacrificing data quality. Figure 7 shows the diagram of the encoding circuit. At first, "0" to "1" transition position is detected at AND gates, then the position is encoded through the wired-OR logic. The most significant bit shows the value of bit 0, and the remaining 5 bits show the encoded data for the "0" to "1" transition position. The most significant bit is needed to detect the transition between the rows.

E. Readout Pipeline

Simultaneous reading and writing require that the operations proceed in phase so that the memory operates as a ring buffer. One row must be read out during each 32 ns interval in which a row is written. The readout cycle (memory read and encoding) is pipelined to two stages and the cycle continues while the trigger signal DS* is asserted. The data are presented on the DOUT lines.

F. Control registers

There are three CSR registers which set / show the operating mode and the settings of the pointers. Two bits of CSR#0 encode the operating mode, and four bits provide serial access to the cells of the TMC arrays. This access path is used for testing each TMC cell. The Read Pointer can be written and read via CSR#1 and the Write Pointer via CSR#2. The CSR register is accessed through the CS* and the CIO lines.

III. Measured Performance

The specifications and the measured performance of the TMC1004 are summarized in Table 1. Each item is discussed below.

A. Linearity

Figure 8-(a) shows the linearity curve of the TMC1004. As the chip is referencing an external quartz oscillator (31.25 MHz), the slope of the linear fit to

the data (time-to-digital conversion factor) is very stable and has the value of 1.000 ± 0.001 bit/ns without any tuning. The integral linearity error (Fig. 8- (b)) is the deviation from the ideal response function. A Gaussian fit to the integral linearity error distribution shows σ = 0.31 ns, and the maximum deviation is less than 1.5 ns.

Figure 9 shows the fine structure of the linearity curve. The first part of the row has a nearly ideal response to input, but in the latter part of the row the response is rather broad. This trend reflects the accumulation of error along a row and the resynchronization at the start of the next row. Making the rows shorter could reduce the integral linearity error but at the cost of increased power dissipation.

Figure 10 shows the differential linearity error. We get σ = 4% from Gaussian fit to the data and maximum deviation is less than 20 %. This indicates the non-uniformity of the delay element is around 4%.

We observed discontinuity in data is less than 0.5 ns for row-to-row, and less than 1 ns for TMC array-to-array.

B. Stability

While the chip has non-negligible amount of integral and differential errors, its overall characteristic is very stable. Figures 11-(a) and (b) show the variation in slope with voltage and temperature for a channel. The variation is plotted as a deviation from the data point of 3.0V and 25 ˚C. Due to the feedback circuit, the slope is stable within 0.1% for voltage variation of 2.6 - 3.4 V and temperature variation of 15 - 55 ˚C.

C. Power Consumption

The most power consuming part of the chip is a sense amplifier circuit. There are 128 sense amps on a chip, one for each column of each channel. To minimize power dissipation, the DC current to the sense amps is normally held off and is raised only when a readout trigger arrives. With the feedback circuit operating, the power dissipation is about 3 mW/ch in 4 channel mode. When continuous write operation starts, the power dissipation increases to about 6.5 mW/ch. Finally, during readout the power dissipation increases by 24 mW/ch. With a readout duty factor of 1 % as expected in a typical operating environment, the average power dissipation is 6.7 mW/ch

D. Time Resolution

Figure 12 shows results of time resolution measurement. In this measurement, the deviation from ideal response line is measured and plotted. Gauss fit to the data shows σ_{total} = 0.52 ns. Assuming the σ_{total} is the quadrature sum of digitization error (σ_{dig} = 0.29 ns) and the TMC

error (σ_{TMC}), we get $\sigma_{TMC} \sim 0.46$ ns. This value is in good agreement with the our rough estimate in section II.

E. Layout

Figure 13 shows the photograph of a TMC1004 chip. Four TMC arrays are arranged in quadrants. Control logic is placed in the cross shaped area separating the arrays. The chip was designed by full-custom layout, and the size is 5.0 mm by 5.6 mm.

IV. Summary

A new time-to-digital converter chip, the TMC1004, has been designed. It has 1 ns/bit least count and can record for up to 4 μs. A novel variable delay element and a feedback circuit are employed to get 1 ns accuracy. Power consumption is very low due to the CMOS static memory-like structure. Tests show that overall linearity and stability are very good. This chip is designed for time-to-digital conversion chip, but the methods used to get 1 ns timing and to record to memory can be adapted to other applications such as a memory for recording high-speed signals.

Acknowledgments

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[1] Y. Arai and T. Baba, "A CMOS Time to Digital Converter VLSI for High-Energy Physics", in 1988 Symposium on VLSI Circuits, Dig. Tech. Papers, Aug.1988, IEEE CAT. No. 88 TH 0227-9 pp 121-122.

[2] A. Stevens et al., "A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors", IEEE J. Solid-State Circuits, vol. SC-24, no. 6, pp. 1748-1752, Dec. 1989.

[3] O. Sasaki et al., "1.2 GHz GaAs Shift Register IC for Dead-Time-Less TDC Application", IEEE Trans. on Nucl. Sci. Vol. 36 (1989)512.

Table 1.TMC1004 Specifications

No. of Channels	4 channel
Least Time Count	1 ns / bit
Time Range	1.024 μs (4 ch), 2.048 μs (2 ch) or 4.096 μs (1 ch)
Clock Frequency	31.25 MHz
Time Resolution	σ = 0.52 ns
Integral Linearity Error	σ = 0.3 ns (< 1.5 bit)
Differential Linearity Error in a row	σ = 0.04 ns (< 0.2 bit)
row-to-row Discontinuity	< 0.5 bit
TMC array-to-array Discontinuity	< 1 bit
Variation of Slope (time-to-digital conversion factor)	< 0.1 % (2.6 - 3.4 V) < 0.1 % (15 - 55 ˚C) < 0.1 % (chip to chip)
Data Output	32 ns cycle 2 stage pipeline. 6 bit encoded output.
No. of Pins	54 I/O pins and 34 Power / Gnd pins
Supply Voltage	3.0 V
Power Consumption	7 mW/ch for 1 % readout duty factor.
Chip size	5.0 mm x 5.6 mm

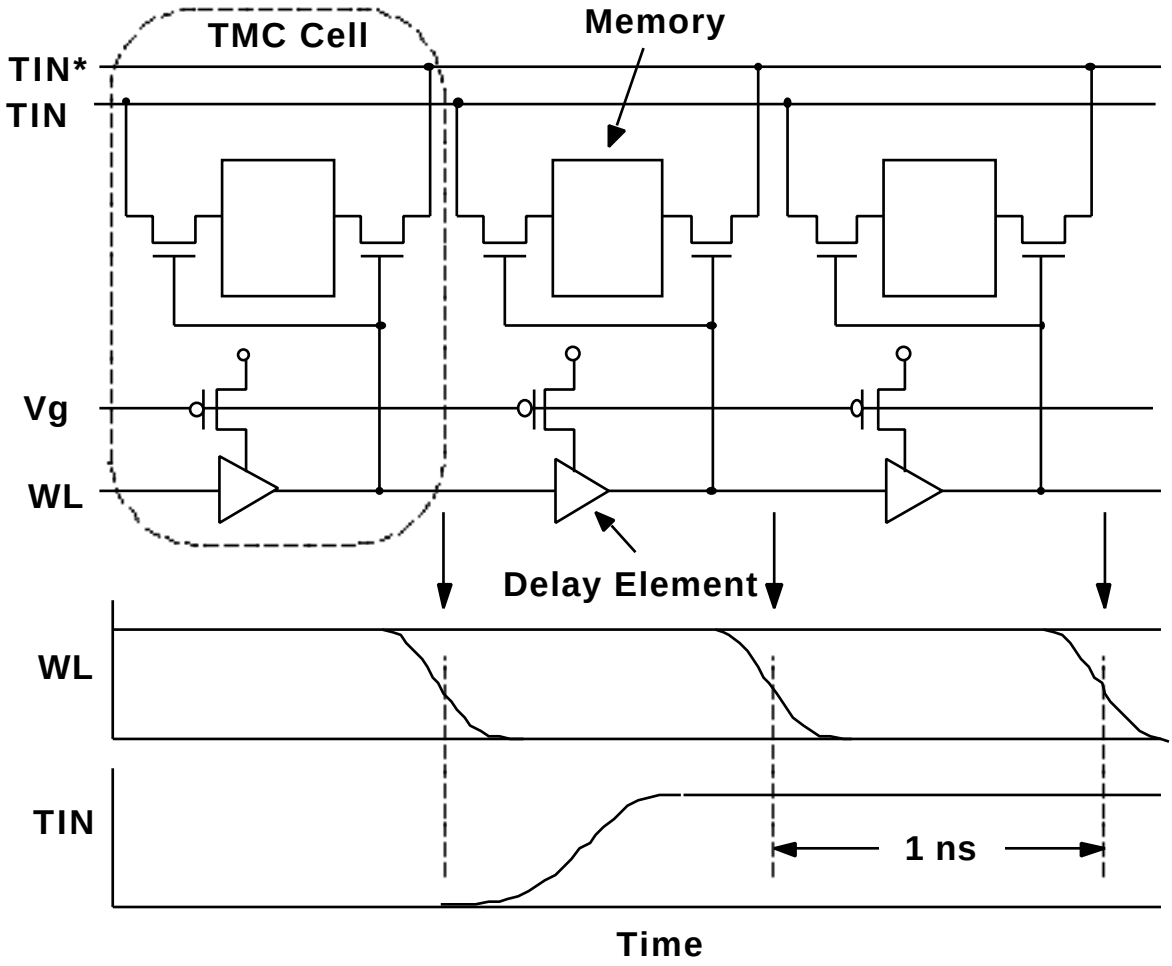


Fig. 1. Input timing write operation in the TMC cells.

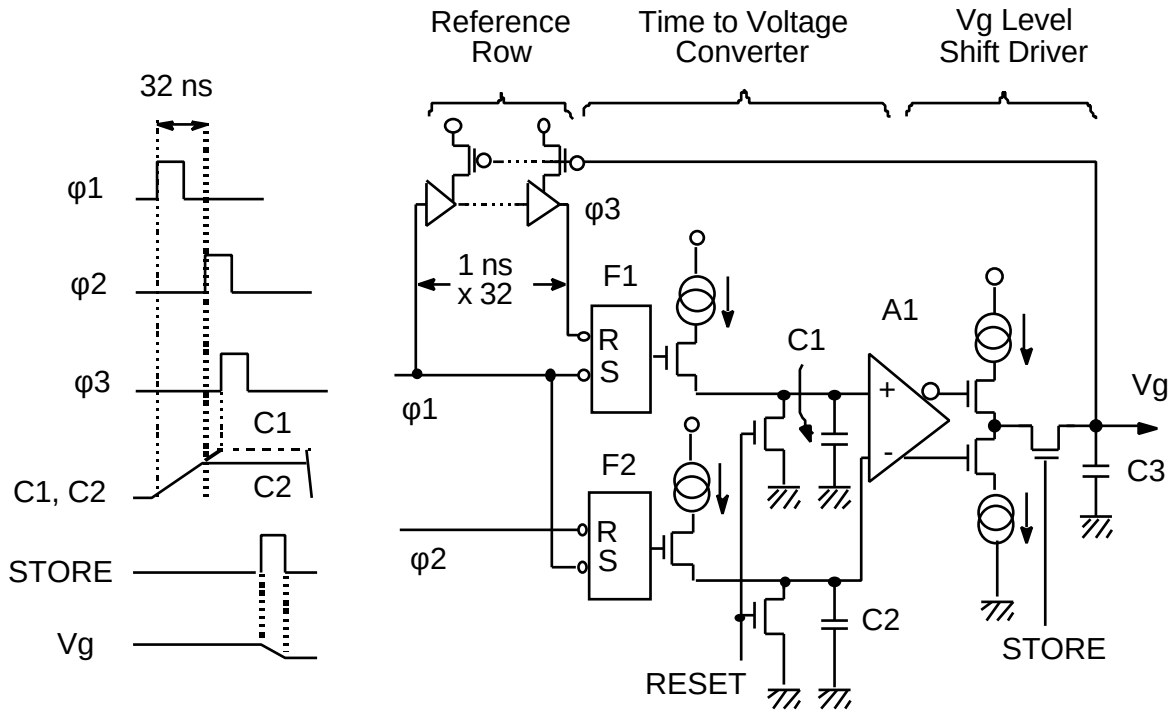


Fig.2. Block diagram of the feedback circuit.

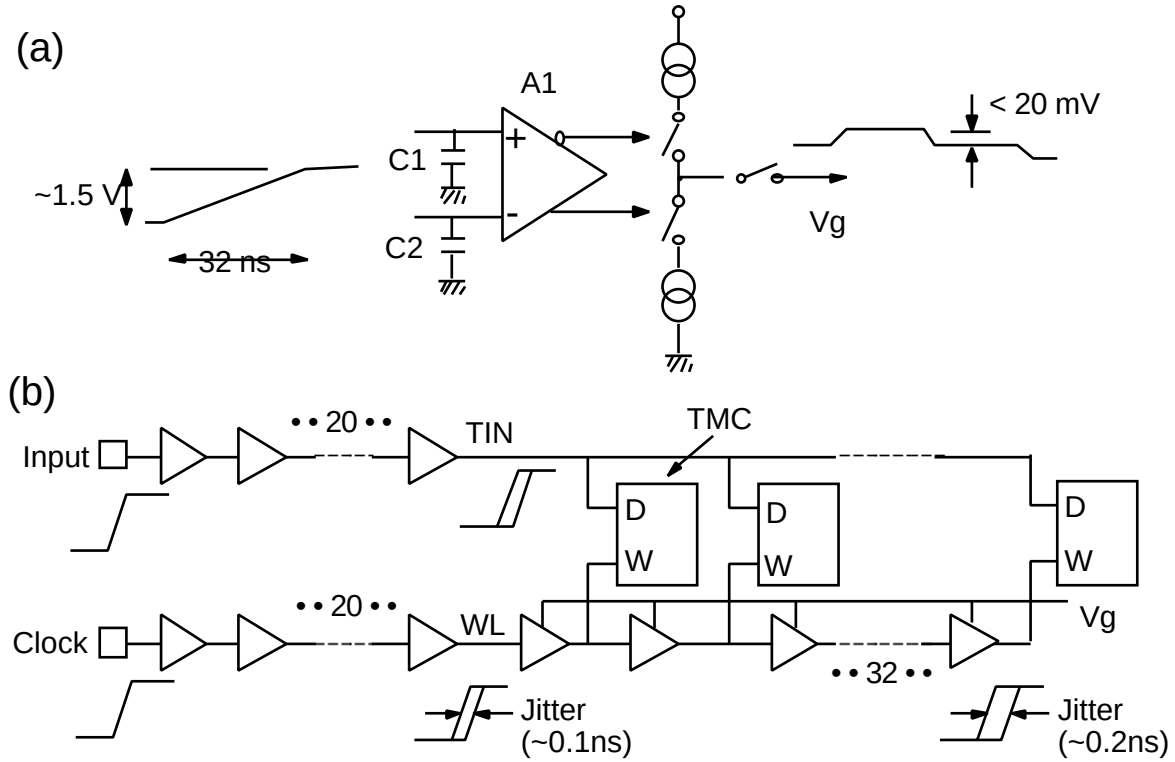


Fig. 3 (a) Signal levels in the feedback circuit. (b) Signal jitter in the input buffers and the TMC circuit.

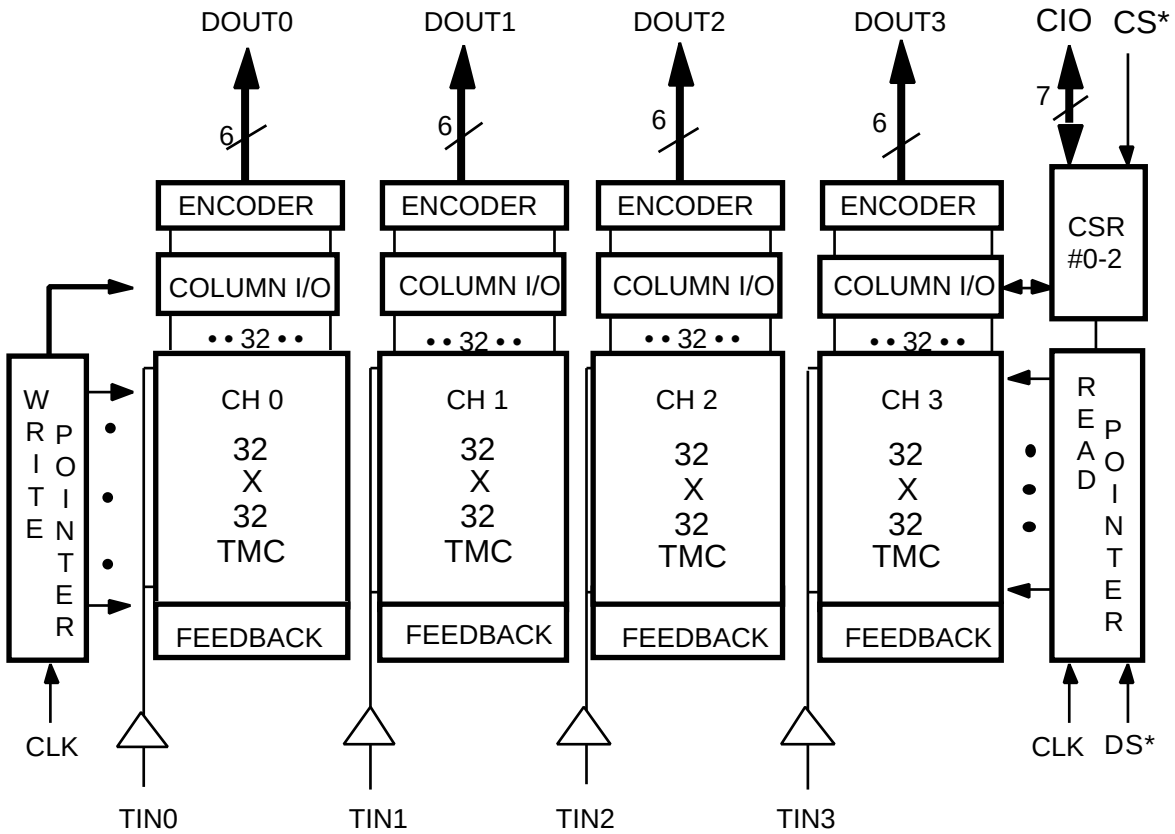


Fig. 4. Block diagram of the TMC1004.

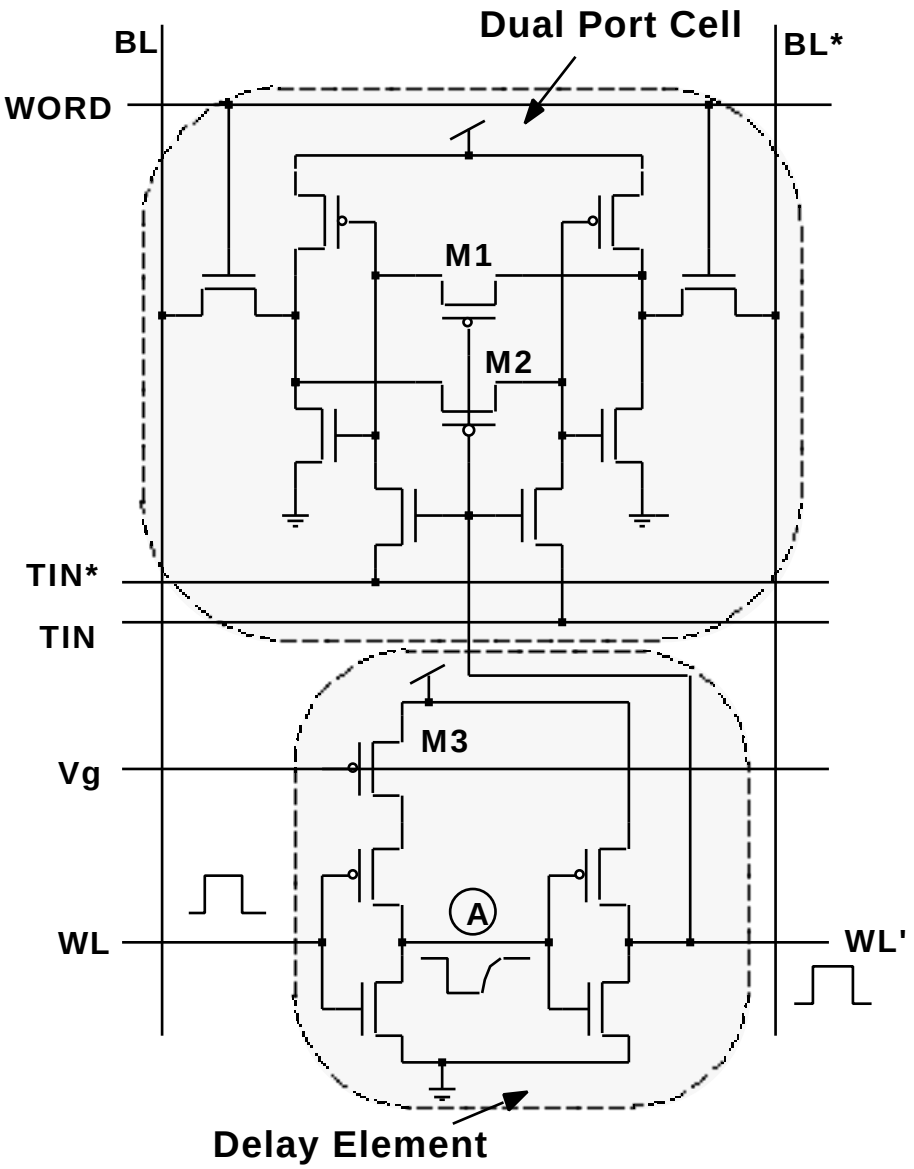


Fig. 5. Schematics of a TMC cell.

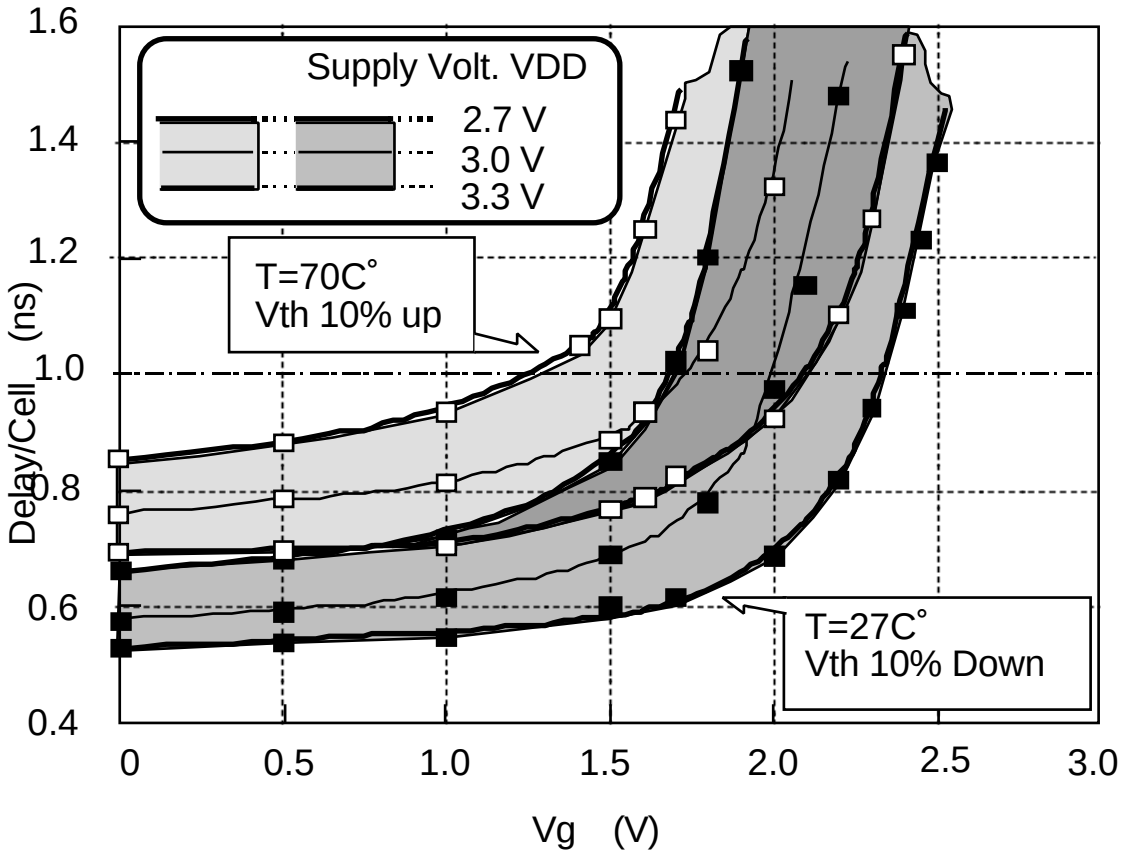
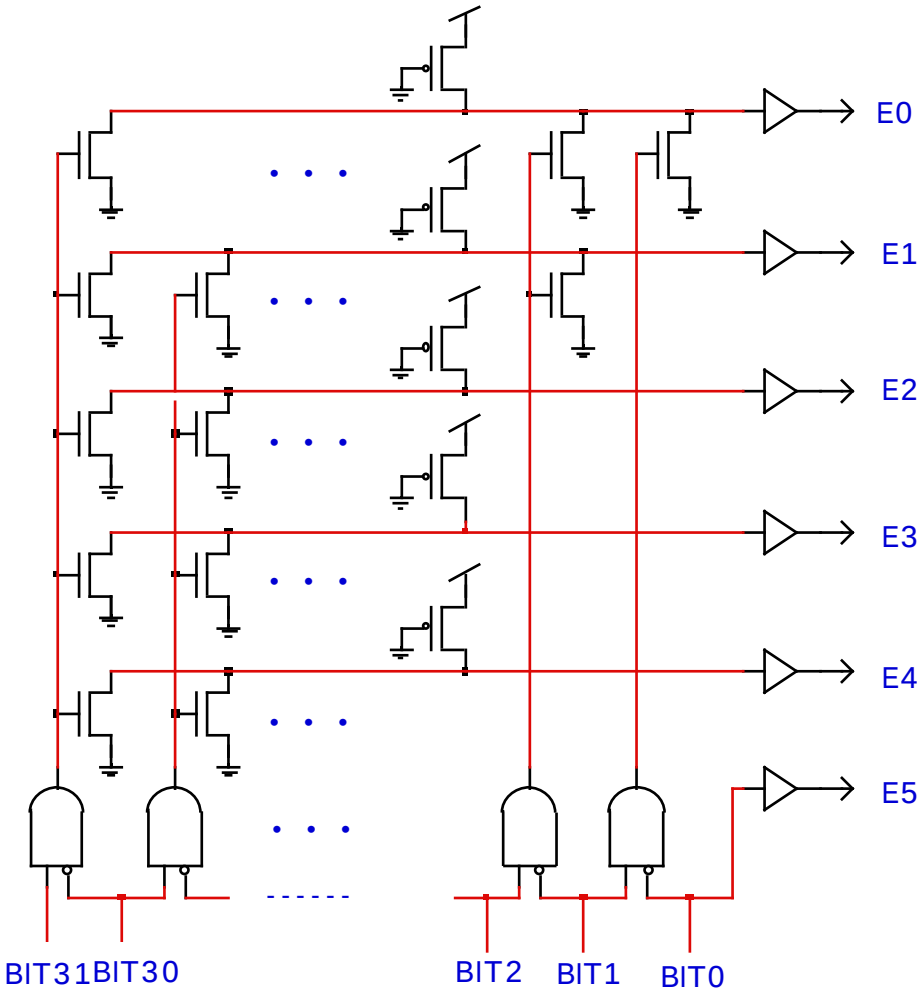


Fig. 6. Results of simulation for the delay time of the delay element.



Bit Pattern	Encoded Data
3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	E E E E E E 5 4 3 2 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0	0 0 0 0 0 1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0	0 0 0 0 1 0
:	:
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0
(not appear)	1 0 0 0 0 1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 1	1 0 0 0 1 0
:	:
1 0 x x x x x x x x x x x x x x x x x x x x x x x x x x x 1	1 1 1 1 1 1

x..xx..x = 0..01..1

Fig.7. Circuit diagram of the encoding logic and a encode table.

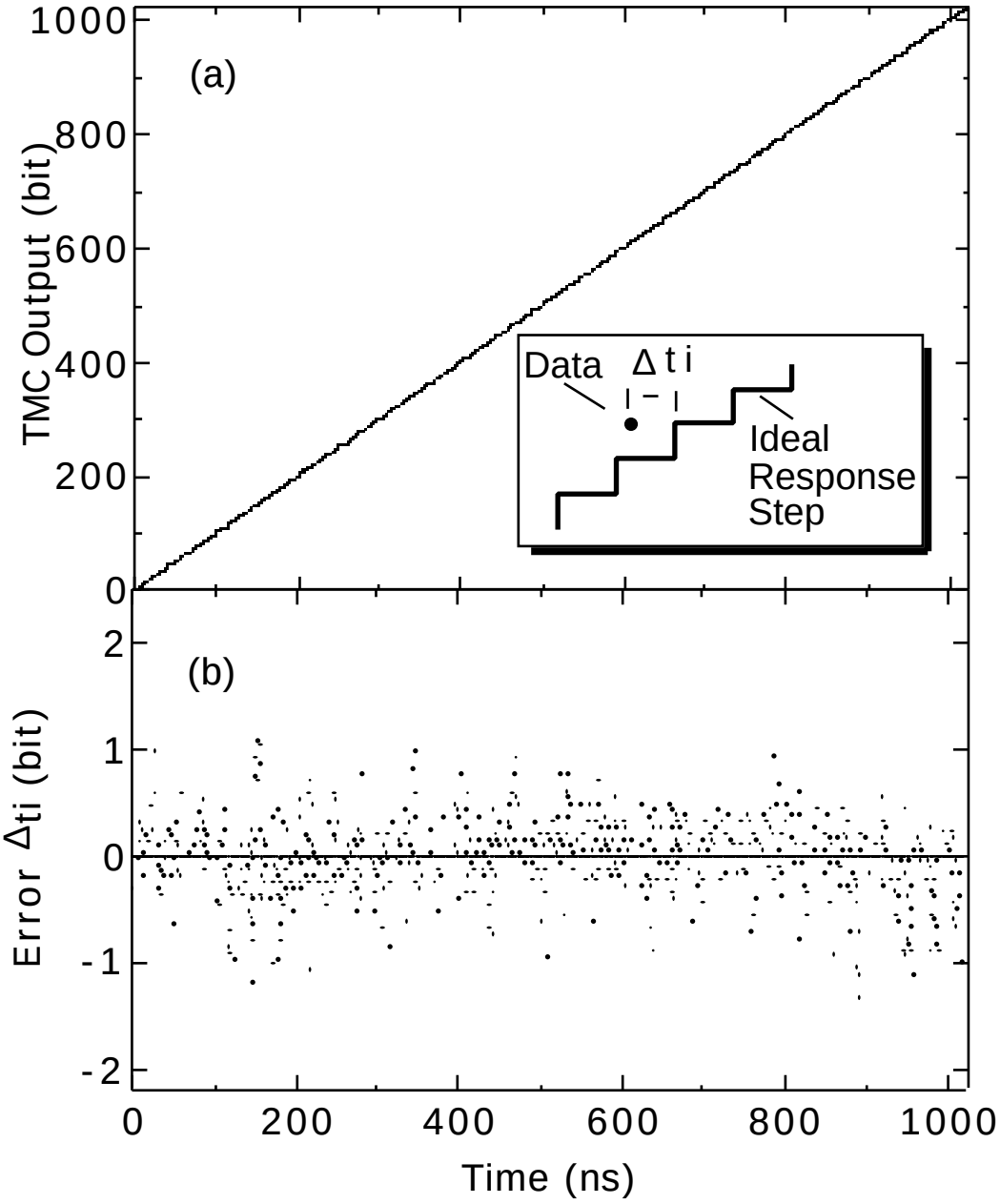


Fig. 8. (a) Linearity curve of the TMC1004. (b) Integral linearity error of the TMC1004. Data are taken for 0.61 ns step and 1672 points.

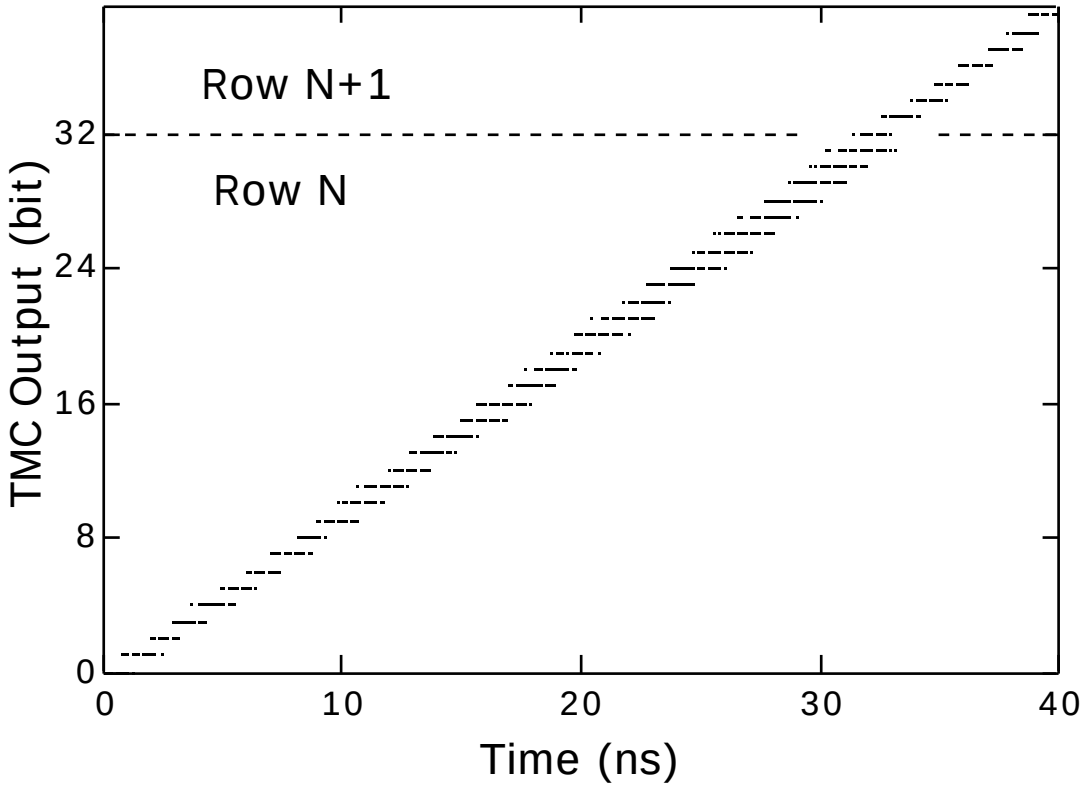


Fig. 9. Fine structure of the linearity curve. Output bits of 0 to 31 correspond to row N, and bits above 31 correspond to row N+1.

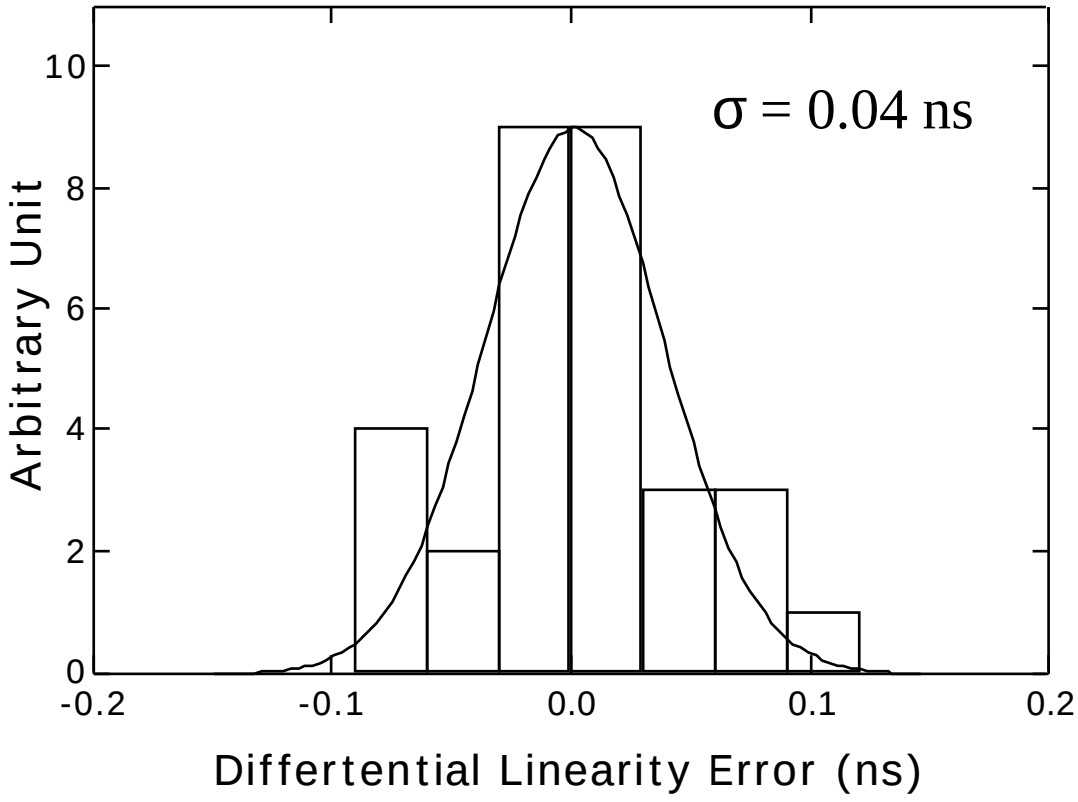


Fig. 10 Distribution of differential linearity error.

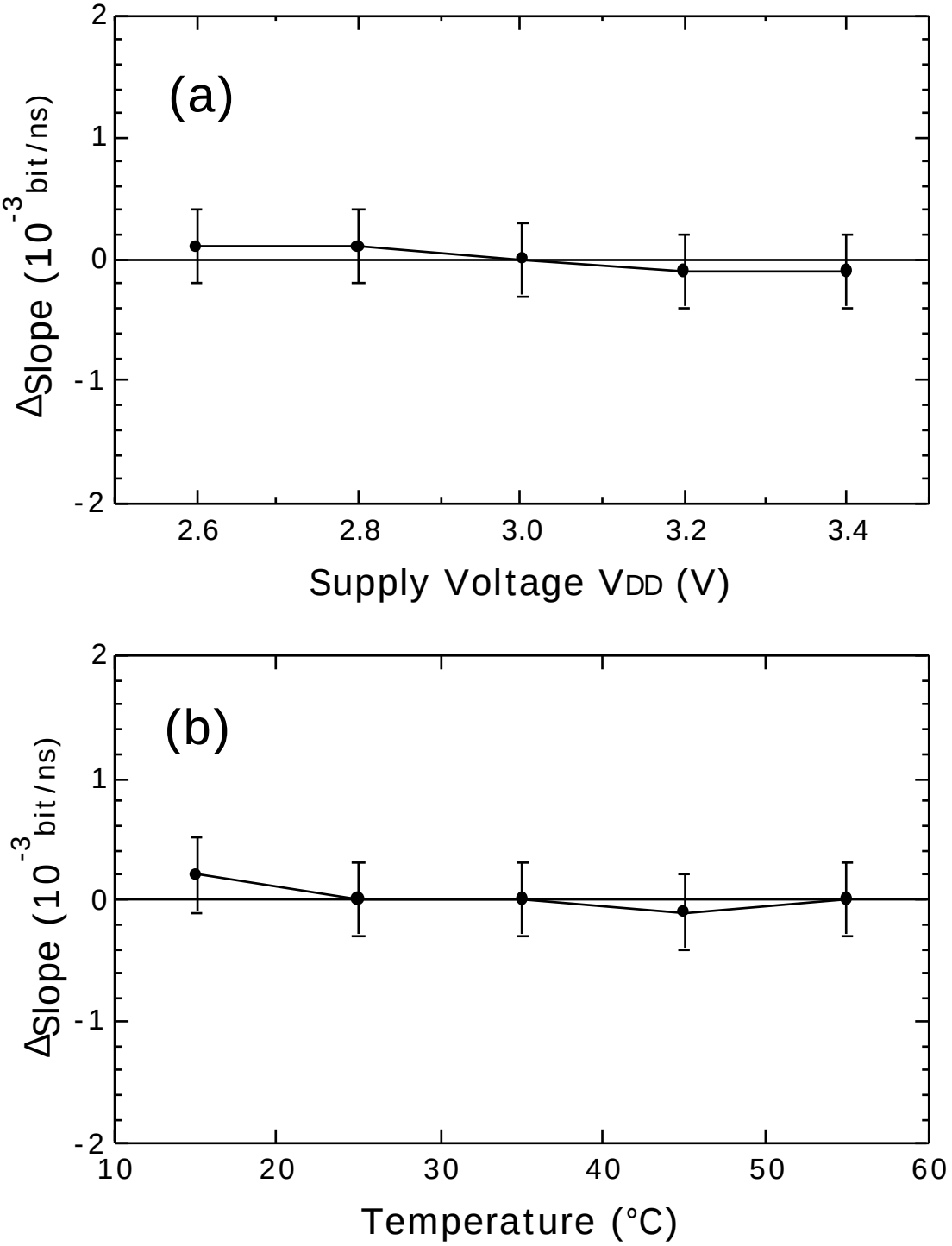


Fig. 11. (a) Slope variation for supply voltages between 2.6 V to 3.4 V. (b) Slope variation for temperature change from 15 ˚C to 55 ˚C. The data are plotted as a deviation from the data point of 3.0 V and 25 ˚C.

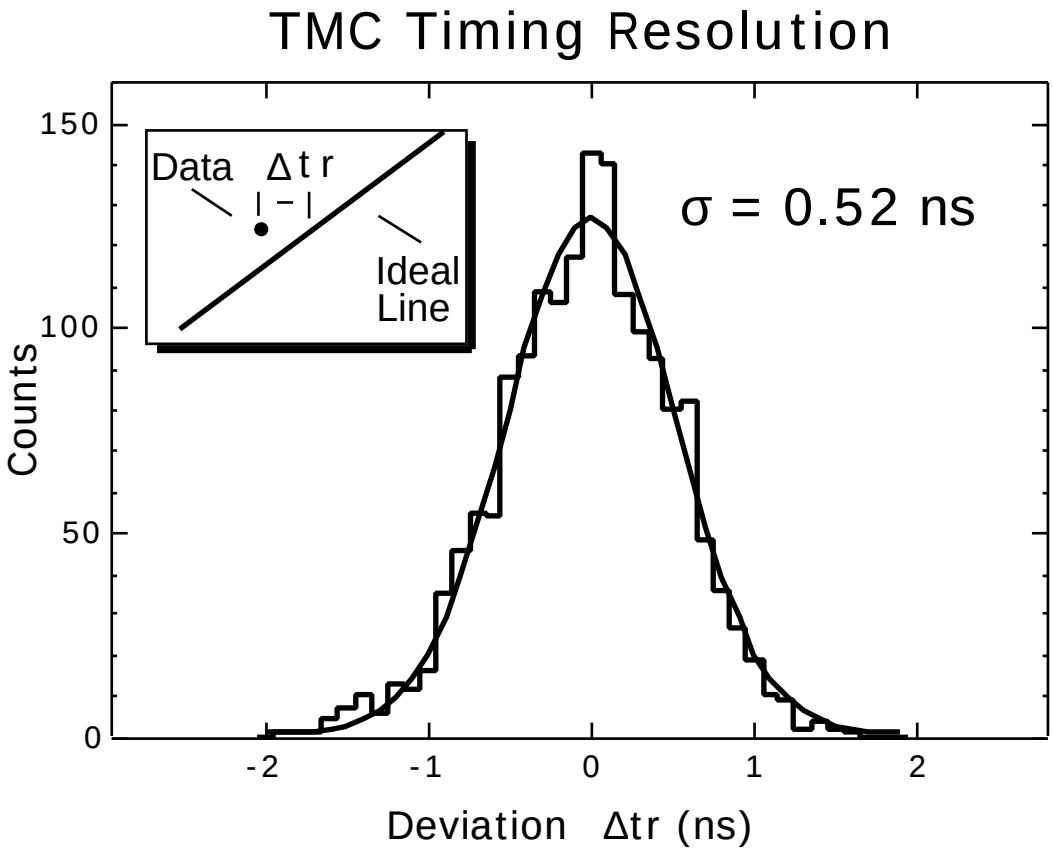


Fig. 12 Time resolution measurement. The deviation from ideal line includes both the digitization error and the TMC error.

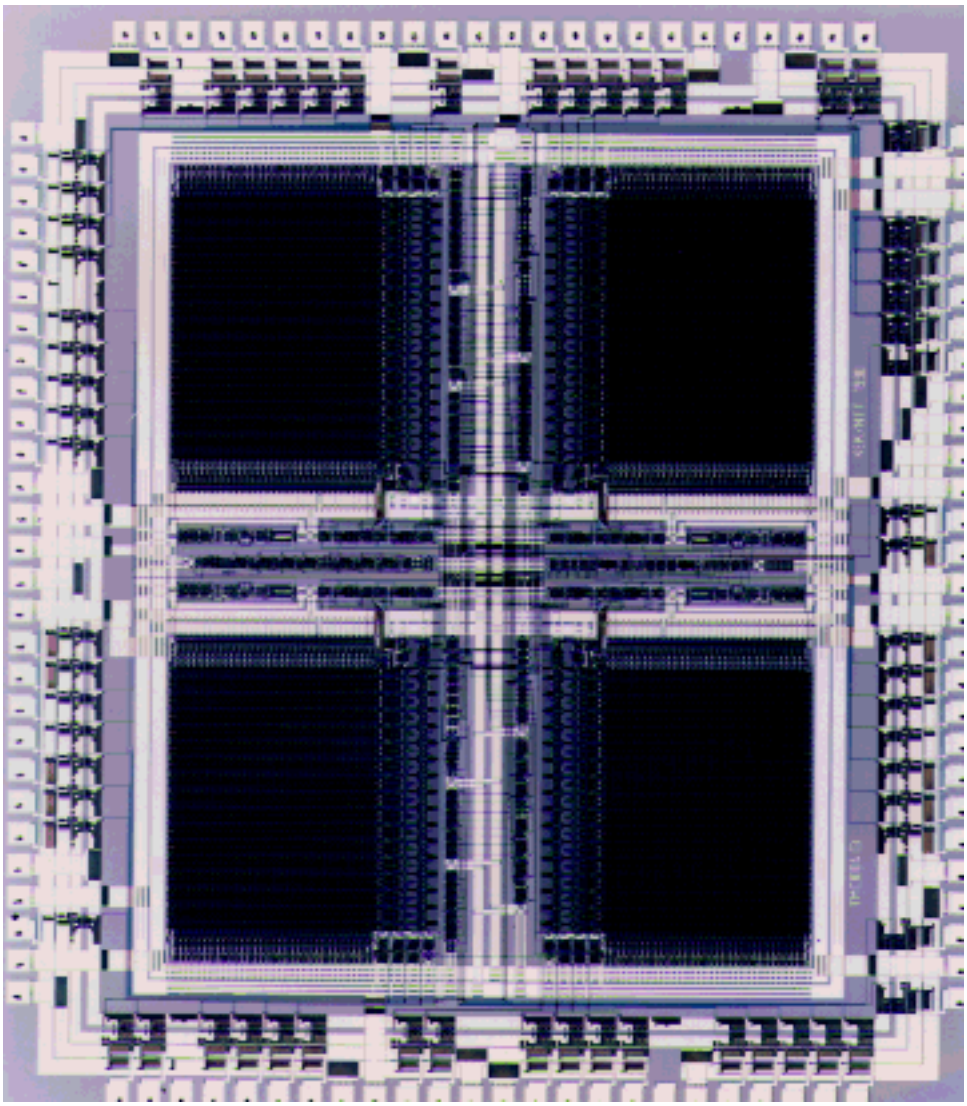


Fig. 13. Photograph of the TMC1004 chip.