Development of a CMOS Time Memory Cell VLSI and a CAMAC module with 0.5 ns resolution

Y. Arai, M. Ikeno and T. Matsumura†

KEK, National Laboratory for High Energy Physics
1-1 Oho, Tsukuba, Ibaraki 305, JAPAN
†NTT LSI Laboratories,
3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-01, JAPAN

Abstract

A CMOS time-to-digital converter chip, the Time Memory Cell (TMC), for high-rate wire chamber application has been developed. The chip has a timing resolution of 0.52 ns, dissipates only 7 mW/channel, and contains 4 channels in a chip. Each channel has 1024 memory locations which act as a buffer 1 μs deep. The chip was fabricated in a 0.8 μm CMOS process and is 5.0 mm by 5.6 mm.

Using the TMC chip, a CAMAC module with 32 input channels was developed. This module is designed to operate in both "Common Start" and "Common Stop" modes. The circuit of the module and test results are described.

I. INTRODUCTION

The development of high density electronics is vital to the success of future experiments at high energy accelerators such as the SSC (Superconducting Super Collider). Since the number of channels is very large, many VLSI chips must be mounted in the very limited space of a detector. The chip must be low-power and high-density, and must store information from the input signals for a few μs pending receipt of a readout trigger.

In the time measurement system for a drift chamber, time-to-digital converters with a resolution of less than 1 ns are required. Although a GaAs shift register clocked at 1 GHz [1] would provide the 1 ns precision, the power dissipation of this technology is unacceptably large. Therefore we sought to accomplish our objectives in CMOS technology where the power dissipation is intrinsically low.

The idea of Time Memory Cell (TMC) was initially proposed by one of us [2] and a test chip was produced [3]. Encouraged at the success of the test chip, a first useful chip (TMC1004) was designed [4]. The TMC1004 includes 4 channels of circuits and each channel has a 1024 bit time memory. One least count is 1 ns and stores 1 μs of data inside the chip. The technology used for the TMC chip is a 0.8 μm CMOS process, and about 100,000 transistors are implemented in the 5.0 mm by 5.6 mm chip area (Fig. 1). Total power consumption for a channel is about 7 mW for a 100 kHz data readout rate.

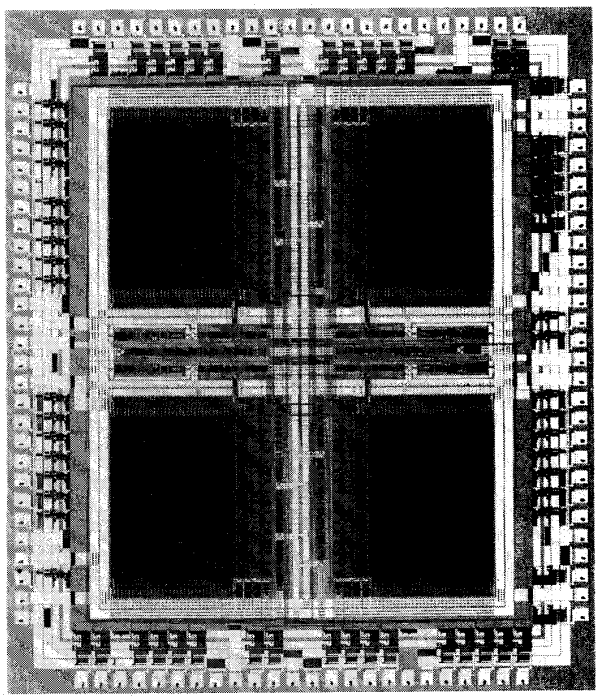


Fig.1 Photograph of the TMC1004 chip

In section II, we briefly describe the design of the TMC1004 chip. In section III, the design of a CAMAC module which uses the TMC chips is described. In section IV, the module performance and plans for the future are presented.

II. TMC CHIP

Figure 2 shows the basic operation of the TMC. As the write signal (WL) timing in each TMC cell is delayed by 1 ns, timing information of the input lines (TIN and TIN*) is recorded in the memory cells sequentially. To keep the delay time constant, the delay time of the delay element is controlled through the Vg line using a feedback circuit which is referenced to an external system clock.

A block diagram of the TMC1004 is shown in Fig. 3. The chip has four TMC arrays, each with 32 rows by 32 columns

0018-9499/92$03.00 © 1992 IEEE

of TMC cells. For accessing the four arrays, there are two pointers (Write and Read) each of which consists of 7 bit counter and decoder. The Write Pointer is incremented each clock cycle. This initiates a pulse in the write line of the designated row. The Read Pointer selects a row for readout and is incremented by the same clock. This scheme with two pointers and dual port cells enables read and write operations to proceed simultaneously.

The 32 bit row data is encoded to 6 bits at readout time. Figure 4 shows the encoding logic and the encode table. The most significant bit shows the value of the first bit of a row to detect the data transition between rows. The remaining 5 bits show the position of a "0" to "1" transition.

There is no provision for multiple transitions in a row of data using the present encode logic. Input signals must be separated by more than 32 ns by external circuitry. In the CAMAC module that we developed, a latch circuit is implemented at the input signal buffer (see section III).

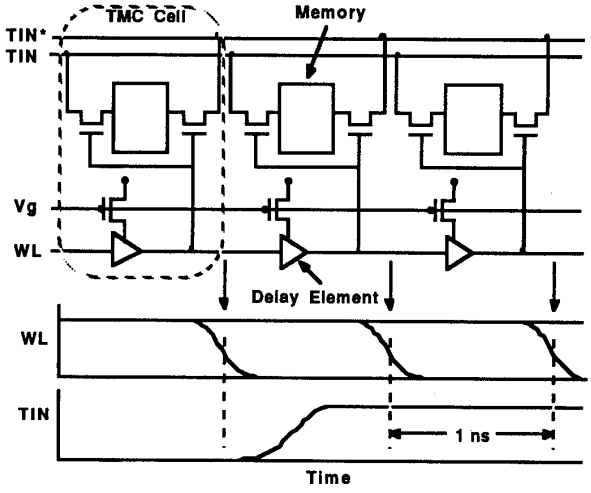


Fig. 2 Input timing write operation in the TMC cells.

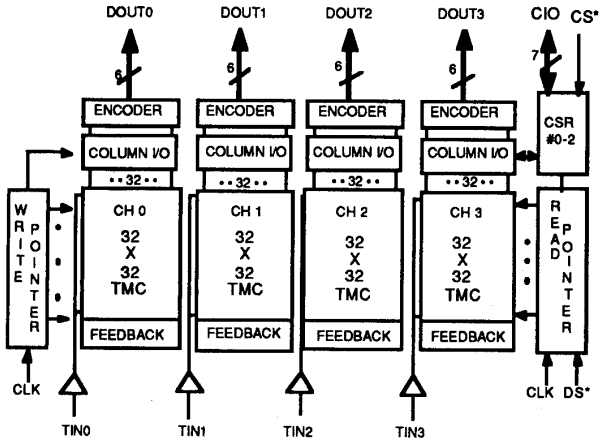
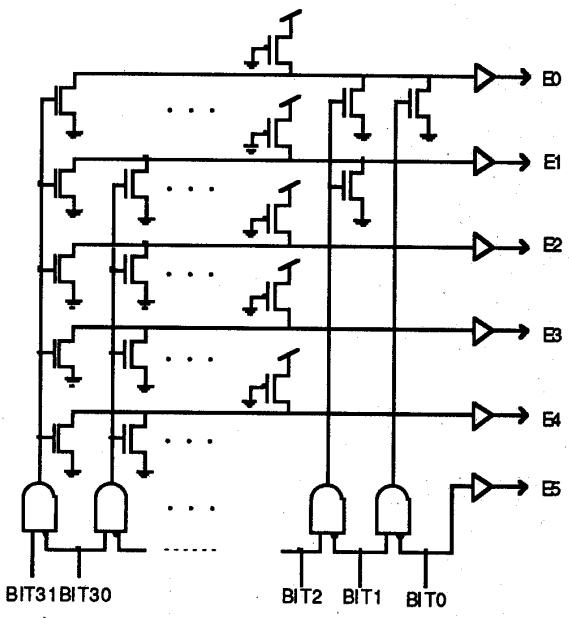


Fig. 3 Block diagram of the TMC1004.



Bit Pattern	Encoded Data
33222222222221111111111	EEEEEE
10987654321098765432109876543210	543210
00000000000000000000000000000000	000000
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10	000001
xxxxxxxxxxxxxxxxxxxxxxxxxxxx100	000010
:	:
10000000000000000000000000000000	011111
11111111111111111111111111111111	100000
(not appear)	100001
xxxxxxxxxxxxxxxxxxxxxxxxxxxxx101	100010
:	:
10xxxxxxxxxxxxxxxxxxxxxxxxxxxxx1	111111

x..xx..x = 0..01..1

Fig. 4 Circuit diagram of the encoding logic and the encode table.

III. CAMAC MODULE

A. General Description

As a test of the TMC chip, a 32-channel CAMAC TDC module was developed. Although the primary purpose of the module is to test the TMC chip, the module has powerful functions as a multi-hit TDC module. Main features of the module are listed in table 1 and a photograph of the module is shown in Fig. 5.

Figure 6 shows the block diagram of the module. The module has eight TMC1004 chips, and it can be configured as 32 channel of 1 μsec range, 16 channels of 2 μsec range, or 8 channels of 4 μsec range. For accessing the module 4 channels are treated in a group, that is, operations are done for one of eight chips. These eight chips are accessed by using CAMAC sub-address A(0) through A(7). Since the output of each

channel is 6 bits wide, four channels of data are read out at once through the 24 bit CAMAC Read lines.

Although the TMC1004 is designed for deadtimeless readout applications, the CAMAC module can not operate in deadtimeless mode because the module does not have data buffers and the CAMAC cycle is very slow compared with the input data bandwidth. Thus the module runs in "Common Start" or "Common Stop" mode selectable by internal switches. In common start mode, the signal recording will stop after a preset number of clock cycles. In common stop mode, previous data are overwritten until the stop signal is received.

Since the TMC chip encodes the position of a "0" to "1" transition point in a 32 bit row, the input signal buffer in the module latches the input signal for 32 ns in order not to create a false code. If the signal width is shorter than 32 ns, the signal is stretched to 32 ns. If the signal is longer than 32 ns, the signal pass through the buffer.

Each chip has three CSR registers. These registers are shown in Table 2 and the function of each bit is described below.

[CSR0]

- SIO3 ~ 0 : Serial I/O bits. These bits are valid only in the Serial I/O mode. One bit data for each channel is read/written through these bits from/to the address pointed to by the Read Pointer(row position) and the Write Pointer(column position) registers.

Table 1. Main features of TMC CAMAC module

Signal Inputs	32 Channel. ECL-differential.
START Input	One, common to all channels, NIM level.
STOP Input	One, common to all channels, NIM level.
One Least Time Count	1 ns/bit
Time Range	1.024 μs (32 ch), 2.048 μs (16 ch) or 4.096 μs (8 ch)
Double Hit Resolution	~32 ns
Timing Measurement Error	σ = 0.52 ns (including digitization error)
Integral Linearity Error	σ = 0.3 ns (< 1.5 bit)
Variation of Slope	< 0.1 % (15 - 55 °C)
CAMAC Commands	Z, C, X and Q
CAMAC Functions	F(0) : Read Data; F(1, 4, 6) : Read CSR0, 1, 2 F(9) : Reset F(17,20,22) : Write CSR0, 1, 2 F(25) : Start
Packaging	CAMAC 1 width module.
Power Requirement	+6 V at 1.2 A, -6V at 0.5 A.

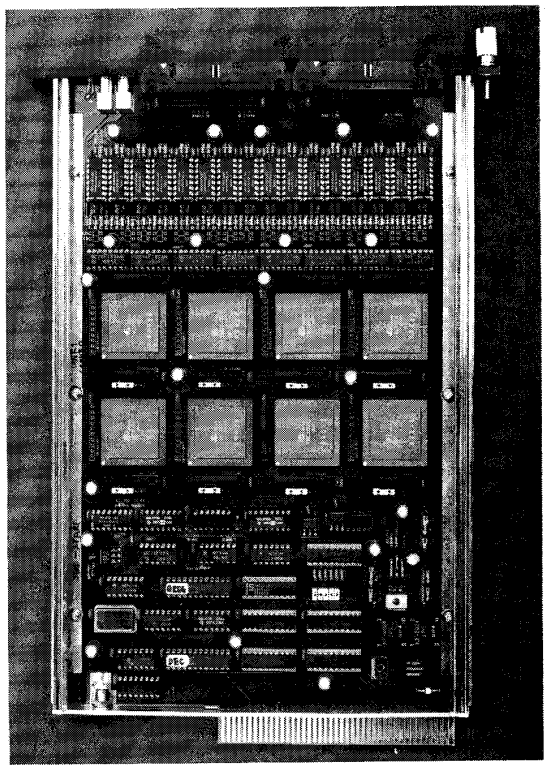


Fig. 5 Photograph of the TMC CAMAC module.

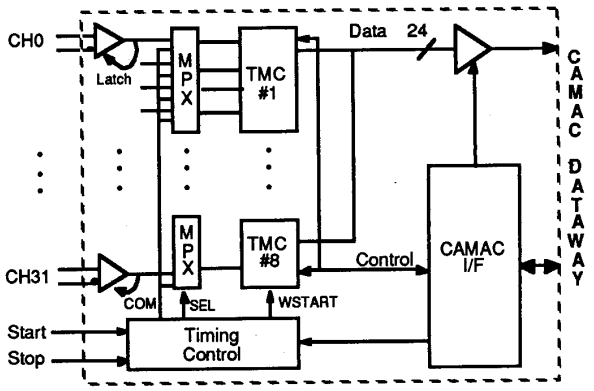


Fig.6 Block diagram of the TMC CAMAC module.

Table 2 Contents of CSR Registers

bit	6	5	4	3	2	1	0
CSR0	-	MOD1	MOD0	SIO3	SIO2	SIO1	SIO0
CSR1	Read Pointer Value						
CSR2	Write Pointer Value						

• MOD0,1 : MODE = (MOD1,MOD0)
MODE = 0 (Stand alone Mode) : Data is read out from the row indicated by the Read Pointer.
MODE = 1 (Slave Mode) : Same as the MODE=0, but the Read Pointer is automatically incremented after the readout.
MODE = 2 (Serial I/O Mode) : This mode is used mainly for testing each bit in the memory. Bit 0 corresponds to the data in the CH0 and bit 1 corresponds to CH1 and so on.

[CSR1]
The value of the Read Pointer is set through this register. The present value of the Read Pointer is read back. This register also works as a row address register in the Serial I/O mode.

[CSR2]
The value of the Write Pointer is set through this register. The present value of the Write Pointer is read back. This register also works as a column address register in the Serial I/O mode.

B. Timing Control and Data Format

The module operates in "Common Start" or "Common Stop" mode. Since the external start or stop signal is not synchronized to the internal clock, we need to record the start/stop timing in addition to the input signal timing. The actual timing of the signal is given by measuring the difference of two times. Start (Stop) timing is recorded in the first (last) 2 columns as shown in Table 3. The Start/Stop pulse has a width of about 12 ns, and can be discriminated from input signal which has a pulse width of more than 32 ns.

The circuit diagram of the timing control is shown in Fig.7. The timing diagrams of the circuit in the common start and common stop modes are shown in Fig. 8-(a) and (b) respectively.

In common start mode, an external start signal sets the flip/flop FF1. The FF1 asserts the WSTART signal which starts the time recording of the TMC, and the input multiplexer (MPX, see Fig. 6) changes to select start pulse at COM. In first 2 clock cycles, the start pulse is recorded by the TMC, and then the MPX returns to select input signals. FF1 is also set by a CAMAC function 'F25'. In this case, the WSTART is asserted synchronous to WCLK and creates a Sync Out signal. The Sync Out signal is used for test purposes. The time recording will stop after a preset time by the SW (0~8 μsec). The F579 chip starts to count clock pulses after receiving the start signal, and the F521 chip compares the counter value with the preset value. When the count reaches the preset value, FF1 is reset and WSTART is negated.

In common stop mode, the circuit is started by an external start signal or CAMAC function 'F25'. After start the input signals are recorded by the TMC chips continuously. When a stop pulse comes, FF1 is reset. The MPX changes to select the stop pulse at COM, and the pulse is recorded by the TMC. After 2 clock cycles of recording the stop pulse, the TMC will stop.

Since the operating voltage of the TMC chip is 3V and the other peripheral chips are operated at 5 V, we must be careful of the signal connections between the TMC and other ICs. As the threshold value of the TMC inputs is 1.5V and the output swing is between 0V and 3V, it is possible to connect the TMC chip to TTL devices directly. However, the output signals of some TTL devices may exceed 3V. We have added schottky diodes between each line and 3V power line to protect the TMC chip.

IV. Performance and Future Plans

The CAMAC module has worked successfully and many tests have been done. The performance that we get is summarized in table 1 and reported in detail in reference 5. Here, we will show only the final results of the timing measurement error (Fig. 9). We have defined the timing measurement error as the deviation from the ideal response line. This error includes both digitization error (σdig=0.29 ns) and TMC circuit error. We get a standard deviation of 0.52 ns from a gaussian fit to the data. This value is good enough for almost all projected high rate wire chamber system.

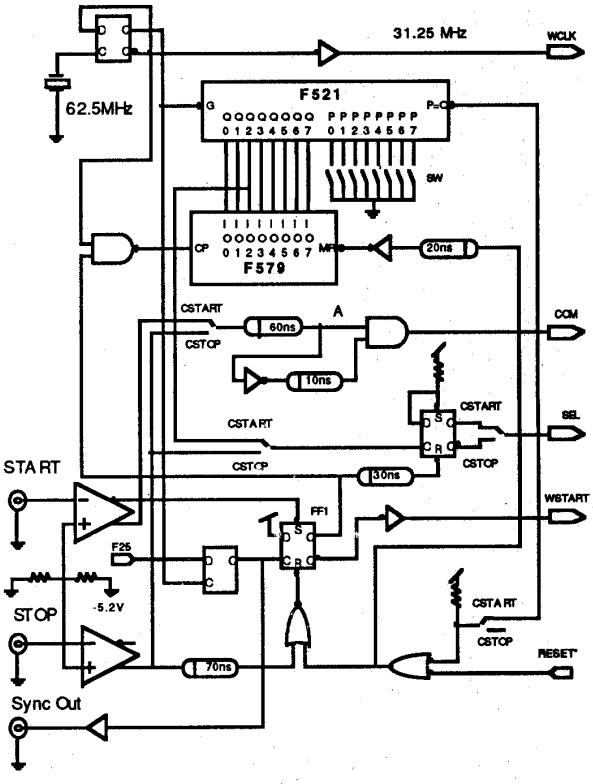


Fig. 7 Circuit diagram of the timing control circuit. Switches are set to CSTART for "Common Start" mode and CSTOP for "Common Stop" mode.

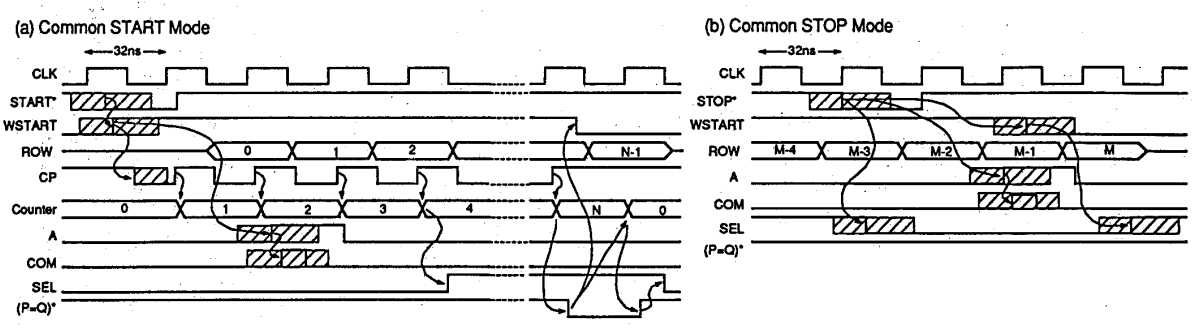


Fig. 8 (a) Timing diagram in the common start mode, and (b) common stop mode. The signal 'ROW' shows the active row into which the input signal is recorded. Other signals are indicated in Fig. 6 and 7. Hatched areas show possible signal timings which are determined by the START/STOP signal timing.

Table 3. Recorded Data area in the TMC chip.

(a) Common Start Mode

31 ... 0	
Start pulse recording area	Row N
Start pulse recording area	Row N+1
.... Input signal recording area	Row N+2
Input signal recording area	Row N+3
:	:
Input signal recording area	Row N+31

(N = Initial Value of the Write Pointer.)

(b) Common Stop Mode

31 ... 0	
Input signal recording area	Row M-32
Input signal recording area	Row M-31
:	:
Input signal recording area	Row M-3
Stop pulse recording area	Row M-2
Stop pulse recording area	Row M-1

(M = Final Value of the Write Pointer.)

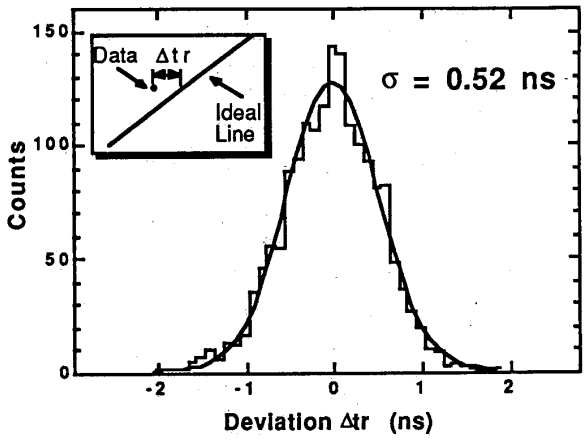


Fig. 9 Timing measurement error of the TMC1004. The data are taken by using the CAMAC module.

The power consumption of the module is very low (~10W), in spite of its high-density and powerful functions.

We are also planning to develop a CAMAC module which has data buffers and a Digital Signal Processor. By implementing the data buffer and reading out the TMC with at the same speed as data is written, the time range of recording may be extended greatly.

There are many plans to improve the performance of the TMC chip; increase the memory size, reduce the cell area of a time memory, improve the timing resolution, and so on. In addition to these improvements, the radiation hardness of the chip is now being intensively studied.

IV. REFERENCES

[1] O. Sasaki et al., "1.2 GHz GaAs Shift Register IC for Dead-Time-Less TDC Application", IEEE Trans. on Nucl. Sci. Vol. 36 (1989)512.

[2] S. Kleinfelder et al., "MTD132 - A New Sub-Nanosecond Multi-hit CMOS Time to Digital Converter", IEEE Trans. on Nucl. Sci. Vol. 38, No.2, (1991)97.

[3] Y. Arai and T. Ohsugi; "An Idea of Deadtimeless Readout System by Using Time Memory Cell", Proceedings of the Summer Study on the Physics of the Superconducting Supercollider, Snowmass, (1986)455.

[4] Y. Arai and T. Ohsugi; "TMC - A CMOS Time to Digital Converter VLSI", IEEE Trans. on Nucl. Sci., Vol. 36, No.1 (1989)528.

[5] Y. Arai, T. Matsumura, and K. Endo, "A CMOS 4CH x 1K Time Memory LSI with 1 NS/Bit Resolution", to be published in IEEE Journal of Solid State Circuits, March 1992.