TMC-TEG5 User's Manual

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TMC-TEG5 is a low-power and high-resolution multi-hit Time-to-Digital Converter LSI produced with Toshiba's 0.5 µm CMOS Sea-of-Gate Technology. Input signals are digitized at TMC (Time Memory Cell) circuits in (clock period)/32 (0.78 ns @40MHz) time bin. The 32 bits output of the TMC are divided into two 16 bits data, and each 16 bits data are encoded into 2 hit tag bits and 4-bit data. Then the data are written to a dual port memory. The write and read operation can be performed at the same time and there is no dead time of data conversion. There are 256 words of dual port memories, and the chip can store data of 6.4 µs period at 40 MHz clock.

To stabilize the internal delay element, PLL circuit is used. User can select 10 - 50 MHz system clock (x1 mode) or 2.5 - 12.5 MHz clock (x4 mode). There are 8 Control and Status Registers (CSRs) which can be read and write through an 8-bit control bus. The package of the chip is 100 pins QFP with 0.8 mm lead pitch. Present TMC-TEG5 chip has implemented 2 channels, but the pin assignment is determined to accomodate 4 input channels for future extension.

MAIN FEATURES

• Least Time Count	: 0.6 - 3.1 ns/bit
• Time Resolution	: RMS = 250 ps (@40 MHz)
• Integral Linearity Error	: < 80 ps @40MHz
• Differential Linearity Error	: < 60 ps @40MHz
• Stability	: (3.0 - 3.6 V. 0 - 70 ˚C)
• System Clock Frequency	: 10 - 50 MHz (x1 mode) 2.5 - 12.5 MHz (x4 mode)
• No. of Channels	: 2 Channels
• Recording depth	: 256 clock cycle (5 - 25 µs)
• Double Hit Resolution	: <12.5 - 16 ns
• Readout mode	: Synchronous or Asynchronous read mode
• Data format	: dual edge encode (2 hit tag + 4 bit)
• Supply Voltage	: 3.3 V
• Process	: 0.5 µm CMOS Sea-of-Gate
• Power Dissipation	: ~ ? mW/Channnel
• Package	: 0.8 mm lead pitch, 100 pin plastic QFP

PIN DESCRIPTION

[I = Input, DI = Differential Input, O = Normal Output, TO = Three State Output; OD = Open drain output, PU = with internal pull-up resistor, PD = with internal pull-down resistor, * = negative logic]

TMC pins

- EDCLK [I] : When this signal is High level, CLKP/CLKN pins are connected to a differential input receiver. When this signal is Low level, the CLKP pin is connected to a single ended input buffer and the CLKN is disconnected from the internal circuit.

- CLKP,CLKN [DI/I] : System clock inputs. In a differential input mode, CLKP act as a non-inverting input and CLKN act as a inverting input. In a single end mode, CLKP pin is used as a system clock input.

- DIV4 [I] : Divide by 4 selection. When this signal is high, the the internal oscillation clock is divided by 4 before the phase compartor of the PLL. Thus the internal clock frequency has 4 times higher frequency of the external clock (CLKP/CLKN).

- RST1* [I] : This input pin is used to reset all the internal circuit. When thei signal is asserted, internal registers, sequencers, and the output FIFOs are initialized. The PLL circuit does not be affected in the reset operation when DIV4 is low. When “divide by 4” mode is selected (DIV4=High), phase lock is lost at the reset.

- RST2* [I] : This input pin is used to reset sequencers and the output FIFOs. All other circuit such as CSR’s and PLL are not affected.

- CIO0~CIO7 [I,TO] : These I/O pins are data lines for control bus which read and write the CSR registers.

- CS* [I] : This signal is a strobe signal for the control bus.

- RA0~2 [I] : These pins are used as address line to the control bus.

- WR* [I] : This pin is a Read/Write* select signal in the control bus.

- ED [I] : When this signal is High level, TINxP/TINxN (x=0..3) pins are connected to a differential input receiver. When this signal is Low level, the TINxP pin is connected to a single ended input buffer and the TINxN pin is disconnected from internal circuit.

- TIN0P ~ TIN1P,TIN0N~1N [DI/I] : Inputs for time measuring signals. In differential input mode, TINxP act as a non-inverting input and TINxN act as a inverting input. In single end mode, TINxP is used for the input of clock.

- TIN2P ~ TIN3P,TIN2N~3N [DI/I] : These pins are dummy for future use. The pins are connected to differential receivers and the outputs of the receiver are available at VGN2-3 pins.

- D0 ~ D11 [TO] : These signals are data output lines. The three-state output buffer is controlled by OE* signal.

- OE* [I] : This input controls the three-state output buffers of D0 ~ D11 and CH0 ~ CH1. When OE* is asserted those output buffers are enabled as shown below. When OE* is negated, those outputs have high impedance.

OE*	SYNCMOD	UPBYTE	D0 ~ D5	D6 ~ D11	CH0 ~ CH1
1	x	x	Hi Z	Hi Z	Hi Z
0	0 (async)	0	Lower Byte	Upper Byte	Ch No. Input
		1	Upper Byte	Upper Byte	Ch No. Input
0	1 (sync)	x	Lower Byte	Upper Byte	Ch No. Output

• SYNCMOD [I] : Set mode to a synchronous mode.

• UBYTE [I] : Select upper byte data in an asynchronous mode.

• CH0 [I/TO] : Bit 0 of the channel number. In an asynchronous mode, the output channel is selected by this signal. In a synchronous mode, this signal indicates present channel number.

• CH1 [I/TO] : This pin is a dummy pin for future use.

• WSTART [I] : This signal starts write cycle of the TMC.

• WRUN [O] : This signal indicates the start of the write cycle in the TMC. This is a synchronized signal with the system clock.

• TRIG [I] : Trigger signal. When this signal is asserted, the read pointer address which is write pointer value minus a offset value is stored into the trigger FIFO.

• TRIGOUT [O] : This signal indicates the receive of the TRIG signal. This is a synchronized signal with the system clock.

• RRUN [O] : This signal indicates the start of the readout sequencer. When this signal is asserted, readout from the duakl port memory to the output FIFO is going.

• VGN0-VGN1 [O] : These pins are outputs of PLL loop filter, and must be connected to external capacitors of 6800 pF.

• VGN2-VGN3 [O] : These pins are dummy for future use. At present, these pins are connected to the outputs of channel 2 and 3 differential receivers at CALEN=0. When CALEN=1, the signal of the CALIN will appear in these pins.

• ENOSC [I] : Enable PLL oscillation.

• OSCOUT [O] : PLL oscillation output. Output of the channel 0 PLL clock is available through this pin.

• OCLK [I] : Input pin of the output clock.

• RE* [I] : Read enable signal.

• EMPFLG* [O] : Empty Flag.

• EVEND* [O] : Event end signal.

• DVALID* [O] : Data valid signal.

• ERR* [OD] : Error signal. This is a open drain output, so an external pull-up resistor is needed. If the trigger FIFO or the output FIFO becomes full, this signal is asserted. This signal is cleared by writing 0 to the bit 4 or 5 of the CSR6, or by the reset.

• ORUN [O] : This signal indicates the status of the output sequencer. When this signal is asserted, output operation is going.

- CALEN [I] : Calibration input enable signal.
- CALIN [I] : CAlibration signal input. When CALEN is high level, this signal is applied to all 4 channels.

Test purpose pins (expert only)

[Following pins are used for test purpose. Normal user can leave those pins open.]

- DEBUG [I] : Enabele debug purpose signals.
- RP0-RP2 [TO] : These pins indicate lower 3 bits of the Read Pointer. This signal is enable by the DEBUG signal.
- WP0-WP2 [TO] : These pins indicate lower 3 bits of the Write Pointer. This signal is enable by the DEBUG signal.
- FRA0-FRA2 [TO] : These pins indicate lower 3 bits of the read address of the output FIFO. This signal is enable by the DEBUG signal.
- FWA0-FWA2 [TO] : These pins indicate lower 3 bits of the write address of the output FIFO. This signal is enable by the DEBUG signal.
- TCLKEN [I] : Clock test enable. When this signal is enabled, the systemclock signal is applied to internal circuit instead of the PLL clock.
- TSTROSC [I] : Enable RTMC test. When this signal is asserted, RTMC output select by DCH0 and 1 is connected to ROSC pin, and its signal is also supplied to the read pointer.

CSR Registers

CSR registers bit assignment

<table>
<tr><td>bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CSR0</td><td colspan="8">Offset Register [OFR]
(R/W:128)</td></tr>
<tr><td>CSR1</td><td colspan="8">Read Pointer Register [RPR]
(R:0)</td></tr>
<tr><td>CSR2</td><td colspan="8">Write Pointer Register [WPR]
(R/W:0)</td></tr>
<tr><td>CSR3</td><td colspan="8">Count Preset Register [CPR]
(R/W:20)</td></tr>
<tr><td>CSR4</td><td colspan="8">Event Number Register [ENR(7:0)]
(R/W:0)</td></tr>
<tr><td>CSR5</td><td>TSTENR
(R/W:0)</td><td>NOENR
(R/W:0)</td><td>-
(R:0)</td><td>-
(R:0)</td><td colspan="4">[ENR(11:8)]
(R/W:0)</td></tr>
<tr><td>CSR6</td><td>SHIFT
(R/W:0)</td><td>MTEST
(R/W:0)</td><td>OFIFUL
(R/W:0)</td><td>TFIFUL
(R/W:0)</td><td>-
(R/W:0)</td><td>TCH1
(R:0)</td><td>TCH0
(R/W:0)</td><td>SELH
(R/W:0)</td></tr>
<tr><td>CSR7</td><td>SOUT
(R:0)</td><td>SIN
(R/W:0)</td><td colspan="6">Test Data Register [TDR]
(R/W:0)</td></tr>
</table>

(Readable/Writable : Initial value)

* CSR0 : Offset Register

- OFR [read/write] : When trigger signal is arrived, this offset value is subtracted from the Write Pointer value, and the result is stored into the trigger FIFO.

* CSR1 : Read Pointer Register

- RPR [read]: Read pointer is a 8-bit up counter which outputs are a addresses of the read port of the Dual Port Memory (DPM). The value of the register is copied from the trigger FIFO when the readout sequence starts.

* CSR2 : Write Pointer Register

- WPR [read/write]: Write pointer is a 8-bit up counter which outputs are a addresses of the write port of the Dual Port Memory (DPM). The write pointer is set through this register and read back present value of the write pointer.

* CSR3 : Count Preset Register

- CPR [read/write]: Set number of data (excluding header) to be written to the output FIFO when a trigger signal is received.

* CSR4 & 5 : Event Number control

- ENR [read/write]: Event Number Register. This 12 bits register keeps a event number. The event numver is written to the header of the data, and incremented for each trigger signal.

- NOENR [read/write] : When this bit is set, the event number is not added to the data.

- TSTENR [read/write] : Test the ENR register. When this bit is set, the ENR value is incremented by PLL clcok or the system clock selecte by the TCLKEN.

* CSR6 : Miscellaneous control.

- SELH [read/write]: Test data select, =0 Lower Part, =1 Higher Part.
  At MTEST=1, SELH=1, Data written to the DPM bit 6-11 will be inverted.

- TCH0~1 [read/write]: Test channel select. TCH = [TCH1,TCH0].

- MTEST[read/write] : Memory Test select. When this bit is set, output of the Test Data Register (TDR) is connected to the input of the DPM and the input of TDR is connected to the output of encoder logic selected by TCH bits and F/R* bit.

- SHIFT [read/write] : Enable Shift In/Out. When this bit is set, the value of the SIN bit is shifted into the encode register which is selected by TCH bits at the end of CSR7 read/write operation.

* CSR7 : Test register.

- TDR [read/write]: Test Data Register.

- SIN [read/write] : Serial Input bit.

- SOUT [read only] : Serial output bit.

Data Encoding Scheme

Digitized data is stored at the dual port memory after data encoding. The data encoding scheme is shown in the following table . Bit position at which the data is changed from "0" to "1" is encoded in the rising edge data, and bit position of "1" to "0" is encoded in the falling edge data. Hit tag bit shows the existence of those transition.

In addition to the transition encoding, user can get all "0" or all "1" information by taking the encoded data at no hit tag. This may help more understanding of the signal behavior.

Table. Data Encoding Scheme

row data bit										Flag [D5,4]	[D3..0] Encoded	Comment
0 (16	1 17	2 18	3 19	..		..	14 30	15 31	16 next 0)	F R	Data	
0	0	0	0	•	•	•	0	0	0	0 0	0	all 0
1	1	1	1	•	•	•	1	1	1	0 0	1	all 1
0	1	1	1	•	•	•	1	1	1	0 1	0	R edge at 0-1
0	0	1	1	•	•	•	1	1	1	0 1	1	R edge at 1-2
:	:	:	:	:	:	:	:	:	:	:	:	
0	0	0	0	•	•	•	0	1	1	0 1	E	R edge at 14-15
0	0	0	0	•	•	•	0	0	1	0 1	F	R edge at 15-16
1	0	0	0	•	•	•	0	0	0	1 0	0	F edge at 0-1
1	1	0	0	•	•	•	0	0	0	1 0	1	F edge at 1-2
:	:	:	:	:	:	:	:	:	:	:	:	
1	1	1	1	•	•	•	1	0	0	1 0	E	F edge at 14-15
1	1	1	1	•	•	•	1	1	0	1 0	F	F edge at 15-16
0	1	f	f	•	•	•	f	f	f	1 1	0	R edge at 0-1 (F exist)
f	0	1	f	•	•	•	f	f	f	1 1	1	R edge at 1-2 (F exist)
:	:	:	:	:	:	:	:	:	:	:	:	
f	f	f	f	•	•	•	0	1	f	1 1	E	R edge at 14-15(F exist)
f	f	f	f	•	•	•	f	0	1	1 1	F	R edge at 15-16(F exist)

f..f = There exist a falling edge in this part.

Output Data Format

D11 D10	D9 . . . D6	D5 D4	D3 . . . D0
	Data High (Late Time)		Data Low (Early Time)
Ftag Rtag	Data	Ftag Rtag	Data

Output Data sequence (UPBYTE=0)

CH	D11 .. D0
0	Ch 0 Event Number (*)
0	Ch 0 Data 1
0	Ch 0 Data 2
0	:
0	Ch 0 Data N
1	Ch1 Event Number (*)
1	Ch 1 Data 1
1	Ch 1 Data 2
1	:
1	Ch 1 Data N

(*) Inserted at NOENR=0.

Output Data sequence (UPBYTE=1)

CH	D5 .. D0
0	Ch 0 Event Number LSB(*)
0	Ch 0 Event Number MSB(*)
0	Ch 0 Data 1 Low
0	Ch 0 Data 1 High
0	:
0	Ch 0 Data N Low
0	Ch 0 Data N High
1	Ch1 Event Number LSB(*)
1	Ch1 Event Number MSB(*)
1	Ch 1 Data 1 Low
1	Ch 1 Data 1 High
1	:
1	Ch 1 Data N Low
1	Ch 1 Data N High

(*)Inserted at NOENR=0.