TMC-PHX1 Electrical Specification

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(Please also reffer to “TMC-PHX1 architecture manual”.)

1.PIN DESCRIPTION

[I = Input, DI = Differential Input, O = Normal Output, TO = Three State Output; OD = Open drain output, PU = with internal pull-up resistor, PD = with internal pull-down resistor, * = negative logic]

1.1. Normal pins

- EDCLK [I] : When this signal is High level, CLKP/CLKN pins are connected to a differential input receiver. When this signal is Low level, the CLKP pin is connected to a single ended input buffer and the CLKN is disconnected from the internal circuit.
- CLKP,CLKN [DI/I] : System clock inputs. In a differential input mode, CLKP act as a non-inverting input and CLKN act as a inverting input. In a single end mode, CLKP pin is used as a system clock input.
- DIV4 [I] : Divide by 4 selection. When this signal is high, the the internal oscillation clock is divided by 4 before the phase compartor of the PLL. Thus the internal clock frequency has 4 times higher frequency of the external clock (CLKP/CLKN).
- RST1* [I] : All reset. This input pin is used to reset all the internal circuit. When this signal is asserted, all internal registers, sequencers, and the output FIFOs are initialized. The PLL circuit also be cleared so the lock will be lost.
- RST2* [I] : Data transffer reset. This input pin is used to reset sequencers and the output FIFOs only. All other circuit such as CSR's and PLL are not affected.
- CIO0~CIO7 [I,TO] : These I/O pins are data lines for control bus which read and write the CSR registers.
- CS* [I] : This signal is a strobe signal for the control bus.
- RA0~2 [I] : These pins are used as address line to the control bus.
- WR* [I] : This pin is a Read/Write* select signal in the control bus.
- ED [I] : When this signal is High level, TINxP/TINxN (x=0..3) pins are connected to a differential input receiver. When this signal is Low level, the TINxP pin is connected to a single ended input buffer and the TINxN pin is disconnected from internal circuit. (Fig. 1)
- TIN0P ~ TIN3P,TIN0N~3N [DI/I] : Inputs for time measuring signals. In differential input mode, TINxP act as a non-inverting input and TINxN act as a inverting input. In single end mode, TINxP is used for the input of clock. (Fig. 1)
- CALEN [I] : Calibration input enable signal. (Fig. 1)
- CALIN [I] : CAlibration signal input. When CALEN is high level, this signal is applied to all 4 channels. (Fig. 1)

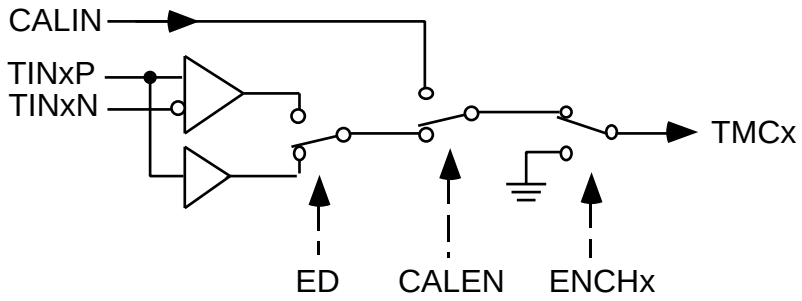


Fig. 1 Data input chain. ENCHx is a bit in CSR7.

- OE* [I] : This input controls the three-state output buffers of D0 ~ D9 and CH0 ~ CH1. When OE* is asserted those output buffers are enabled as shown below. When OE* is negated, those outputs have high impedance.
- SYNCMOD [I] : Set mode to a synchronous mode.
- CH0 - CH1 [I/TO] : Bit 0 of the channel number. In an asynchronous mode, the output channel is selected by this signal. In a synchronous mode, this signal indicates present channel number.
- D0 ~ D9 [TO] : These signals are data output lines. The three-state output buffer is controlled by OE* signal.

Asynchronous mode (SYNCMOD=0) output control.

input		output
OE*	CH	D00 ~ D09
1	x	Hi Z
0	0	Ch0 data
0	1	Ch1 data
0	2	Ch2 data
0	3	Ch3 data

Synchronous mode (SYNCMOD=1) output control.

input	output	
OE*	CH	D00 ~ D09
1	Hi Z	Hi Z
0	Ch No.	Data

- WSTART [I] : This signal starts write cycle of the TMC.
- WRUN [O] : This signal indicates the start of the write cycle in the TMC. This is a synchronized signal with the system clock.
- TRIGS [I] : Trigger signal. When this signal is asserted, the read pointer address which is write pointer value minus a offset value is stored into the trigger FIFO.
- TRIGD [I] : Trigger signal. When this signal is asserted, the read pointer address which is write pointer value minus a offset value is stored into the trigger FIFO.

- TRIGC [I] : Trigger signal. When this signal is asserted, the read pointer address which is write pointer value minus a offset value is stored into the trigger FIFO.
- TRIGOUT [O] : This signal indicates the receive of the TRIG signal. This is a synchronized signal with the system clock.
- RRUN [O] : This signal indicates the start of the readout sequencer. When this signal is asserted, readout from the duakl port memory to the output FIFO is going.
- VGN0-VGN3 [O] : These pins are outputs of PLL loop filter, and must be connected to external capacitors of 6800 pF.
- ENOSC [I] : Enable PLL oscillation.
- OSCOUT [O] : PLL oscillation output. Output of the PLL clock is available through this pin. Channel is selected by TCH bits (CSR7).
- OCLK [I] : Input pin of the output clock.
- RE* [I] : Read enable signal.
- EMPFLG* [O] : Empty Flag.
- EVEND* [O] : Event end signal.
- DVALID* [O] : Data valid signal.
- ERR* [OD] : Error signal. This is a open drain output, so an external pull-up resistor is needed. If the trigger FIFO or the output FIFO becomes full, this signal is asserted. This signal is cleared by writing 0 to the bit 4 or 5 of the CSR6, or by the reset.
- ORUN [O] : This signal indicates the status of the output sequencer. When this signal is asserted, output operation is going.
- TFIFUL [O] : Trigger FIFO full signal.
- RPUP [I] : Increment Read Pointer.
- RCKSEL [I] : Read sequencer clock selection.
  RCKSEL=0 : same frequency as the system clock.
  RCKSEL=1 : half frequency of the system clock.
- TSTPLL [I] : Test PLL circuit. Normally connected to GND.

1.2. Test pins

Following pins are used for test purpose. Normal user can leave those pins open.

- ENTSIG [I, PD] : Enabele test signals.
- RP0-RP2 [TO] : These pins indicate lower 3 bits of the Read Pointer. This signal is enable by the DENTSIG signal.

• WP0-WP2 [TO] : These pins indicate lower 3 bits of the Write Pointer. This signal is enable by the ENTSIG signal.

• FRA0-FRA2 [TO] : These pins indicate lower 3 bits of the read address of the output FIFO. This signal is enable by the ENTSIG signal.

• FWA0/ENR5-FWA2/ENR7 [TO] : This signal is enable by the ENTSIG signal. These pins indicate lower 3 bits of the write address of the output FIFO when TSTPLL=0. These pins are also used for PLL check (TSTPLL=1).

• TCLKEN [I, PD] : Clock test enable. When this signal is enabled, the systemclock signal is applied to internal circuit instead of the PLL clock.

• TESTI [I, PD] : Test Input Buffer.

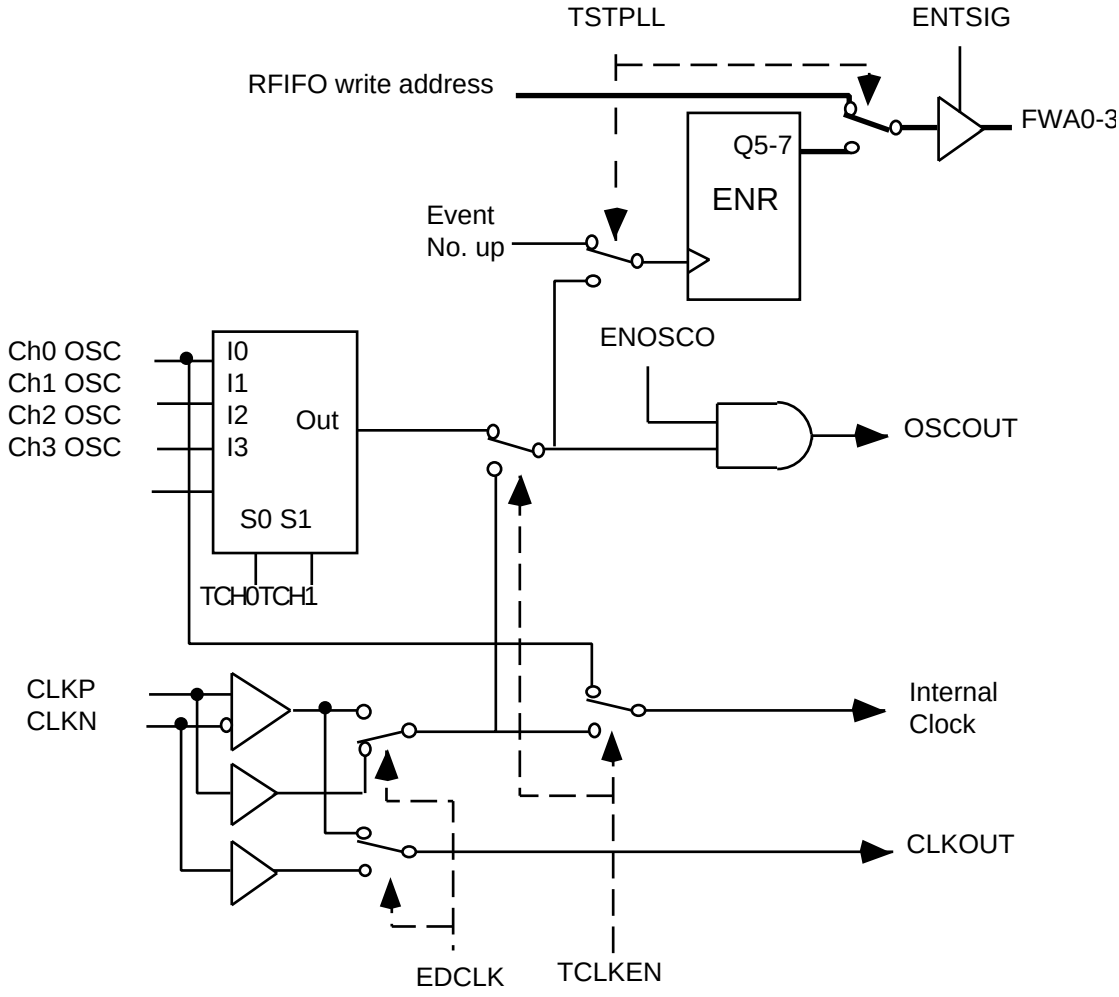


Fig. 2. Clock and oscillation select path. Signals of ENOSCO, TCH0 and 1 come from CSR7.

2.TMCPHX1 Pin Assignments

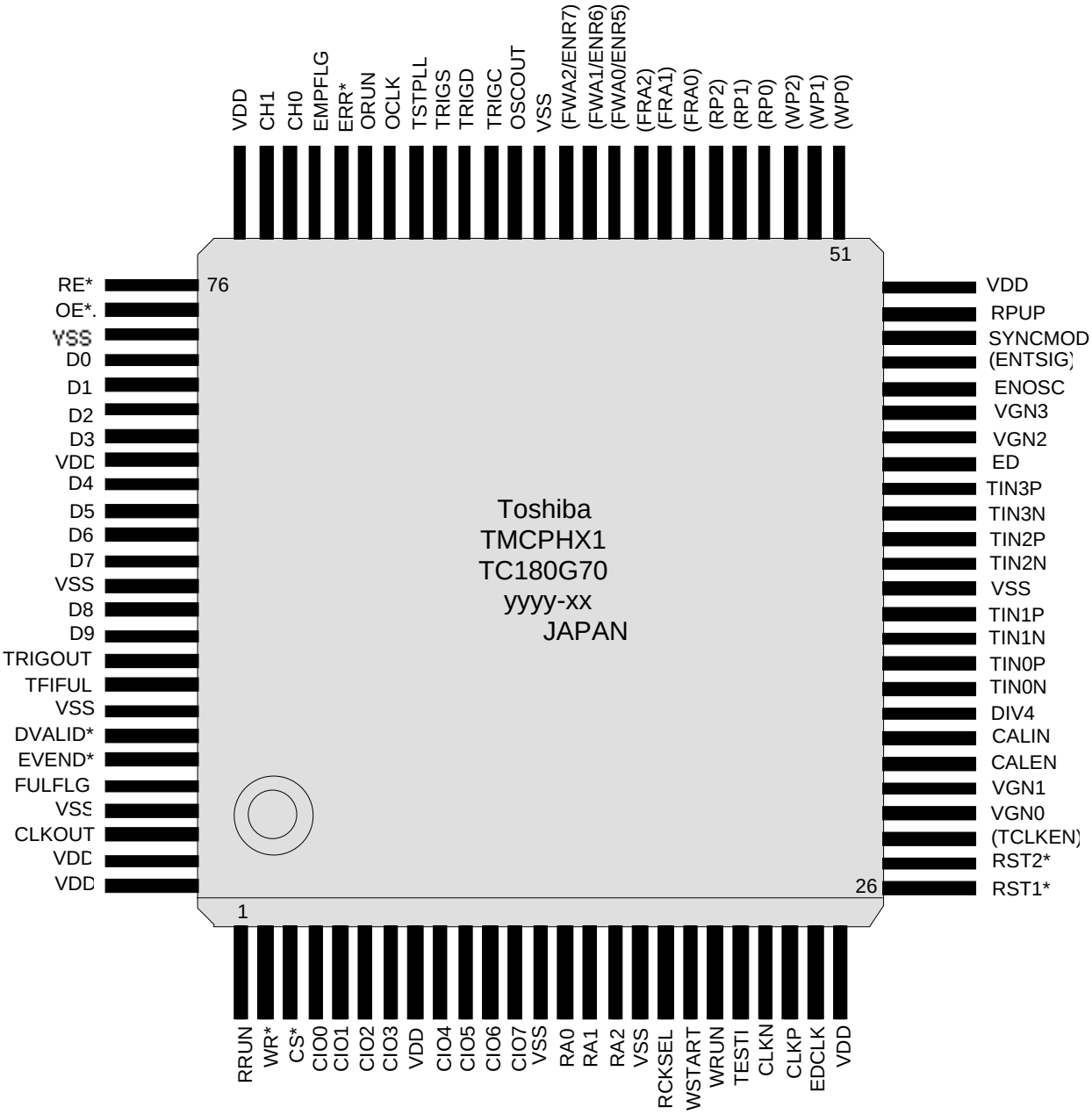
()=Test Signals(leave open).

Pin No	Signal Name
1	RRUN
2	WR*
3	CS*
4	CIO0
5	CIO1
6	CIO2
7	CIO3
8	VDD
9	CIO4
10	CIO5
11	CIO6
12	CIO7
13	VSS
14	RA0
15	RA1
16	RA2
17	VSS
18	RCKSEL
19	WSTART
20	WRUN
21	TESTI
22	CLKN
23	CLKP
24	EDCLK
25	VDD
26	RST1*
27	RST2*
28	(TCLKEN)
29	VGN0
30	VGN1
31	CALEN
32	CALIN
33	DIV4
34	TIN0N
35	TIN0P
36	TIN1N
37	TIN1P
38	VSS
39	TIN2N
40	TIN2P
41	TIN3N
42	TIN3P
43	ED
44	VGN2
45	VGN3
46	ENOSC
47	(ENTSIG)
48	SYNCMOD
49	RPUP
50	VDD

)

Pin No	Signal Name
51	(WP0)
52	(WP1)
53	(WP2)
54	(RP0)
55	(RP1)
56	(RP2)
57	(FRA0)
58	(FRA1)
59	(FRA2)
60	(FWA0/ENR5)
61	(FWA1/ENR6)
62	(FWA2/ENR7)
63	VSS
64	OSCOUT
65	TRIGC
66	TRIGD
67	TRIGS
68	TSTPLL
69	OCLK
70	ORUN
71	ERR*
72	EMPFLG
73	CH0
74	CH1
75	VDD
76	RE*
77	OE*
78	VSS
79	D0
80	D1
81	D2
82	D3
83	VDD
84	D4
85	D5
86	D6
87	D7
88	VSS
89	D8
90	D9
91	TRIGOUT
92	TFIFUL
93	VSS
94	DVALID*
95	EVEND*
96	FULFLG
97	VSS
98	CLKOUT
99	VDD
100	VDD

3. Package



TMCPHX1 Pin Assignment (Top View)

( ) = Test Signals (leave open)

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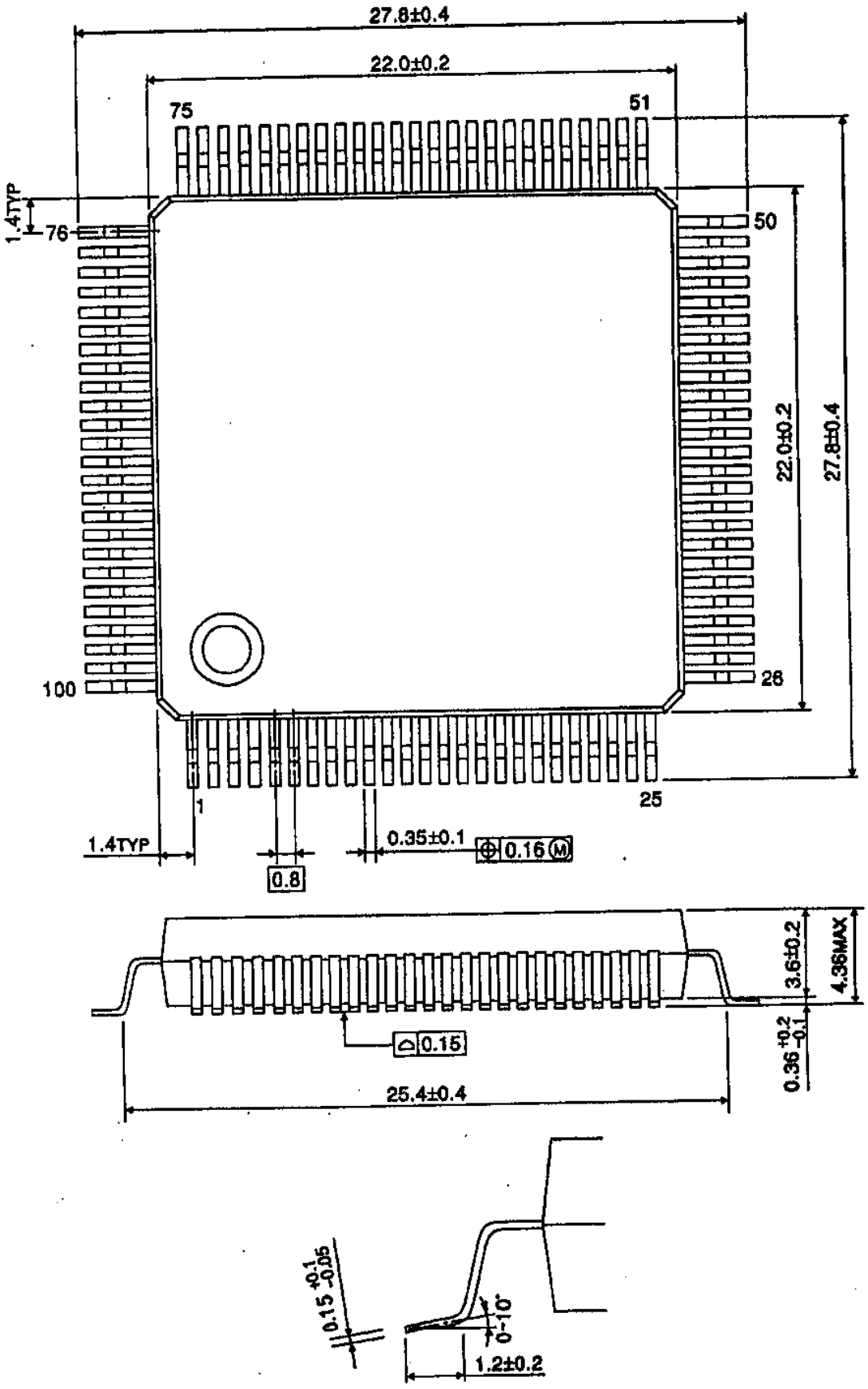


QFP100 : 100-pin Plastic Flat Package (Unit : mm)

4.Electrical Characteristics

4.1.Maximum Ratings

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	-0.3 to +4.6 V
V_{IN}	Input Voltage	-0.3 to VDD+0.3 V
I_{IN}	Input Current	±10 mA
T_{STG}	Storage Temperature	-40 to +125 ûC

4.2. Recommended Operating Condition

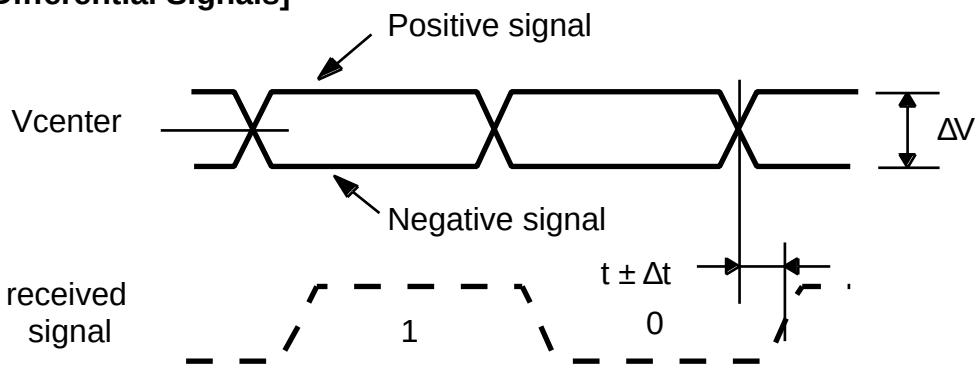
(V_{SS} = 0V)

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	3.3 to 3.8 V
Ta	Ambient Temperature	0 to +60 ûC

4.3.DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input High Voltage		V_{DD} x 0.8		
V_{IL}	Input Low Voltage		V_{DD} x 0.2		
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	-10	10	µA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	-10	10	µA
V_{OH}	High-Level Output Voltage	FRA0-2, FWA0-2, RP0-2, WP0-2, WRUN, ORUN, RRUN, TRIGOUT, TFIFUL; I_{OH} = -4 mA (B4)	2.4		V
		All Signals except above; I_{OH} = -8 mA (B8)	2.4		V
V_{OL}	Low-Level Output Voltage	FRA0-2, FWA0-2, RP0-2, WP0-2, WRUN, ORUN, RRUN, TRIGOUT, TFIFUL; I_{OH} = 4 mA (B4)		0.4	V
		All Signals except above I_{OH} = 8 mA (B8)		0.4	V
I_{OZ}	3-state Output Leakage Current		-10	10	µA
I_{DDS}	Quiescent Device Current	$V_{IN} = V_{DD}$ or V_{SS}		60	µA
Vcenter	Center voltage of differential signal	ΔV = 200 mV, | Δt | < 1 ns	1.4	2.4	V
ΔV	Differential signal amplitude		200	-	mV

[Differential Signals]



4.4. AC Characteristics

(VDD = 3.3 V, Ta = 25 ˚C.)

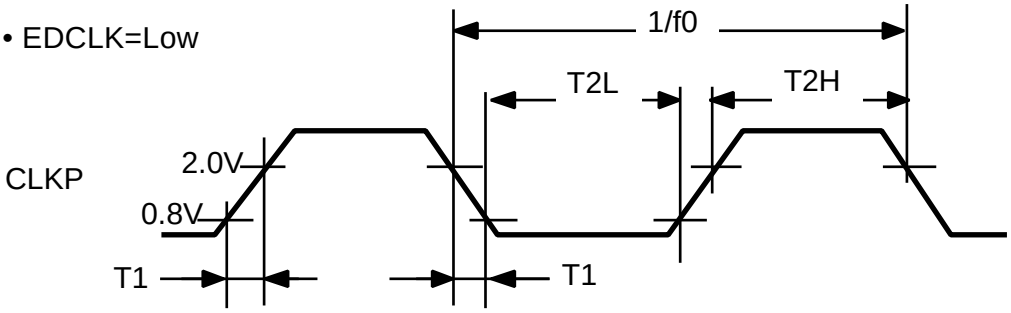
(FRA0-2, FWA0-2, RP0-2, WP0-2, WRUN, ORUN, RRUN, TRIGOUT : Cload = 25 pF, All other output signals : Cload = 50 pF)

4.4.1. Clock Signal Characteristics

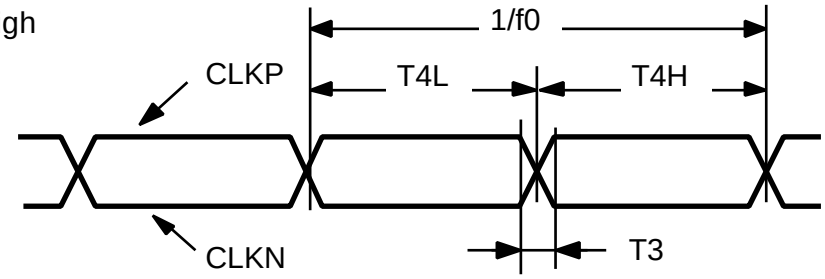
Symbol	Characteristics	Condition	Min	Typ	Max	Unit
f0	CLK frequency	DIV4=L	10	-	50	MHz
		DIV4=H	2.5	-	12.5	MHz
T1	CLK rise and fall time	EDCLK=L	-	-	3.0	ns
T2L/T2H	CLK duty factor	EDCLK=L	0.5	1.0	1.5	
ΔV/T3	CLK rise and fall rate	EDCLK=H	-	-	1	V/ns
T4L/T4H	CLK duty factor	EDCLK=H	0.5	1.0	1.5	
T5	External clock and PLL clock phase offset	DIV4=H				ns
T6	External clock and PLL clock phase offset	DIV4=L				ns
T7	Rising edge delay between OSCOUT and PLL clock					ns
T8	Falling edge delay between OSCOUT and PLL clock					ns

[Clock Waveforms]

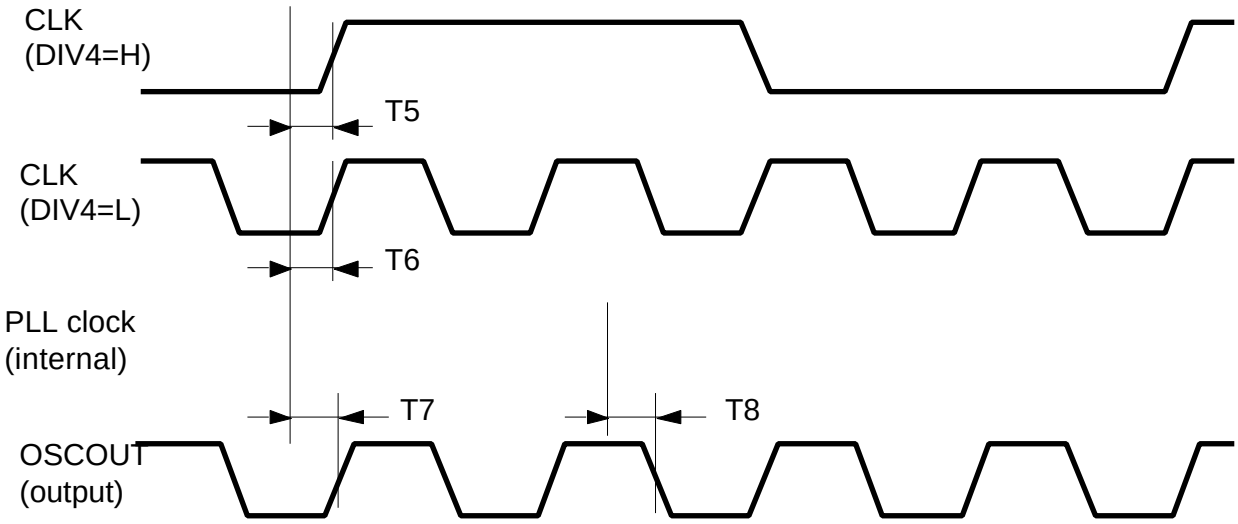
• EDCLK=Low



• EDCLK=High



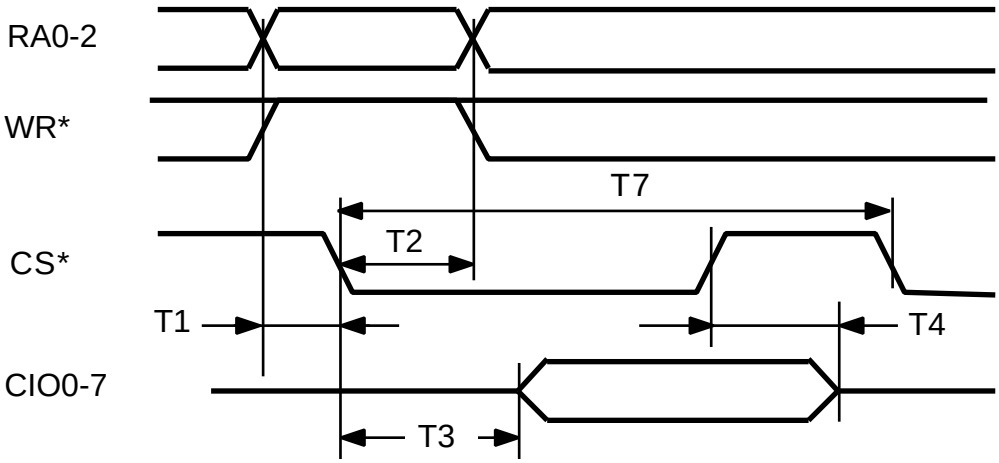
[Clock Offsets]



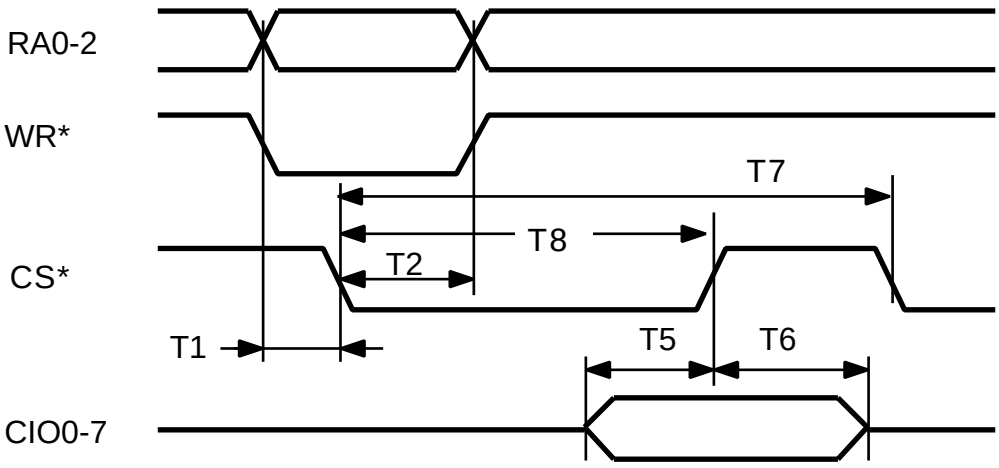
4.4.2. CSR Access Timing

Symbol	Characteristics	Min	Max	Unit
T1	RA, WR* setup time	1.0	-	ns
T2	RA, WR* hold time	3.0	-	ns
T3	CS* asserted to CIOx asserted	5.0	21	ns
T4	CS* negated to CIOx negated	3.7	14	ns
T5	CIO0-7 setup time	0.0	-	ns
T6	CIO0-7 hold time	6.0	-	ns
T7	Cycle time		-	ns
T8	CS* pulse width		-	ns

[CSR Read Cycle Timing Diagram]



[CSR Write Cycle Timing Diagram]



4.4.3. Input Recording Timing

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	WSTART setup time					ns
T2	WSTART hold time					ns
T3	WRUN assert timing					ns
T4	WRUN negate timing					ns
T5	Input recording timing	Δt=bit width				ns

(*) If WSTART is asserted outside of this safety area, it is not guaranteed that the input recording will start from the next cycle. User can identify the start of recording by checking WRUN signal., or synchronize the WSTART signal to CLK signal if necessary.

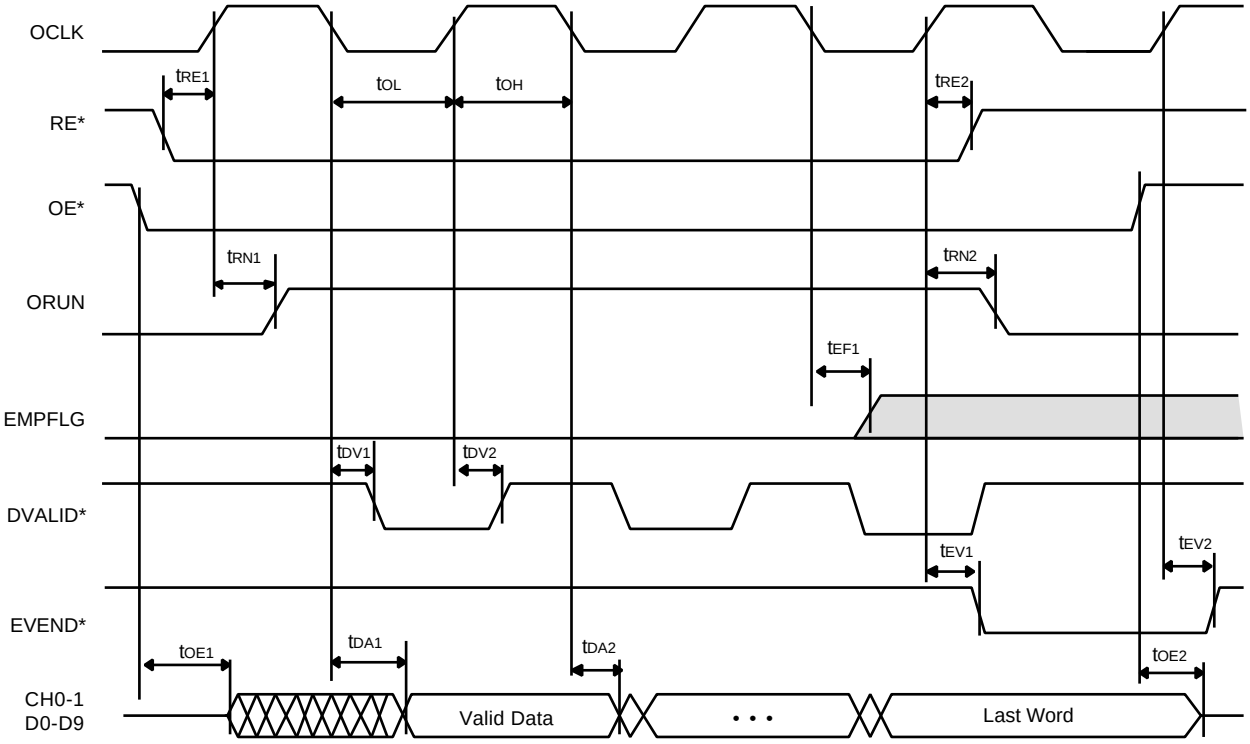
4.4.4. Readout Timing

Symbol	Characteristics	Condition	Min	Max	Unit
t_{OE1}	OE* assert to data line enable time		2.0	9.0	ns
t_{OE2}	OE* negate to data line disable time		2.0	9.0	ns

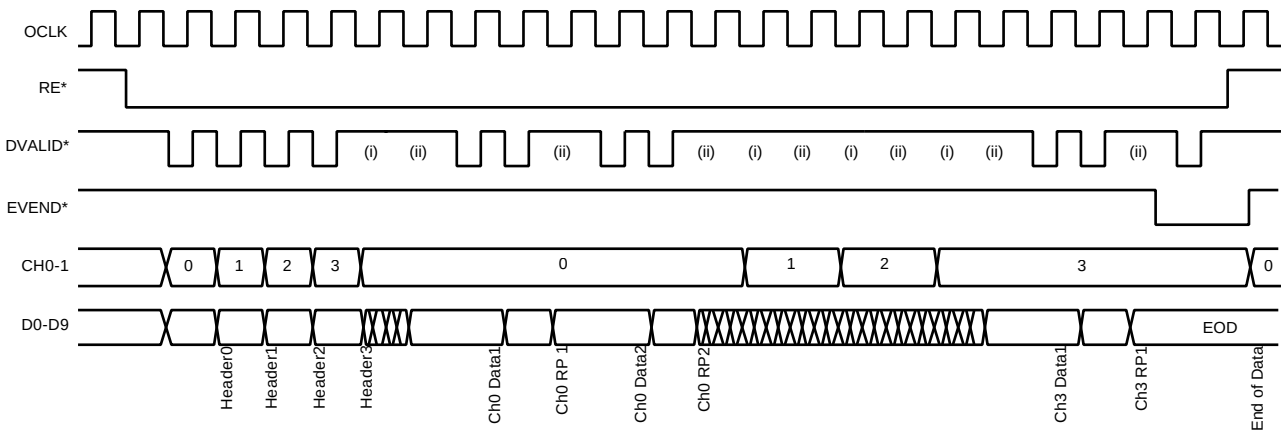
4.4.5. Synchronous Readout Timing

Symbol	Characteristics	Condition	Min	Max	Unit
t_{RE1}	RE* Setup time		4.0	-	ns
t_{RE2}	RE* Hold time		0.0	-	ns
t_{RN1}	ORUN assert timing		2.0	10.0	ns
t_{RN2}	ORUN negate timing		2.0	10.0	ns
t_{DV1}	OCLK low to DVALID* assert time		3.0	12.5	ns
t_{DV2}	OCLK high to DVALID* negate time		3.0	12.5	ns
t_{DA1}	OCLK low to data valid time		-	19.0	ns
t_{DA2}	OCLK low to data invalid time		3.0	-	ns
t_{EF1}	OCLK low to EMPFLG* assert time		5.0	20.0	ns
t_{EV1}	OCLK high to EVEND* assert time		2.5	11.0	ns
t_{EV2}	OCLK high to EVEND* negate time		2.5	11.0	ns
t_{OH}	OCLK high pulse width		10.0	-	ns
t_{OL}	OCLK low pulse width		13.0	-	ns

[Synchronous Mode]



• Example of data output sequence in synchronous mode with zero suppression

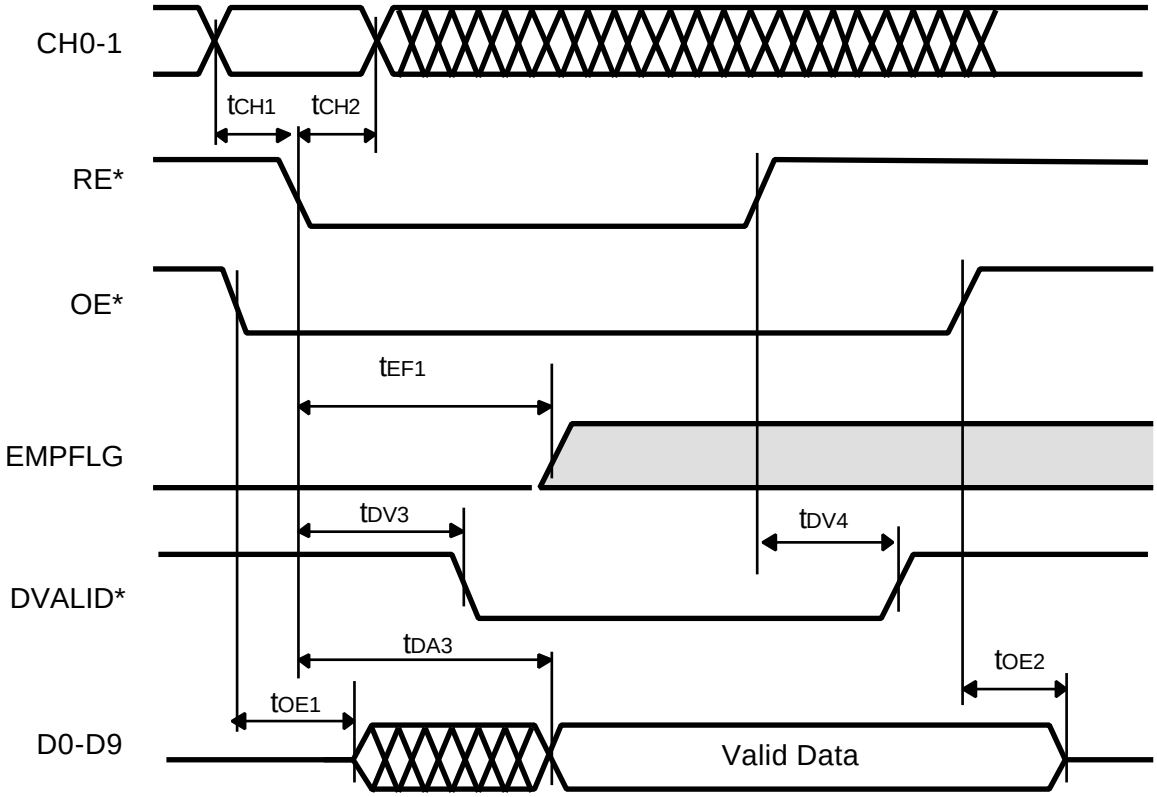


(i) --- missing DVALID* cycle due to channel change, (ii) --- missing DVALID* cycle due to data check

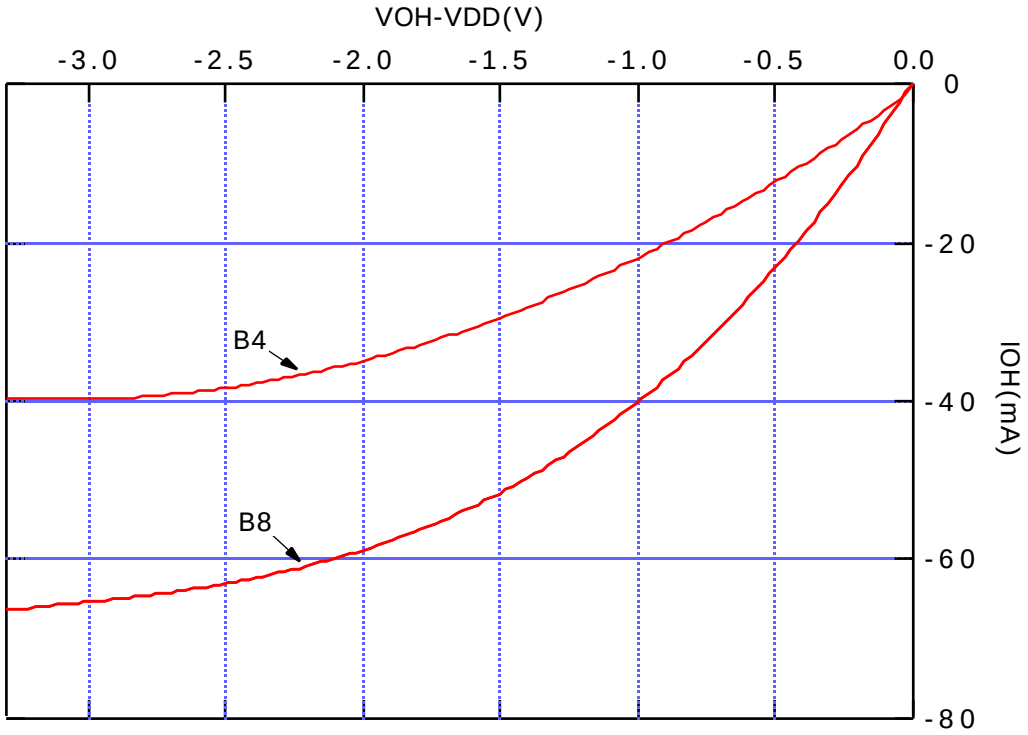
4.4.6. Asynchronous Readout Timing

Symbol	Characteristics	Condition	Min	Max	Unit
t_{CH1}	CH0,CH1 Setup time		2.0	-	ns
t_{CH2}	CH0,CH1 Hold time		2.0	-	ns
t_{DV3}	RE* assert to DVALID* assert time		3.5	14.5	ns
t_{DV4}	RE* negate to DVALID* negate time		3.5	14.5	ns
t_{DA3}	RE* assert to data valid time		-	21.0	ns
t_{DA4}	RE* negate to data invalid time		7.5	-	ns
t_{EF1}	RE* assert to EMPFLG* assert time		5.5	22.0	ns
t_{RL}	RE* low pulse width		10.0	-	ns
t_{RH}	RE* high pulse width		10.0	-	ns

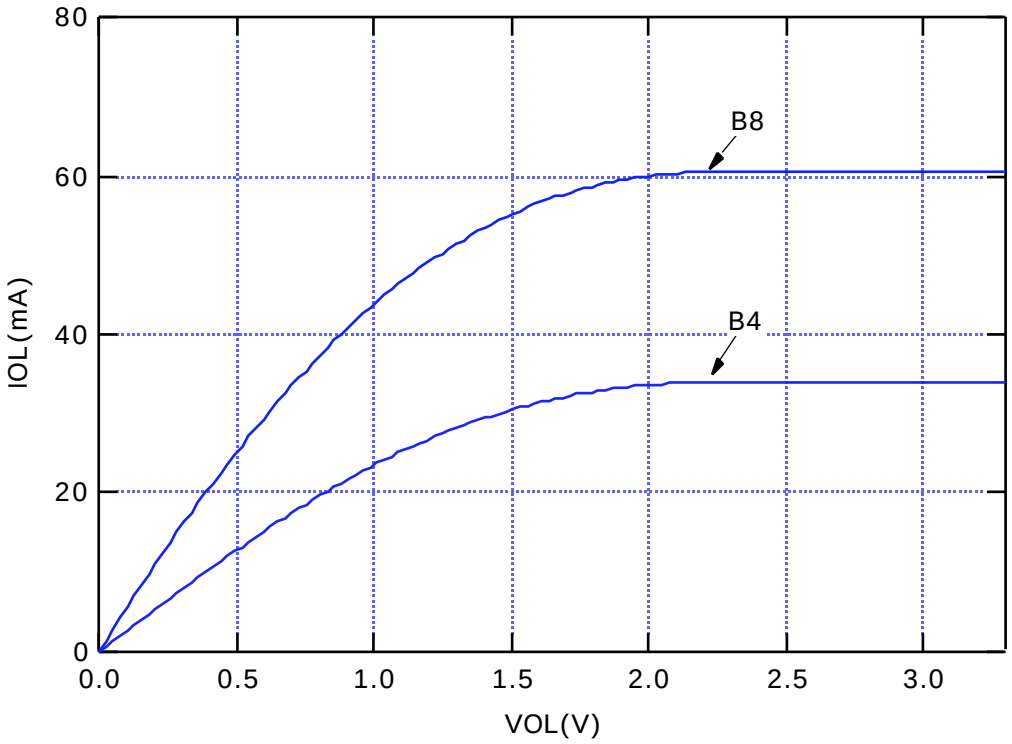
[Asynchronous Mode]



4.5.Output driver characteristic



Output High Level Current Characteristic (VDD=3.3V, Ta=25 °C, typ)



Output Low Level Current Characteristic (VDD=3.3V, Ta=25 °C, typ)