68K20FPI

68020 FASTBUS Processor Interface Technical Manual

Version 3.0 May, 1991

Y. Arai
KEK, National Laboratory for High Energy Physics
1-1 Oho, Tsukuba, Ibaraki 305, JAPAN

CONTENTS

1 INTRODUCTION

The 68020 FASTBUS Processor Interface (68K20FPI) is a FASTBUS master module which has a powerful 32 bit microprocessor (68020) and a Floating Point Co-Processor (68881).

It has a local memory sub-board (now 1 MB, can be upgraded in future) and 8 ROM sockets (64, 128, 256 or 512k bits ROM's) which are accessed both from CPU and FASTBUS. Internal bus is also used by Ethernet controller to transfer packet data by DMA. The module also has Ethernet tranceiver in the board, so you can connect many 68K20FPI's in a crate easily. The module also has two RS232C ports, SCSI Interface and NIM input and output connectors.

Features;

I. Processor Side
1. 68020 microprocessor with 16(25) MHz clock.
2. 68881 Floating Point Co-Processor with 16 MHz clock.
3. 1 MB static RAM sub-board with battery backup.
4. 32 bit port PROM(64 - 512k bit) x 8 or 32 bit port x 4 + 8 bit port x 4 ROM.
5. Dual RS-232C serial line interface(300 - 38.4 k baud).
6. AM7990/6992 Ethernet interface with tranceiver.
7. WD33C93 SCSI(Small Computer System Interface) Bus Interface for disk driver application etc.
8. User programable Input and Output Lemo connectors (NIM level).
9. Real Time Clock with battery backup.

II. Fastbus Side
1. FASTBUS single width module.
2. CSR 0(Enable, Run, SR enable, SR assert, CPU Reset, User Interrupt, and ID bits), CSR 8(Arbitration level and type).
3. All FASTBUS addressing mode as master.
4. Maximum Block Transfer rate of about 6 MB/s as master.
5. Accesssed via Geographical addressing and Random Data and Block Transfer read/write as slave.
6. Maximum Block Transfer rate of about 10 MB/s as slave.
7. AS/AK lock and GK hold options.
8. Receives SR, SS <>0 and User interrupts.
9. Assert/Negate Service Request(SR).

2 BLOCK DIAGRAM

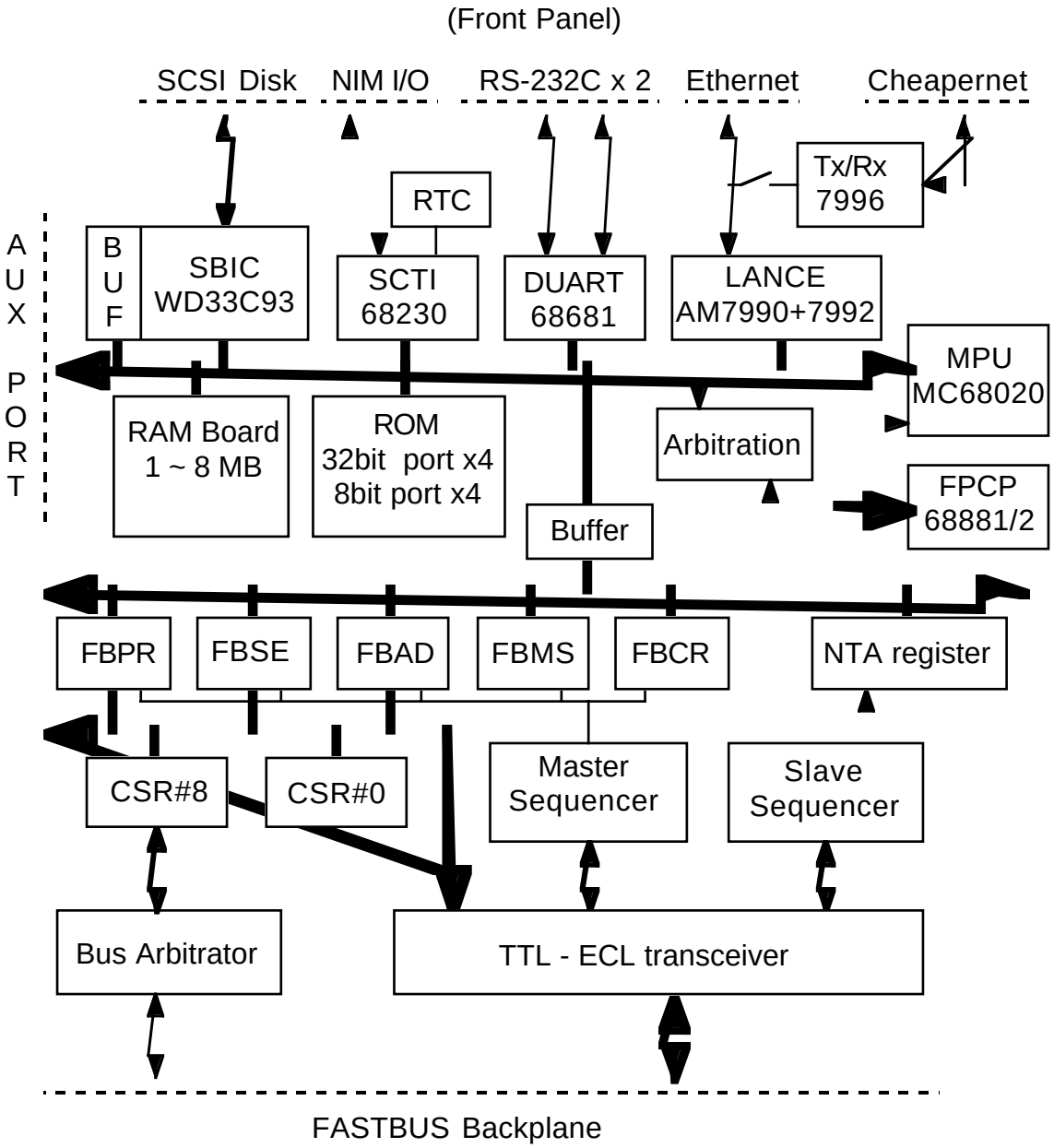


Fig.1 Block diagram of the 68K20FPI.

3 REGISTERS

The 68K20FPI has several registers for 68020 side and 2 registers for FASTBUS side.

* 68020 side

FBAD ---- FASTBUS Address/Data Register.
FBPR ---- FASTBUS Primary Address Register.
FBSE ---- FASTBUS Secondary Address Register.
FBMS ---- FASTBUS Mode Select Register.
FBCR ---- FASTBUS Control and Status Register.
SCTI ---- SCSI, NIM I/O, Real Clock, Timer Control Register.

SBICA --- SCSI-Bus Interface Controller Address Register.
SBICR --- SCSI-Bus Interface Controller Register.
SBICD --- SCSI Data Buffer.
DUART --- Dual Asynchronous Receiver/Transmitter and Miscellaneous information.
LANCE --- Ethernet Controller.
FPCP ---- Floating Point Coprocessor.

* FASTBUS side

CSR#0 --- Enable, Run, SR enable, SR assert and ID bits etc.
CSR#8 --- Arbitration level and type.

Address map the 68K20FPI is shown in Appendix A.

3.1 FBAD

FASTBUS Address/Data register (Long Word Port). When the processor read/write this register, the master sequencer will start and execute FASTBUS cycle according to the FBPR, FBSE, FBMS and FBCR.

This register is actually used in many purpose (gate, latch ...), but user need not care for that.

3.2 FBPR

FASTBUS Primary Address register (Long Word Port). When the processor starts FASTBUS operation, the contents of this register is used as Primary Address of FASTBUS.

3.3 FBSE

FASTBUS Secondary Address register (Long Word Port). When the processor starts FASTBUS operation and NOSEC bit of FBMS is zero, the contents of this register is used as Secondary Address of FASTBUS.

3.4 FBMS

FASTBUS Mode Select register (Long Word Port). When the processor starts FASTBUS Address Cycle, AMS0 and AMS1 are used as Mode Select bits. When the processor proceeds to Data Cycle, DMS0 and DMS1 are used as Mode Select bits. (DMS0 bit means the operation is Block/Pipeline Transfer, so you should also set ASLock at the begining of the operation and reset the ASLock bit after the operation.)

NOSEC bit indicates whether the Secondary Address Cycle will be done or not. If NOSEC bit is set, the Secondary Address Cycle will be skipped. When ASLOCK bit is set, AS/AK lock is maintained after next operation. When GKHOLD bit is set, GK is hold after next operation. If ASEG bit is set, EG bit is asserted during address cycle. As this is usually done by ancillary logic, user does not need to set this bit in normal operation.

FBMS - FASTBUS Mode Select/Error Status Register

Bit	Name	Contents
31-18	-	not used
17	DMS2	Data Cycle MS2 value (>V2.0)
16	AMS2	Address Cycle MS2 value (> V2.0)
15	DATC	Error at Data Cycle
14	SADC	Error at Secondary Address Cycle
13	PADC	Error at Primary Address Cycle
12	ARBC	Error at Arbitration Cycle
11	DK	DK ststus on error
10	SS2	Slave Status 2 on error
9	SS1	Slave Status 1 on error
8	SS0	Slave Status 0 on error
7	ASEG	Assert EG at Address Cycle flag
6	GKHOLD	GK Hold flag
5	ASLOCK	AS Lock flag
4	NOSEC	No Secondary Address Cycle flag
3	DMS1	Data Cycle MS1 value
2	DMS0	Data Cycle MS0 (Block/Pipe) value
1	AMS1	Address Cycle MS1 value
0	AMS0	Address Cycle MS0 value

3.5 FBCR

FASTBUS Operation Control and Status registers (Byte Port). FBCR is made up of several registers which is implemented by MC68230 LSI. These registers control FASTBUS operation and interrupt. Please refer to Appendix A and the Data Sheets of the MC68230.

Port	Bit	R/W	Contents
A	3	R	Bus DK
	2	R	Bus AK
	1	R	Slave
	0	R	Master
B	7	R/W	Assert RB * (0 = assert RB)
	6	R/W	Reset Sequencer
	5	R/W	Negate SR
	4	R/W	Assert SR
	3	R/W	Reset GK
	2	R/W	Set GK
	1	R/W	Enable CPU Reset from CSR#0
	0	R/W	Set Enable and RUN
C	7	R/W	Debug Mode* (must be 1)
	4	R	CSR#0 Enable and Run*
	3	R/W	Long Timer Interrupt Enable
	2	R/W	Data Cycle Timer Interrupt Enable
	1	R/W	Secondary Address Cycle Timer Enable
	0	R/W	Primary Address Cycle Timer Enable

(* -- negative logic)

Interrupt source

H1 --- Timer Interrupt
H2 --- SS Interrupt
H3 --- SR Interrupt
H4 --- CSR#0 User Interrupt

3.6 SCTI

SCSI, NIM I/O, Real Time Clock and Timer Control Register.

Port A - SBIC Control Register

Bit	R/W	Contents
7	R/W	SCSI Control Mode
6	-	-
5	-	-
4	-	-
3	W	SCSI Reset
2	W	SBIC Reset
1	R/W	SBIC Data Transfer Enable
0	W	SBIC Buffer Address Reset

Port B - Real Time Clock Control Register 1

Bit	R/W	Contents
7	R	RTC Busy
6	W	RTC Address Write
5	W	RTC Read
4	W	RTC Write
3	R/W	RTC Data bit 3
2	R/W	RTC Data bit 2
1	R/W	RTC Data bit 1
0	R/W	RTC Data bit 0

Port C - Real Time Clock Control register 2

Bit	R/W	Contents
7	-	-
6	-	-
5	-	-
4	-	-
3	-	-
2	-	-
1	R/W	RTC Select
0	R/W	RTC Stop

Control bit

H1 --- SBIC Interrupt
H2 --- not used
H3 --- NIM Input
H4 --- NIM Output

3.7 SBICA

SBIC Address Register. The registers of SBIC are read (or written) in a two step operation. The address of the register to be accessed is written into the SBICA register. During a subsequent operation, the data being read (or written into) the register port SBICR. The contents of the SBICA is incremented by one each time a register is accessed. Exceptions to this are the Address, Auxiliary Status, Data and Command Registers (Appendix C).

3.8 SBICR

SBIC Register port. The contents of the register selected in the SBICA is read from (or written into) the SBICR.

3.9 SBICD

SBIC Data Port. The data read from (or written into) SCSI bus is stored in a buffer(8 k byte). The address of the data buffer is cleared via "SBIC Buffer Address Reset" (SCTI port-A 0) bit. The address is incremented by one each time the data port is accessed.

3.10 DUART

Dual Asynchronous Receiver/Transmitter. Dual RS232C port and miscellaneous information.

Input Port

Bit	Contents
IP5	System information 3 (FPCP)
IP4	System information 2
IP3	System information 1
IP2	System status 3
IP1	System status 2
IP0	System status 1

Output Port

Bit	Contents
OP7	-
OP6	-
OP5	-
OP4	Bus Timeout Enable
OP3	Bus Timeout Clock
OP2	System status 3
OP1	System status 2
OP0	System status 1

3.11 LANCE

Ethernet Controller. See Am7990 Manual and Appendix F.

3.12 FPCP

Floating point Coprocessor. See MC68881 Manual.

3.13 CSR #0

o Module ID and Control and Status bit

Bit (*)	read	write
0	-	-
S1	Enabled	Enable
S2	RUNning	RUN
3	-	-
S4	SR Assertion Enabled	Enable SR Assertion
S5	SR asserted	Assert SR
S6	CPU Reset Status	CPU Reset
7	-	-
S8	User Interrupt Status	User Interrupt Set
9-15	-	-
16	Module ID "0"	-
C17	Module ID "0"	Disable
C18	Module ID "0"	HALT
19	Module ID "0"	-
C20	Module ID "0"	Disable SR Assertion
C21	Module ID "1"	SR Reset
C22	Module ID "0"	CPU Reset Clear
23	Module ID "1"	-
C24	Module ID "0"	User Interrupt Reset
25	Module ID "0"	-
26	Module ID "0"	-
27	Module ID "0"	-
28	Module ID "1"	-
29	Module ID "0"	-
30	Module ID "0"	-
31	Module ID "0"	-

*) Bit numbers preceeded by the letter S or C indicate that the bit is either Set (S) or Clear (C) bit associated with a selective set/clear action.

*) Bit 6 : CPU Reset. Reset signal is asserted to CPU and peripherals when this bit is set and Enable CPU bit is on (FBCR port B-1). After 516 clock cycle (about 3.3 usec for 16MHz CPU), this bit should be cleared.

*) Bit 16-31 : The module ID is set by dip switch and the ID of this module is "10A0(hex)".

3.14 CSR #8

o Arbitration Level and Type

AD<5:0> : Arbitration Level
AD<7> : = 0 No Assured Access Protocol
= 1 Assured Access Protocol

4 FASTBUS OPERATION

Let me show some of the FASTBUS operation programing examples below.

(1) Data Space Random Read

```
*
*Macro   MSset     AMS,DMS,NOSEC,ASLOCK,GKHOLD,ASEG
*
MSset    Macro
         EQU       ¥1 + ¥2<<2 + ¥3<<4 + ¥4<<5 + ¥5<<6 + ¥6<<7
         Endm
*
DSR      MSset     0,0,0,0,0,0          Data Space Randum with Sec. Adr.
*
         Move.l    #PRADR,FBPR          Set Primary Address
         Move.l    #SEADR,FBSE          Set Secondary Address
         Move.l    #DSR,FBMS            Set Mode Select
         Move.l    FBAD,D0              Read from FASTBUS to D0
```

(2) CSR Space Random Write

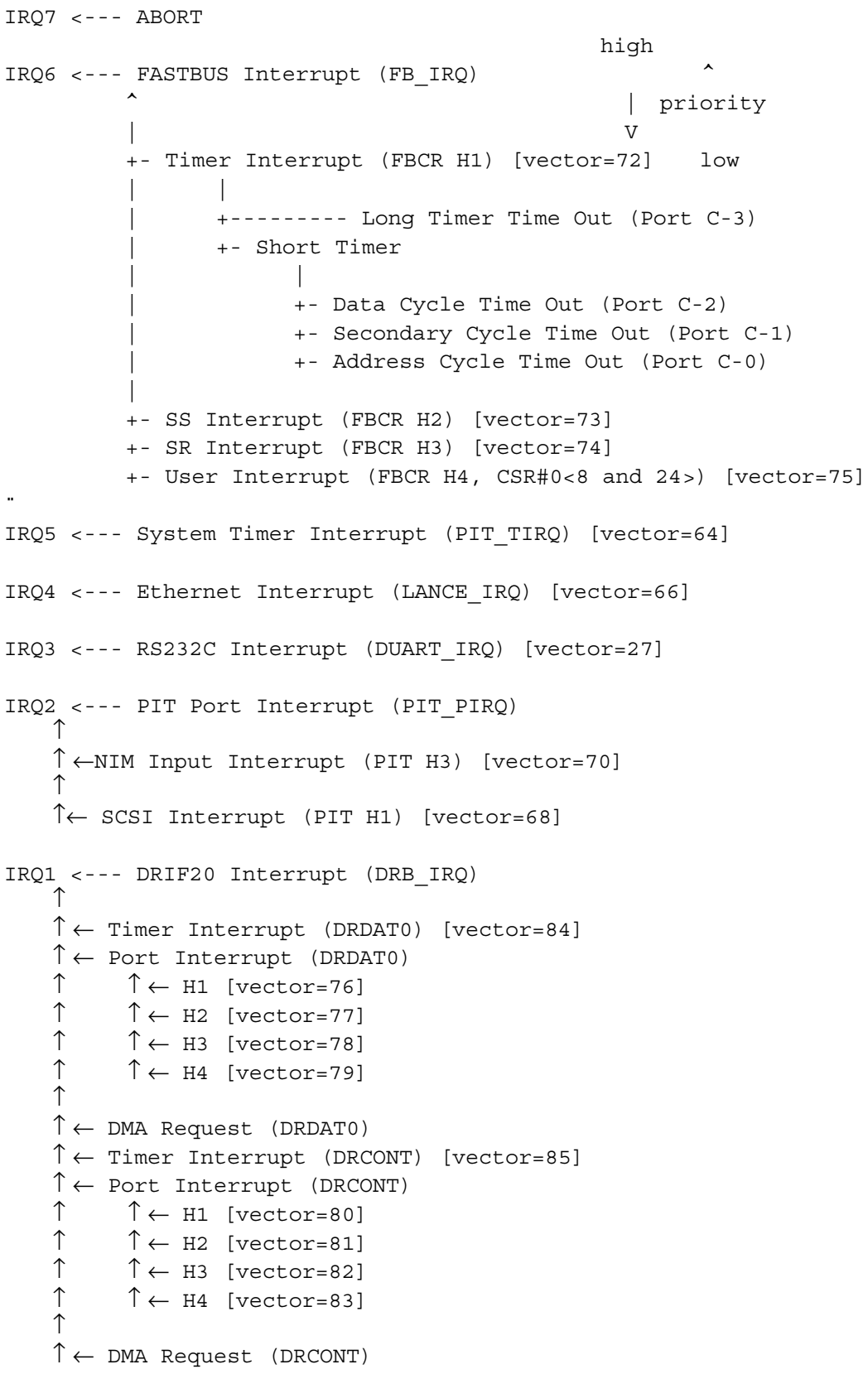
```
*
CSR      MSset     1,0,0,0,0,0          AMS=1 (CSR Space)
*
         Move.l    #PRADR,FBPR          Set Primary Address
         Move.l    #SEADR,FBSE          Set Secondary Address
         Move.l    #CSR,FBMS            Set Mode Select
         Move.l    D0,FBAD              Write D0 to FASTBUS
```

(3) Data Space Block Read

```
*
DSB      MSset     0,1,0,1,0,0          DMS=ASLock=1 (Block Transfer)
*
         Move.l    #PRADR,FBPR          Set Primary Address
         Move.l    #SEADR,FBSE          Set Secondary Address
         Move.l    #DSB,FBMS            Set Mode Select
         Lea       Buffer,A0            Load Buffer Address in A0
         Move.l    #Count,D1            D1 = Word Count
         Bra.s     Ls                   Branch to Loop Start
Loop     Move.l    FBAD,(A0)+           Read FASTBUS
Ls       Dbra      D1,Loop              Loop Until Count Out
         Clr.l     FBMS                 End AS/AK Lock
```

5 INTERRUPT

There are several source of interrupt to the processor;



5.1 System Timer Interrupt

This interrupt is used in a operating system to switch tasks.

5.2 Ethernet Interrupt

This interrupt will occur when a packet is received or a packet transmission is finished.

5.3 RS232C Interrupt

This interrupt can be used to control terminal I/O.

5.4 NIM Input Interrupt

NIM Input Interrupt will occur if the NIM Interrupt is enabled and the NIM input signals goes from low to high. The Interrupt is controlled by SCTI H3 bit.

5.5 FASTBUS Interrupt

There are several interrupt sources in the FASTBUS part. These are connected to the FBCR register interrupt bit H1 - H3.

5.5.1 Long Timer Time Out -

Long Timer Time out will occur if the Long Timer Interrupt is enabled and then the processor attempt to operate on FASTBUS and no response was received after Long Timer Time out period. The processor will jumps to the Port Vector Address when the interrupt occurs. If the Long Timer Interrupt occurs, H1S(Timer Interrupt) will be set. The FASTBUS operation will be aborted and the data is obscure if the operation is read. The status at the timeout can be checked by reading FBMS register.

The Interrupt is controlled by the Port C-3 and H1 in the FBCR. The Long Timer can be set between 128 ms to 8 sec by jumper pin. The timer will not stop even if the WT is asserted.

5.5.2 Short Timer Time Out -

Short Timer Time out will occur if the Short Timer Interrupt is enabled and then the processor attempt to operate on FASTBUS and no response was received after Short Timer Time out period. The processor will jumps to the Port Vector Address when the interrupt occurs. If the Short Timer Interrupt occurs, H1S(Timer Interrupt) will be set. The FASTBUS operation will be aborted and the data is obscure if the operation is read. The status at the timeout can be checked by reading FBMS register.

The Interrupt is controlled by the Port C-0,1,2(Address, Secondary and Data respectively) and H1 Control in the FBCR. The Short timer can be set between 0.8 us to 819 us by jumper pin. The timer will stop if the WT is asserted.

5.5.3 SS Response Error -

SS(Slave Status) Error Interrupt will occur if the SS Interrupt is enabled and non zero SS value is returned when the processor attempt to operate on FASTBUS. The processor will jumps to the Port Vector Address when the interrupt occurs.

If the SS Error Interrupt occurs, H2S(SS Interrupt) will be set and FBMS register will latch the SS value and corresponding FASTBUS cycle bit. The FASTBUS operation will be stopped and the data may be obscure if the operation is read. The Interrupt is controlled by the H1 Control bits in the FBCR.

5.5.4 Service Request Interrupt -

SR Interrupt will occur if the SR Interrupt is enabled and SR is asserted on the segment and current operation of the processor is end. The processor will jumps to the Port Vector Address when the interrupt occurs.

If the SR Interrupt occurs, H3S will be set. The Interrupt is controlled by the H3 Control bits in the FBCR.

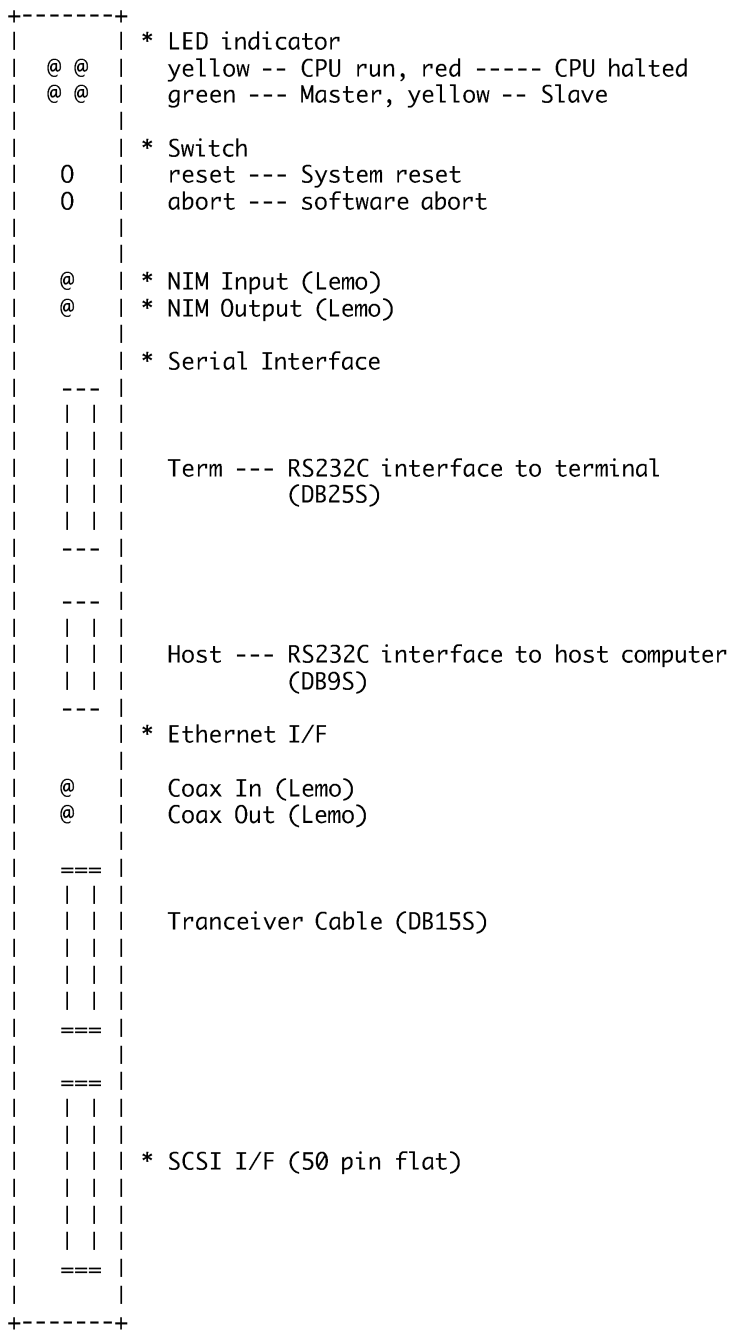
5.5.5 User Interrupt -

User Interrupt will occur if the User Interrupt is enabled and CSR 0<8> is set and current operation of the processor is end. The processor will jumps to the Port Vector Address when the interrupt occurs. The use of this bit is application dependent. This can be used to notice some information to the processor. The bit CSR 0<8> is also used as flag even if the interrupt is disabled.

If the User Interrupt occurs, H4S will be set. The Interrupt is controlled by the H4 Control bits in the FBCR.

6 HARDWARE

6.1 Front Panel



6.2 Power Consumption

```
   5.0 V x   7.0 A
  -5.2 V x   2.0 A
   2.0 V x   0.5 A
  ----------------------
             Total    46 W
```

6.3 Jumper Pins And Switches

@ --- Default Setting

* JA1 : MPU Cash Control

@ Open ----> Enable
Close ---> Disable

* JA2 : FPCP Clock

@ 1 - 2 : 16.6 MHz
2 - 3 : 12.5 MHz

* JA3 : Interrupt Level Setting

Source	Level
1 --- (reserved)	12 --- IRQ1
2 --- PIT_PIRQ	11 --- IRQ2
3 --- DUART_IRQ	10 --- IRQ3
4 --- LANCE_TIRQ	9 --- IRQ4
5 --- FB_IRQ	8 --- IRQ5
6 --- PIT_TIRQ	7 --- IRQ6

@ Default Setting

```
12 ---
11 --- 2
10 --- 3
 9 --- 4
 8 --- 6
 7 --- 5
```

-(old version)----------

Source	Level
1 --- LANCE_IRQ	12 --- IRQ1
2 --- DUART_IRQ	11 --- IRQ2
3 --- PIT_PIRQ	10 --- IRQ3
4 --- PIT_TIRQ	9 --- IRQ4
5 --- FB_IRQ	8 --- IRQ5
6 --- (Reserved)	7 --- IRQ6

@ Default Setting

```
12 ---
11 --- 3
10 --- 2
 9 --- 1
 8 --- 4
 7 --- 5
```

---

* JA4 : Interrupt Acknowledge

Receiver	Acknowledge
1 --- LANCE_IACK(autovector)	12 --- IACK1
2 --- DUART_IACK	11 --- IACK2
3 --- PIT_PIACK	10 --- IACK3
4 --- PIT_TIACK	9 --- IACK4
5 --- FB_IACK	8 --- IACK5
6 --- (Reserved)	7 --- IACK6

@ Default Setting
(Same as JA3)

* JA5 : MPU Clock

1 - 2 : 25.0 MHz
@ 2 - 3 : 16.6 MHz

* JC1 : RAM Acknowledge

@ 1 - 8 : x + 30 ns
2 - 7 : x + 60 ns
3 - 6 : x + 90 ns
4 - 5 : x + 120 ns

* JC2 : RAM Size (Sub-Board Address Size)

@ 1 - 14, 2 - 13, 3 - 12 : 1 MB
2 - 14, 3 - 13, 4 - 12 : 2 MB
3 - 14, 4 - 13, 5 - 12 : 4 MB
4 - 14, 5 - 13, 6 - 12 : 8 MB
5 - 14, 6 - 13, 7 - 12 : 16 MB

+--version 1.x ----------+
| * JE1 : ROM Size |
| |
| 1 - 9, 2 - 8, 3 - 7 : 2764 |
| 2 - 9, 3 - 8, 4 - 7 : 27128 |
| 3 - 9, 4 - 8, 5 - 7 : 27256 |
| @ 4 - 9, 5 - 8, 6 - 7 : 27512 |
| |
|* JE2 : ROM Type |
| |
| 2 - 3, 4 - 5 : 2764, 27128 |
| 2 - 3, 5 - 6 : 27256 |
| @ 1 - 2, 5 - 6 : 27512 |
| |
|* JE3 : Byte/Long Word Port Selection |
| |
| 1 - 2, 5 - 6 : Long Word Port |
| @ 2 - 3, 4 - 5 : Byte Port |
+----------+

* JE1 :

* JE2 : ROM Type
1 - 2 : 512 kbit
2 - 3 : 256 kbit

* JE3 : ROM/RAM Select for UE4
  1 - 2 : RAM
  2 - 3 : ROM

* JE4 : ROM/RAM Select for UE4
  1 - 2 : ROM
  2 - 3 : RAM

* JE50 : ROM acknowledge timing
  1 - 10 : x ns
  2 - 9 : x+20 ns
  3 - 8 : x+40 ns
  4 - 7 : x +60 ns
  5 - 6 : x+80 ns

* SF1 : System Information Switch (Defined by Software)

  1 : BOOT (@ON---monitor/debugger, OFF---auto boot OS-9)
  2 : FPIMON (@ON---microware debugger, OFF---FPI monitor)
  3 : FPCP Sence (@ON---Sence, OFF---No sence)

* DF1 : System Status Display (Defined by Software)

  1 : monitor program
  2 : OS-9/68020
  3 :

* JF1 : Bus Timeout Set

  1 - 8 : No Timeout
  2 - 7 : t x 256
  3 - 6 : t x 64
@ 4 - 5 : t x 16
  (t = 1us - 32ms (@10us)): DUART Timer)

* JF2 : FASTBUS Long Timer Set

  1 - 8 : No Timeout
@ 2 - 7 : t x 16384
  3 - 6 : t x 4096
  4 - 5 : t x 512
  (t = 1us - 32ms (@10us): DUART Timer)

* SWH1 : Ethernet Tranceiver Use

  All Close : Use Tranceiver
@ All Open : No Use Tranceiver

* JH1 : LANCE Accesss Space Set

  Close : User Space
  Open : Supervisor Space

* SK1, SK2 : CSR#0 ID Switch

SK2 - 8 : bit 31
.
.
SK1 - 1 : bit 16

(Close = 1, Open = 0)

* JL1 : Slave Sequencer Clock Select

1 - 8 : (Single Step)
2 - 7 : 10 MHz
@ 3 - 6 : 20 MHz
4 _ 5 : 33 MHZ

* (SWP1 : Single Step Switch)

* JP1 : Master Sequencer Clock Select

1 - 8 : (Single Step)
2 - 7 : 10 MHz
@ 3 - 6 : 20 MHz
4 - 5 : 33 MHz

* JP2 : FASTBUS Short timer Set

1 - 8 : No Timeout
2 - 7 : 1.6 us (dont't use)
3 - 6 : 26 us
@ 4 - 5 : 410 us

* JQ1 : Slave Sequencer Bus Request Enable

@ Close : Enabled
Open : Disabled

APPENDIX A --- ADDRESS MAP

(Only Lower 24 bits are used for address decoding)

Address	Contents 0 8 16 24 31	Comments
0 3FF	Exception Vector	
400 7FF	debugger work area	
800 17FF	OS9 Excep. Vect / System Stack	
1800 27FF	OS9 Global Memory	RAM (1 MB)
2800 BFFFF	OS9 Work Memory	
C0000 DF000 EF000 FFFFF	FASTBUS Buffer /r0 (r0_128kb) FASTBUS work area	^ | CPU/FASTBUS Dual Ported RAM | | V
100000 FFFFF	Reserved for RAM Extension	
800000 800004 80FFFF	Power On SSP Power On PC debugger/BOOT ROM	
810000 81FFFF	User ROM	ROM (512 kB)
820000 82FFFF	User ROM	
830000 83FFFF	Battery Backup RAM	
840000 860000 87FFFF	OS9 ROM x 4 (Long Port) OS9 modules ROMDISK (/rom0)	
880000 8FFFFF	Reserved for ROM Extension	
900000 FAFFFF	Aux. Board Address Space	
FB0000 FB0004 FB0008	FBAD FBPR FBSE	

FB000C	FBMS	
FB0010		
	Reserved	
FB00FF		
FB0100	|xxxxxxxxxxxxxxxxxxxxxxxxxxxx	
	SCTI |xxxxxxxxxxxxxxxxxxxxxxxxxxxx	Appendix C
FB011F	|xxxxxxxxxxxxxxxxxxxxxxxxxxxx	
FB0120	SBICA |xxxxxxxxxxxxxxxxxxxxxxxxxxxx	
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	
FB0140	SBICR |xxxxxxxxxxxxxxxxxxxxxxxxxxxx	Appendix D
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	
FB0160	SBICD |xxxxxxxxxxxxxxxxxxxxxxxxxxxx	
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	
FB0180		
	Reserved	
FB01FF		
FB0200	|	
	DUART| |	Appendix E
FB020F	|	
FB0210		
	Reserved	
FB02FF		
FB0300	LANCE RDP | LANCE RAP	
FB0304		
	Reserved	
FB03FF		
FB0400		
	Reserved	
FB0FFF		
FB1000	|	
	FBCR |	Appendix B
FB101F	|	
FB1020		
	Reserved	
FFFFFF		

68K20FPI address map

APPENDIX B --- FBCR REGISTER (MC68230)

FBCR registers (MC68230)

( ) -- Default Setting

address	bit 7	6	5	4	3	2	1	0	
FB1000	Port Mode		H34 E	H12 E	H4 Se	H3 Se	H2 Se	H1 Se	PGCR
	(0)	(0)	(1)	(1)	(0)	(0)	(0)	(0)	
FB1001	*	SVCRQ sel		InterPFS		Port Int Pri Cont			PSRR
		(0)	(X)	(1)	(1)	(0)	(0)	(0)	
FB1002	Port A Data Direction								PADDR
	(1)	(1)	(1)	(1)	(0)	(0)	(0)	(0)	
FB1003	Port B Data Direction								PBDDR
	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	
FB1004	Port C Data Direction								PCDDR
	(1)	(X)	(X)	(0)	(1)	(1)	(1)	(1)	
FB1005	Port Interrupt Vector Register						*	*	PIVR
FB1006	A Sub Mode		H2 Control			H2 En	H1 En	H1 St	PACR
	(1)	(X)	(0)	(X)	(X)	(0/1)	(0/1)	(X)	
FB1007	B Sub Mode		H4 Control			H4 En	H3 En	H3 St	PBCR
	(1)	(X)	(0)	(X)	(X)	(0/1)	(0/1)	(X)	
FB1008	Port A Data Register ($F0)								PADR
FB1009	Port B Data Register ($82)								PBDR
FB100A	Port A Alternate Register								PAAR
FB100B	Port B Alternate Register								PBAR
FB100C	Port C Data Register ($80)								PCDR
FB100D	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	PSR
FB100E	null								
FB100F	null								
FB1010	TOUT/TIACK Cont		ZD Ct	*		Clock Cont		T Ena	TCR
	(0)	(0)	(X)	(0)		(0)	(0)	(0)	
FB1011	Timer Interrupt Vector Register								TIVR
FB1012	null								
FB1013	Count Preload Register (high)								CPRH
FB1014	Count Preload Register (mid)								CPRM
FB1015	Count Preload Register (low)								CPRL
FB1016	null								
FB1017	Count Register (high)								CNTRH
FB1018	Count Register (mid)								CNTRM
FB1019	Count Register (low)								CNTRL
FB101A								ZDS	TSR

9 APPENDIX C --- SCTI REGISTER (MC68230)

SCTI registers (MC68230)

( ) -- Default Setting

address	bit 7 6 5 4 3 2 1	
FB0100	Port Mode |H34 E|H12 E|H4 Se|H3 Se|H2 Se|H1 Se (0) (0) | (0) | (0) | (1) | (1) | (1) | (1)	PGCR
FB0101	| SVCRQ sel | Inter PFS |Port Int Pri Cont | (0) (X) | (1) (1) | (0) (0) (	PSRR
FB0102	Port A Data Direction (1) (X) (X) (X) (1) (1) (1) (1)	PADDR
FB0103	Port B Data Direction (0) (1) (1) (1) (1/0) (1/0) (1/0) (1/0)	PBDDR
FB0104	Port C Data Direction (X) (X) (X) (X) (X) (X) (1)	PCDDR
FB0105	Port Interrupt Vector Register | * | *	PIVR
FB0106	A Sub Mode | H2 Control |H2 En|H1 En|H1 St (1) (X) | (0) (X) (X) | (0) | (1) | (X)	PACR
FB0107	B Sub Mode | H4 Control |H4 En|H3 En|H3 St (1) (X) | (1) (0) (1/0) | (0) | (1) (X)	PBCR
FB0108	Port A Data Register	PADR
FB0109	Port B Data Register	PBDR
FB010A	Port A Alternate Register	PAAR
FB010B	Port B Alternate Register	PBAR
FB010C	Port C Data Register	PCDR
FB010D	H4 | H3 | H2 | H1 | H4S | H3S | H2S | H1S Level | Level | Level| Level | | |	PSR
FB010E	null	
FB010F	null	
FB0110	TOUT/TIACK Cont |ZD Ct| * | Clock Cont |T Ena (1) (0) (1) | (0) | | (0) (0) (1)	TCR
FB0111	Timer Interrupt Vector Register	TIVR
FB0112	null	
FB0113	Count Preload Register (high)	CPRH
FB0114	Count Preload Register (mid)	CPRM
FB0115	Count Preload Register (low)	CPRL
FB0116	null	
FB0117	Count Register (high)	CNTRH
FB0118	Count Register (mid)	CNTRM
FB0119	Count Register (low)	CNTRL
FB011A	| ZDS	TSR

10 APPENDIX D --- SBIC REGISTER (WD33C93)

( ) -- Default Setting

A0 AR	bit 7 6 5 4 3 2 1	
0 *	Address Register	AR (W) ASR (R)
	INT | LCI | BSY | CIP | 0 | 0 | PE | DBF	
1 0	0 | 0 | 0 | 0 | 0 | ID2 | ID1 | ID0	OID
1 1	DMA | WDB | 0 | 0 | 0 | 0 | HA | HPE	CNR
1 2	Time Out Period Register	TPR
1 3	Total Sectors Register /CDB1	TSR
1 4	Total Heads Register /CDB2	THR
1 5	Total Cylinders Register (high) /CDB3	TCRH
1 6	Total Cylinders Register (low) /CDB4	TCRL
1 7	Logical Address Register (high) /CDB5	LARH
1 8	Logical Address Register (mid high) /CDB6	LARMH
1 9	Logical Address Register (mid low) /CDB7	LARML
1 A	Logical Address Register (low) /CDB8	LARL
1 B	Sector Number Register /CDB9	SNR
1 C	Head Number Register /CDB10	HNR
1 D	Cylinder Number Register (high) /CDB11	CNRH
1 E	Cylinder Number Register (low) /CDB12	CNRL
1 F	0 | 0 | 0 | 0 | 0 | TL2 | TL1 | TL0	TLR
1 10	0 | CP6 | CP5 | CP4 | CP3 | CP2 | CP1 | CP0	CPR
1 11	0 | TP2 | TP1 | TP0 | 0 | OF2 | OF1 | OF0	STR
1 12	Transfer Count Register (high)	TCRH
1 13	Transfer Count Register (mid)	TCRM
1 14	Transfer Count Register (low)	TCRL
1 15	0 | 0 | 0 | 0 | 0 | DI2 | DI1 | DI0	DIR
1 16	ER | ES | 0 | 0 | SIV | SI2 | SI1 | SI0	SIR
1 17	SS7 | SS6 | SS5 | SS4 | SS3 | SS2 | SS1 | SS0	SSR (R)
1 18	SBT | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0	CCR
1 19	DR7 | DR6 | DR5 | DR4 | DR3 | DR2 | DR1 | DR0	DR

(A0 = 0 --> SBICA, A0 = 1 --> SBICR)

11 APPENDIX E --- DUART REGISTER (MC68681)

address	bit 7 6 5 4 3 2 1 0	name
FB0200	Mode Register A	MR1A,MR2A
FB0201	Status Register A Clock-Select Register A	SRA (R) CSRA (W)
FB0202	Command Register A	CRA (W)
FB0203	Receiver Buffer A Transmitter Buffer A	RBA (R) TBA (W)
FB0204	Input Port Change Register Auxiliary Control Register	IPCR (R) ACR
FB0205	Interrupt Status Register Interrupt Mask Register	ISR IMR
FB0206	Counter/Timer Upper Register	CTUR
FB0207	Counter/Timer Lower Register	CTLR
FB0208	Mode Register B	MR1B,MR2B
FB0209	Status Register B Clock-Select Register B	SRB CSRB
FB020A	Command Register B	CRB (W)
FB020B	Receiver Buffer B Transmitter Buffer B	RBB TBB
FB020C	Interrupt Vector Register	IVR
FB020D	Input Port Output Port Configuration Register	IPR OPCR
FB020E	Start Counter Command Output Port Register (bit set)	(R) OPRS(W)
FB020F	Stop Counter Command Output Port Register (bit reset)	(R) OPRC(W)

12 APPENDIX F --- LANCE REGISTER (AM7990)

( ) -- Default Setting

address	bit 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	name
FB0300	CSR Data	RDP
FB0302	not used |A1|A0	RAP

Bit	CSR0	CSR1	CSR2	CSR3
0	INIT	"0"	IADR(16)	BCON
1	STRT	IADR(1)	IADR(17)	ACON
2	STOP	IADR(2)	IADR(18)	BSWP
3	TDMD	IADR(3)	IADR(19)	reserved
4	TXON	IADR(4)	IADR(20)	reserved
5	RXON	IADR(5)	IADR(21)	reserved
6	INEA	IADR(6)	IADR(22)	reserved
7	INTR	IADR(7)	IADR(23)	reserved
8	IDON	IADR(8)	reserved	reserved
9	TINT	IADR(9)	reserved	reserved
10	RINT	IADR(10)	reserved	reserved
11	MERR	IADR(11)	reserved	reserved
12	MISS	IADR(12)	reserved	reserved
13	CERR	IADR(13)	reserved	reserved
14	BABL	IADR(14)	reserved	reserved
15	ERR	IADR(15)	reserved	reserved

13 APPENDIX G --- RTC REGISTER (MSM58321RS)

address	bit			
	3	2	1	0
0	Second 1			
1	*	Second 10		
2	Minute 1			
3	*	Minute 10		
4	Hour 1			
5	24H/12H	PM/AM	Hour 10	
6	Week			
7	Day 1			
8	Leap Year		Day 10	
9	Month 1			
A	*	*	*	Month 10
B	Year 1			
C	Year 10			
D	Reset (W)			