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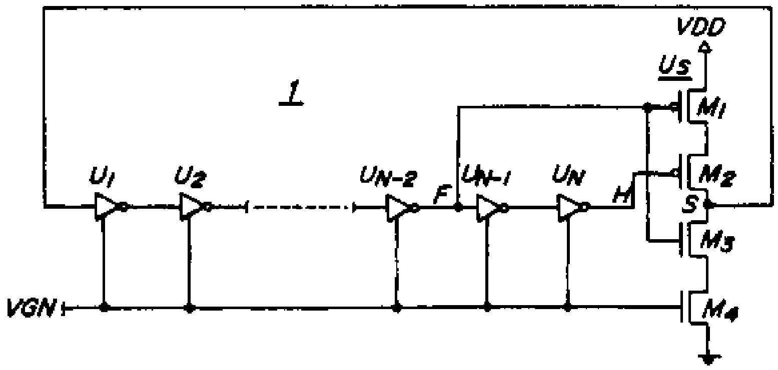
(54) Voltage-controlled oscillating circuit.

(57) The present invention is to provide a voltage controlled oscillating circuit comprising a multi-staged phase inversion circuit composed of 4 or more even-number N stages of phase inversion devices connected in a series; and a switch circuit having a delay time characteristic similar to that of said phase inversion circuit, wherein the switch circuit satisfies oscillation conditions by converting an output phase of the even-numbered inverters connected in a series into such a phase that is the same as those of the outputs of odd-numbered inverters connected in a series; thereby obtaining timing signals having a period equal to 1/N of the oscillation period.

FIG. 3A



The present invention relates to a voltage-controlled oscillating circuit to be used in a phase locked loop (PLL) circuit, which has played an important role in a high-speed signal processing circuit that requires high-speed, high-precision control of timing signals; and more particularly to a voltage-controlled oscillating circuit wherein a timing signal having a period of one even-numberth of the oscillation period.

The art of high-speed, high-precision controlling of timing signals has been one of the most important technologies in various electronics devices. Especially, in experiments of high energy physics that require a processing of highly frequent output signals coming out of a detector, it is necessary to control and measure high-speed, high-precision signals in both an accelerator and the detector.

On the other hand, in the technical fields of electronic apparatus, there has been a significant advance in the wide band system of video apparatus and enhancement of speed in computers and information transmission networks. Accordingly, there has been also required a further improved high-speed processing of digital signals in these technological fields.

A conventional phase locked loop (PLL) circuit, which plays an important role in the above-mentioned high-speed signal processing, has such a construction as shown in Fig. 1. Namely, the output pulse of the voltage-controlled oscillator (VO) is supplied into the phase comparator (PC), wherein the frequency and phase of the output pulse is compared with those of an input pulse (IP), then a phase difference detected as a comparison output is supplied into the loop filter (LF) in order to derive a phase error voltage to be fed back to the voltage-controlled oscillator (VO) to control the oscillation frequency, thereby obtaining an output pulse (OP) whose phase is locked to that of the input pulse (IP). With the above PLL circuit, there can be attained, if necessary, an output pulse (OP) having such a frequency equal to the value obtained by multiplying the frequency of the input pulse (IP) with an integer M or dividing the frequency with the M.

In particular, when a so-called ring oscillator 1 as shown in Fig. 2, wherein an output pulse of a multi-staged phase inversion circuit is fed back to the input side of the circuit, and a propagation delay time in respective devices can be controlled by an applied voltage, is used therein as the voltage-controlled oscillator VO, there can be obtained such a timing signal that has a time interval shorter than the oscillation output period T by deriving an output pulse from each inverter U at respective stages. For example, in the ring oscillator 1 having five stages of inverters U_1-U_5 connected in a series as shown in Fig. 2, there are generated oscillation pulses A, B, C, D and E each of which repeats bistable phase inversion with a period T. The phase inversion output A-E of respective inverters U_1-U_5 delay from the immediately preceding one with the same time intervals as shown in the figure. For instance, the adjoining leading edges in the phase inversion outputs A and C have such a time interval therebetween that is equal to one-fifth of the oscillation period T.

In order to oscillate the ring oscillator 1, it is necessary to fulfill such oscillation condition that the output 2 of the last stage should have an inverted level of the first stage input 3 at preceding cycle. Accordingly, the number of inverters to be connected in a series should be an odd number in order to oscillate the ring oscillator 1. As a result, there is only obtained such a timing signal that has a period equal to one odd-numberth of the oscillation period. On the other hand, in many controlling circuits or measuring circuits, there have been required timing pulses having such a time interval that has a period equal to one even-numberth of the oscillation period. In particular, there has been a great demand for timing signals having a period equal to $1/2^n$ of an oscillation period in a field of digital signal processing. As described above, however, conventional voltage-controlled oscillating circuits have not been able to meet these requirements since they have to include odd-numbered inverters connected in a series.

Meanwhile, an output signal detected by a detector for high energy beam particle such as a wire chamber needs to be measured with precision of not more than 1 ns. If it is intended to conduct such a precision measurement through a direct method, it is necessary to utilize a clock signal having a high frequency of 1 GHz or more. This is practically difficult to realize; and even if possible, the cost would amount to a significantly large sum.

In this connection, it may be possible to directly produce a clock signal having a frequency of around 100 MHz in a CMOS integrated circuit, if a phase locked loop (PLL) circuit is introduced into the CMOS integrated circuit. However, it is still difficult to obtain a clock signal having a frequency of 1 GHz by a direct means. Even if such a clock signal is obtained, it is not practical since it increases the power consumption of the CMOS integrated circuit.

Although it is difficult to directly produce clock signals having a frequency of 1 GHz, it is enough for many applications just to obtain clock pulses having time interval of 1 ns. Such a clock pulse can be obtained by utilizing such a ring oscillator in which a number of clock signal-producing circuits with a much lower frequency are operated successively at time intervals of 1 ns. Accordingly, it is considered to successively derive clock pulses from respective stages of the ring oscillator. As mentioned above, however, it is still difficult to produce timing signals having such a period equal to one even-numberth of the clock period. Meanwhile, a signal processing in a digital circuit may preferably be conducted at a timing of $1/2^n$ of the period. Accordingly, when the signal processing is conducted at a timing other than $1/2^n$ of the period, namely at a timing of one odd-numberth of the period which is easily derived from a circuit utilizing a conventional ring oscillator, the data obtained as processing results should be corrected by using an appropriate coefficient as a multiplier. As a result, the precision of signal processing is greatly deteriorated and the signal processing has to have a complicated system.

An aim of the present invention is to solve the above-mentioned problems and to provide an improved voltage-controlled oscillating circuit, wherein a timing signal having a period equal to one even-numberth of the oscillation period can be derived from a ring oscillator, which has only been able to produce a timing signal having such a period equal to one odd-numberth of the oscillation period.

Another aim of the present invention is to provide a voltage-controlled oscillating circuit wherein a switch circuit controls the propagation delay of the switch circuit and even number (N) stages of inverters connected in a series so that a low logic-level signal is subjected to a propagation delay corresponding to N+1 stages and a high logic-level signal is subjected to a propagation delay corresponding to N-1 stages; wherein the oscillation maintains.

A further aim of the present invention is to provide a voltage-controlled oscillating circuit comprising a multi-staged phase inversion circuit composed of 4 or more even-number N stages of phase inversion devices connected in a series, wherein a phase inversion delay time is controlled by means of an applied voltage, and a switch circuit having a delay time characteristic similar to that of the phase inversion circuit; wherein a switch output is at high logic level when outputs of phase inversion devices in the last stage and in the second from last stage of said multi-staged phase inversion circuit are both at low logic level, while the switch output is at low logic level when the output of phase inversion device in the second from last stage is at high logic level; wherein the output of the switch circuit is fed back to the input of the multi-staged phase inversion circuit so as to form an oscillating circuit; wherein a timing signal having a time interval of one-Nth of the oscillation period of the oscillating circuit can be taken out from respective phase inversion devices in respective stages of the multi-staged phase inversion circuit and the switch circuit.

Therefore, according to the present invention, there can be easily attained a timing signal having such a period equal to one even-numberth of the clock period, which has been difficult to be derived from a conventional oscillating circuit, in the course of integral multiplication of a clock frequency by means of a phase locked loop (PLL) circuit. In particular, since a timing signal having a period of $1/2^n$ of the clock period can be easily obtained, high-speed processing of digital signals comes to be conducted with ease. Therefore, the voltage-controlled oscillating device according to the present invention can have a wide application to various technologies from digital video apparatus to computer networks.

For example, the voltage-controlled oscillating circuit according to the present invention can be applied to devices used in the experiments of high energy physics for processing output signals highly frequently detected by a detector and in synchronous circuits for high-resolution image displaying apparatus such as high definition television (HDTV). Some examples of electronic apparatus in which the voltage-controlled oscillating circuit of the present invention can be applied may include the following:

High precision time-to-digital converter;
Synchronous circuit for video signals;
High-speed serial communication device;
Semiconductor testing device; and
Measuring device for distance between two cars.

Preferred embodiments of the present invention will be described hereinbelow by way of example only with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram illustrating a constitution of a phase locked loop (PLL) circuit;

Fig. 2 is a diagram illustrating a constitution of a conventional voltage-controlled oscillating circuit and waveforms of pulses in respective stages thereof;

Fig. 3A is a circuit diagram illustrating a rough constitution of a voltage-controlled oscillating circuit according to the present invention;

Fig. 3B is a circuit diagram illustrating a constitution of a inverter in each stage of the oscillating circuit shown in Fig. 3A;

Fig. 3C is a circuit diagram illustrating a detailed constitution of inverters shown in Fig. 3B;

Fig. 4A is a circuit example of an 8 inverter stage illustrating a constitution of a voltage-controlled oscillating circuit according to the present invention;

Fig. 4B is a waveform diagram showing waveforms of pulses in respective stages of the oscillating circuit shown in Fig. 4A;

Fig. 5 is a circuit diagram showing an applied example of the oscillating circuit according to the present invention which utilizes a leading edge of respective inverters;

Fig. 6 is a waveform diagram showing waveforms of pulses in respective stages of the oscillating device shown in Fig. 5; and

Fig. 7 is a circuit diagram showing another applied example of the oscillating circuit according to the present invention which utilizes a trailing edge of respective inverters.

Throughout different views of the drawings; PLL is a phase-locked loop, VO is a voltage-controlled oscillator, PC is a phase comparator, LF is a loop filter, IP is an input pulse, OP is an output pulse, f(t) is an external signal and $f(t_1)$, $f(t_2)$ are levels at time t_1 and time t_2 respectively, CK is a reference clock signal, D_1, D_2, D_3 ··· D_8 are data output signal, FF_1, FF_2, FF_3 ··· FF_8 are flip-flop circuits, U_1, U_2, U_3 ··· U_n are voltage controlled inverters, M_1, M_2, M_3 ··· M_8 are MOS type transistors, A ··· H, and S are output nodes, U_S is a switch circuit, VGN is a control voltage signal, IN is an input terminal of inverter, OUT is an output terminal of inverter, VDD is a drain voltage, 1 is a ring oscillator, 2 is a last stage output of ring oscillator, 3 is a first stage input of ring oscillator.

Referring now to Fig. 3A, there is shown a circuit diagram of a voltage-controlled oscillating circuit according to the present invention. In Fig. 3A, there is shown a constitution of a ring oscillator which is constructed by connecting phase inverting devices U_1-U_N, namely inverters U_1-U_N of an arbitrary even number (N) not less than 4 of in a series, and feeding outputs of a switch circuit US, which is connected to the last phase inverting device in the series, back to the input side of the phase-inverting devices connected in a series. A controlling voltage VGN is applied to each inverter U_1-U_N and to the switch circuit U_S so as to change the delay time of phase inversion in each of the inverters U_1-U_N and switch circuit U_S.

In fact, the voltage-controlled phase inverting devices U_1-U_N shown in Fig. 3A is constituted by four MOS-type transistors M_5-M_8 connected in a series as seen in Fig. 3C, like as the switch circuit U_S, which is composed of four MOS-type transistors M_1-M_4 connected in a series. With respect to the two transistors in the middle, however, there is such a difference that gate electrodes of M_2 and M_3 are controlled individually in the switch circuit U_S, while gate electrodes of M_6 and M_7 are connected parallel. In order to take out a timing signal having such a period that is exactly equal to one-Nth of the oscillation period T of the ring oscillator, it is important to equate the output load of each inverter with that of the switch circuit in addition to making respective inverters and the switch circuit have similar circuit constitutions. Therefore, a P-MOS transistor M_5 in each inverter is made to correspond to M_1 of the switch circuit, and is used as a dummy to equate the driving ability in the P-MOS transistor side with that of the switch circuit. Incidentally, the switch circuit U_S operates similarly even when gate connections are reversed between MOS transistors M_1 and M_2.

Therefore, while a phase inversion occurs in each stage of inverters U_1-U_N, wherein the output pulse has the logic level inverted from that of the input pulse supplied to the gate electrode of MOS transistor, the switch circuit U_S operates in a manner similar to that of a NOR circuit, and thus the output pulse in node S of the switch circuit is at high logic level when both of the output pulse in node F of the stage U_{N-2}, i.e. the second stage from the last stage, and the output pulse in node H of the last stage U_N are at low logic level, and the output pulse in node S of the switch circuit is at low logic level when the output pulse in node F of the stage U_{N-2} is at high logic level. Accordingly, the phase of the output pulse which is fed back to the input side of the even-numbered inverters connected in a series, is equal to the phase of the output pulse coming out of the odd-numbered inverters connected in a series, thereby satisfying oscillating conditions of a ring oscillator.

In this connection, N-MOS transistors M_8 and M_4 in respective inverters U_1-U_N and in the switch circuit U_S are control transistors for controlling the delay time in the respective of them. In fact, M_8 and M_4 only control the timing for trailing the output pulse. However, since the polarity of pulse is inverted at every succeeding stage in the phase inversion circuit, timings for leading and trailing of the phase inversion can be controlled alternately.

Next, with respect to an example of the voltage-controlled oscillating circuit, wherein the number N of inverters connected in a series is eight, circuit constitution thereof is illustrated in Fig. 4A, and timing of the signal at each stage is successively shown in Fig. 4B. In the following, explanation will be given only on the timing for leading edge in the phase inversion of the signal; however, almost the same is true of the timing for trailing edge. Referring to the timing diagram shown in Fig. 4B, in the case where the output pulse in node A of the inverter U_1 is at high logic level at the time of t_0, the leading edge is transferred to every other stage in the series, as illustrated by the arrows in the figure, with a time interval of T/8, i.e. one-eighth of the oscillation period T.

In this connection, an explanation will be made on the circuit operation of the switch circuit U_S. In the timing diagram of Fig. 4B, when the output node F of the inverter U_6 is at low logic level at the time of t_1, the MOS transistor M_1 of the switch circuit U_S is in ON state and MOS transistor M_3 is in OFF state. In this case, however, the output node H of the inverter U_8 is at high logic level, and thus the MOS transistor M_2 is in OFF state. As a result, the output node S of the switch circuit U_S is in floating state, thereby maintaining the immediately preceding low logic level. On the contrary, at the time of t_2, when the output node H of the inverter U_8 is inverted to one at low logic level, the output node F of the inverter U_6 is still at low logic level. Accordingly, both of M_1 and M_2 are in ON state, and the output node S of the switch circuit U_S comes to be at high logic level at the time of t_3 due to a phase inversion occurred therein.

On the other hand, when the output node F of the inverter U_6 is at high logic level at the time of t_4, the MOS transistor M_1 is in OFF state and MOS transistor M_3 is in ON state. Accordingly, the output node S of the switch circuit U_S is subjected to a phase inversion toward the low logic level at the time of t_5 without waiting for the output node H of the inverter U_8 to be inverted to the high logic level.

As described above, in the voltage-controlled oscillating circuit according to the present invention, the signal in node S has experienced time delays at 9 stages, which are owing to respective phase inversions occurred in the inverters U_1-U_8 and the switch circuit U_S with respect to the input signal at low logic level, while the output signal in node S has experienced time delays at 7 stages, which are owing to respective phase inversions occurred in the inverters U_1-U_6 and the switch circuit U_S with respect to the input signal at high logic level. As a result, although the total time delay during one period T of a phase inversion signal includes even-numbered time delays occurred in $9+7=16$ stages, oscillation caused by repeating phase inversions can be maintained because the phase inversion signal at low logic level and that at high logic level are respectively subjected to odd-numbered phase inversions. Accordingly, since the polarity of the phase inversion signal is reverted to the original one at every second stage in the series, it is possible to take out a timing pulse at time intervals equal to one-eighth of the phase inverting oscillation period T.

In Figs. 5 and 7, f(t) shows an external signal; CK is a reference clock signal; PC is a phase comparator; LF is loop filter; VGN is a control voltage; and D_1, D_2, D_3 $\cdots$ D_8 respectively show a data output signal of flip-flop circuits FF_1-FF_8.

By combining respective flip-flop circuits FF_1-FF_8 with respective inverters U_1-U_8 of the oscillating circuit of the present invention as shown in Figs. 5 and 7 in order to constitute a device wherein the external signal f(t) is successively latched by means of an output signal of each inverter, it becomes possible to detect the change in the external signal f(t) at time intervals of one-eighth of the period of the reference clock,signal CK which is phase-locked by the PLL circuit utilizing the oscillating circuit according to the present invention.

The operation of this circuit will be explained below. By constituting the phase-locked loop (PLL) circuit so that an output 4 of the voltage-controlled oscillating circuit 1 according to the present invention and the reference clock CK are connected to the input of the phase comparator PC, and the controlling voltage VGN is derived through the loop filter LF, the oscillating circuit 1 of the present invention can produce oscillations having a period equal to that of the reference clock signal CK under certain conditions. In this connection, since every other output signal of inverters U_1-U_8 and the switch circuit U_S has a leading edge at intervals of one-eighth of the oscillation period T as described before referring to Fig. 4B, every other flip-flop circuit among FF_1-FF_8 may successively latch the logic level of the external signal f(t) as respective data outputs D_1, D_2, $\cdots$, D_8, D_1, $\cdots$, at the intervals of T/8 as shown in Fig. 6. The data output D_1 has a level $f(t_1)$ of the external signal at the time of t_1, the data output D_2 has a level $f(t_2)$ of the external signal at the time of t_2, and so do the following data outputs D_3, $\cdots$, D_8. Accordingly, by examining the data outputs D_1-D_8, when the external signal f(t) is changed can be known with a preciseness of T/8.

Referring now to Fig. 7, there is shown another constitution example of oscillation device, which utilizes trailing edges of respective stages. The oscillation device of this example is different from that of Fig. 5 in positions at which the flip-flop circuits are connected, and respective flip-flop circuits FF_1-FF_8 latch the logic level of the external signal f(t) at respective trailing edges of the signals. In both oscillation devices shown in Figs. 5 and 7, it is important to make respective stages have an equal load for maintaining the time intervals of latch constant, for example, by incorporating a dummy capacity.

As is clear from the above explanation, while the voltage-controlled oscillating circuit, which has been conventionally used in a PLL circuit, has been applied thereto primarily for the purpose of utilizing the oscillation output signal whose phase is synchronous with that of the input signal; according to the present invention, timing signals can further be taken out at time intervals of 1/N (N is an even number) of the oscillation period. In particular, since timing signals having a time interval of $1/2^n$ of the oscillation period, if combined with counters which utilize oscillation output of the oscillating circuit according to the present invention as the input thereof, there can be attained such a remarkable effect that a high-speed, high-precision measurement can be continuously conducted for a long time without difficulty.

Claims

1. A voltage-controlled oscillating circuit comprising a multi-staged phase inversion circuit composed of 4 or more even-number N stages of phase inversion devices connected in a series, wherein a phase inversion delay time is controlled by means of an applied voltage, in each of said phase inversion devices, and a switch circuit having a delay time characteristic similar to that of said phase inversion circuit; wherein a switch output is at high logic level when outputs of phase inversion devices in the last stage and in the second from last stage of said multi-staged phase inversion circuit are both at low logic level, while said switch output is at low logic level when said output of phase inversion device in the second from last stage is at high logic level; wherein said output of said switch circuit is fed back to the input of said multi-staged phase inversion circuit so as to form an oscillating circuit; wherein a timing signal having a time interval of one-Nth of the oscillation period of said oscillating circuit can be taken out from respective phase inversion devices in respective stages of said multi-staged phase inversion circuit and said switch circuit.

2. The voltage-controlled oscillating circuit according to claim 1, wherein timing signals having a time interval of one-Nth of the oscillation period respectively taken out from phase inversion devices in respective stages of said multi-staged phase inversion circuit and said switch circuit are respectively input to latch circuits, thereby successively detecting an external signal transition.

FIG. 1

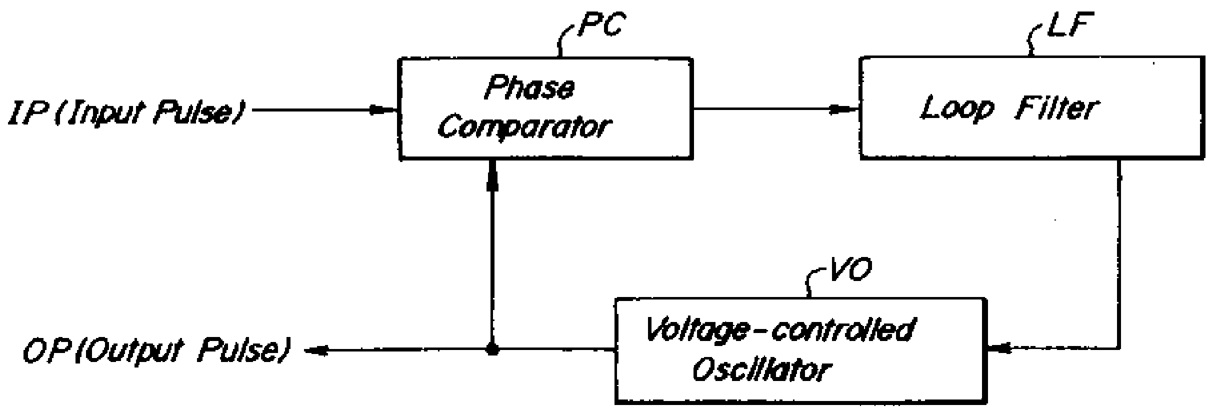

PC
Phase Comparator
LF
Loop Filter
IP (Input Pulse)
VO
Voltage-controlled Oscillator
OP (Output Pulse)

FIG_2

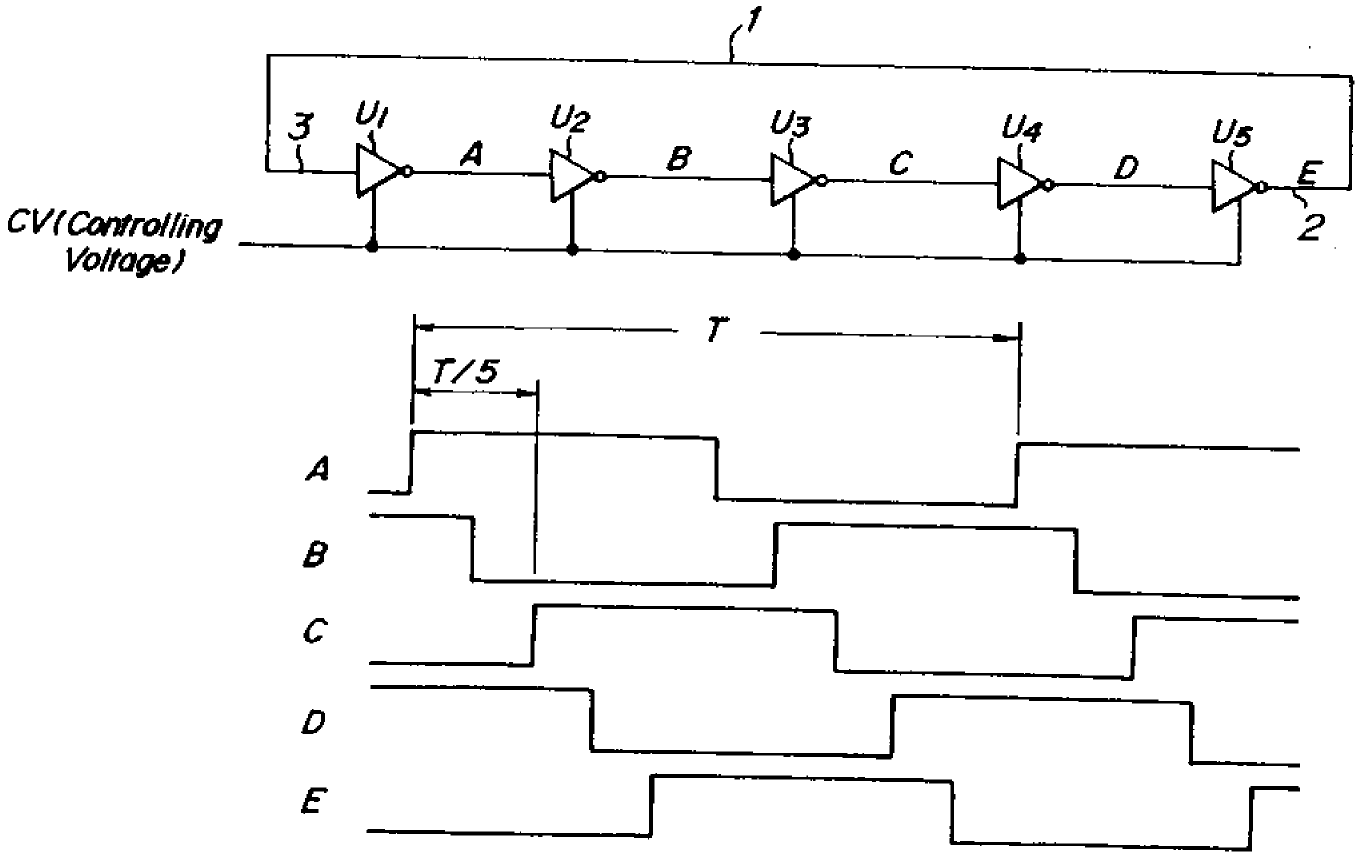


FIG_3A

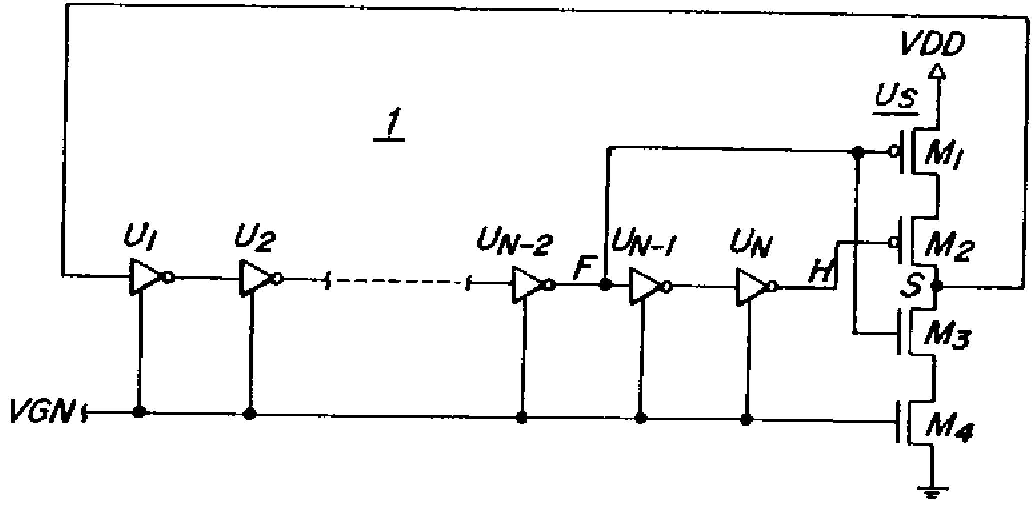


FIG_3B

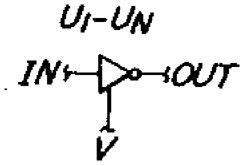


FIG_3C

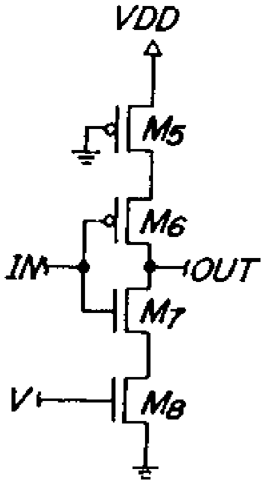


FIG_4A

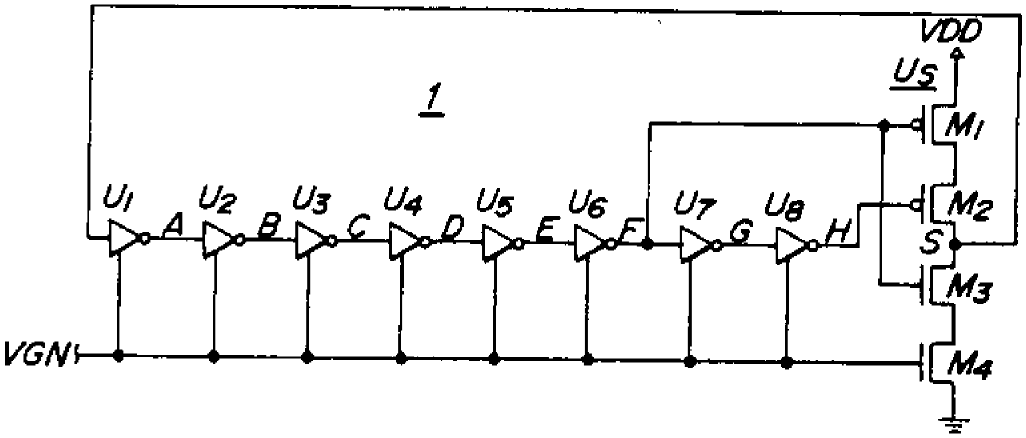

1
VDD
U5
M1
M2
S
M3
M4
U1
A
U2
B
U3
C
U4
D
U5
E
U6
F
U7
G
U8
H
VGN

FIG_4B

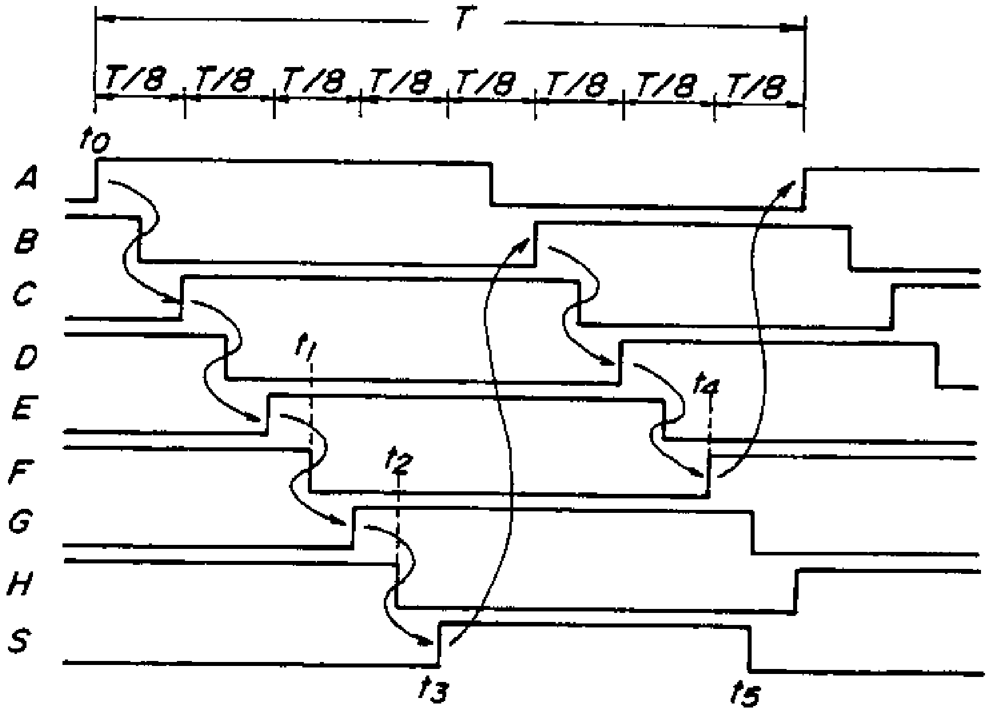

T
T/8
T/8
T/8
T/8
T/8
T/8
T/8
T/8
t0
A
B
C
D
E
F
G
H
S
t1
t2
t3
t4
t5

FIG_5

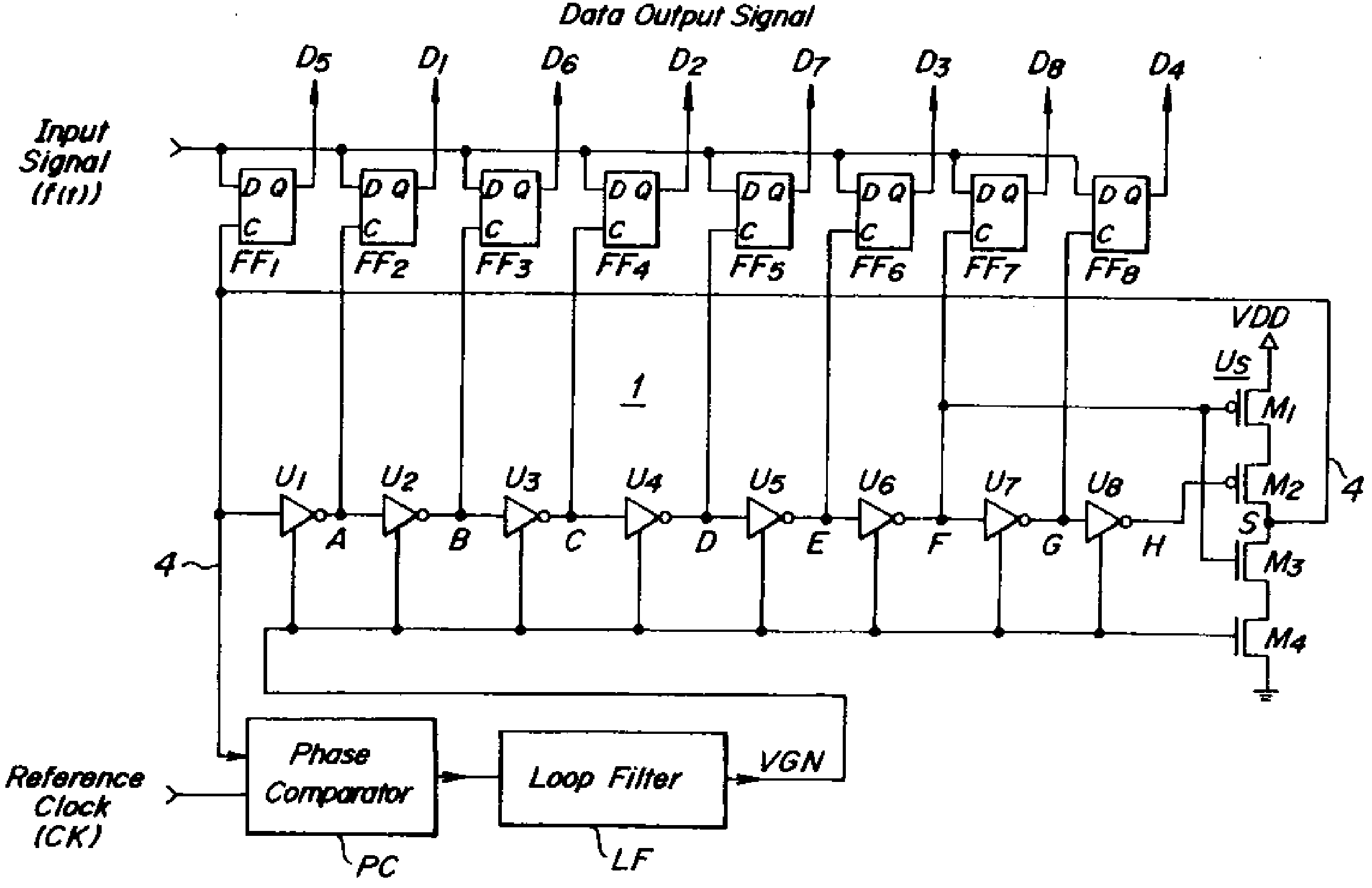

Data Output Signal
D5
D1
D6
D2
D7
D3
D8
D4
Input Signal (f(t))
D Q
C
FF1
FF2
FF3
FF4
FF5
FF6
FF7
FF8
1
VDD
Us
M1
M2
S
M3
M4
4
U1
U2
U3
U4
U5
U6
U7
U8
A
B
C
D
E
F
G
H
4
Reference Clock (CK)
Phase Comparator
PC
Loop Filter
LF
VGN

FIG. 6

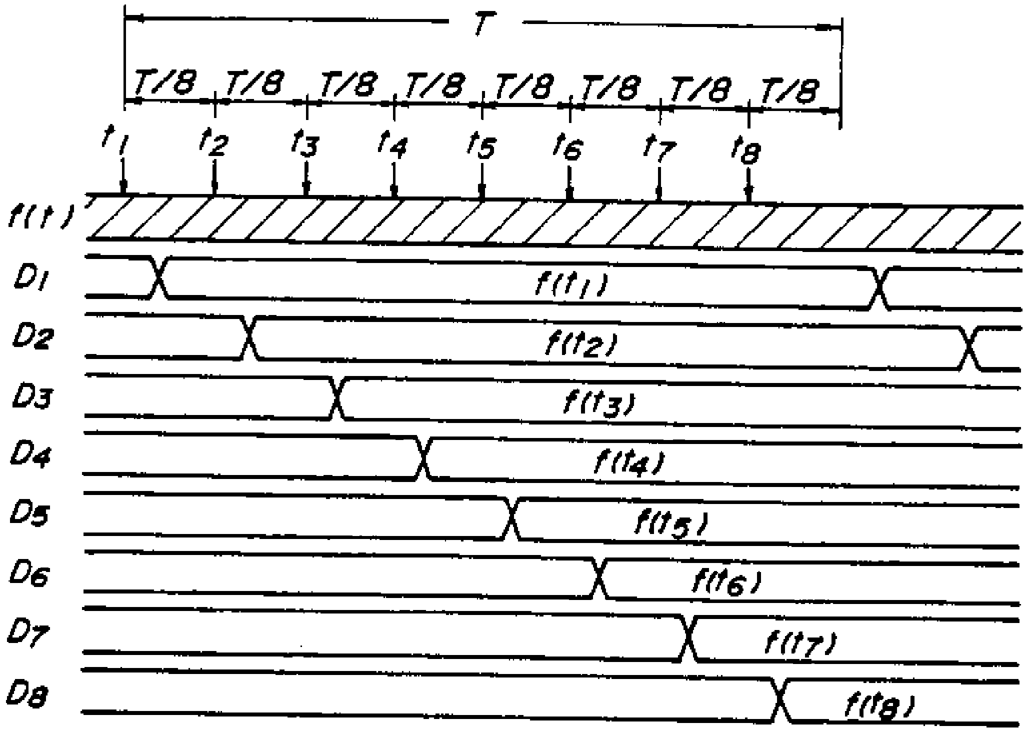
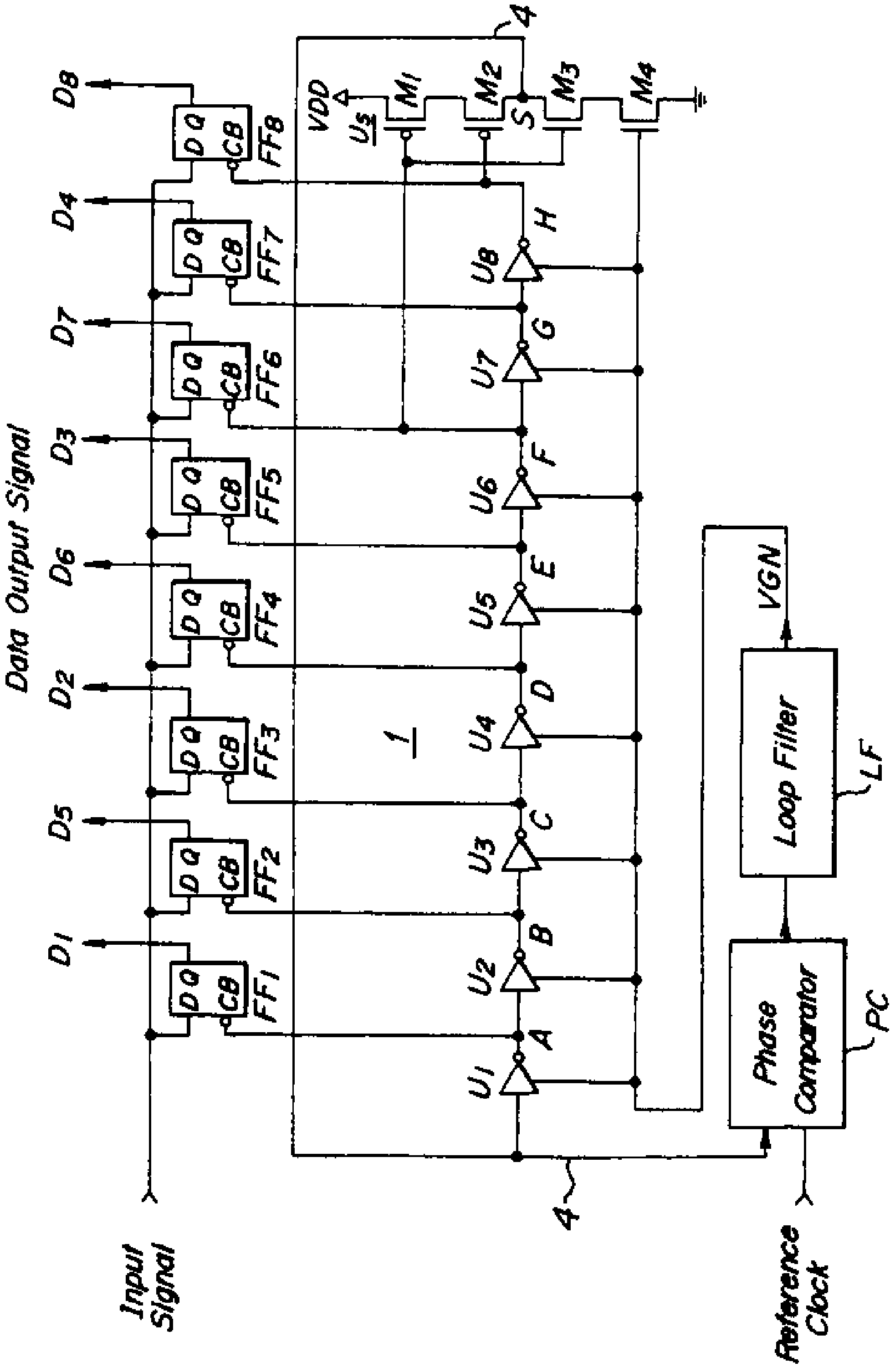

T
T/8
T/8
T/8
T/8
T/8
T/8
T/8
T/8
t1
t2
t3
t4
t5
t6
t7
t8
f(t)
D1
f(t1)
D2
f(t2)
D3
f(t3)
D4
f(t4)
D5
f(t5)
D6
f(t6)
D7
f(t7)
D8
f(t8)

FIG. 7


Data Output Signal
D1
D5
D2
D6
D3
D7
D4
D8
D Q
CB
FF1
FF2
FF3
FF4
FF5
FF6
FF7
FF8
U1
U2
U3
U4
U5
U6
U7
U8
A
B
C
D
E
F
G
H
1
4
VDD
Us
M1
M2
M3
M4
S
VGN
Loop Filter
LF
Phase Comparator
PC
Input Signal
Reference Clock