64-Ch TMC-VME Module Manual

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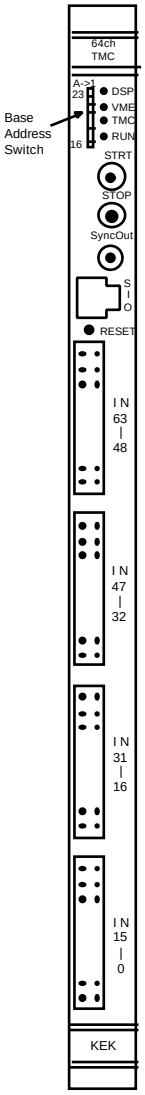
Introduction

TMC-VME module has been developed for the high-rate wire chamber applications[1]. The module uses custom developed LSI Time Memory Cell (TMC1004) [2, 3] as a time-to-digital converter. External FIFO buffers enables to store 64 μsec timing data. To convert raw TMC data to real timing data, a Digital Signal Processor Motorola DSP56002 is implemented.

A debug monitor program "TMCBUG" and a data acquisition program "TMCDAQ" were also developed and described in another document[4, 5].

References

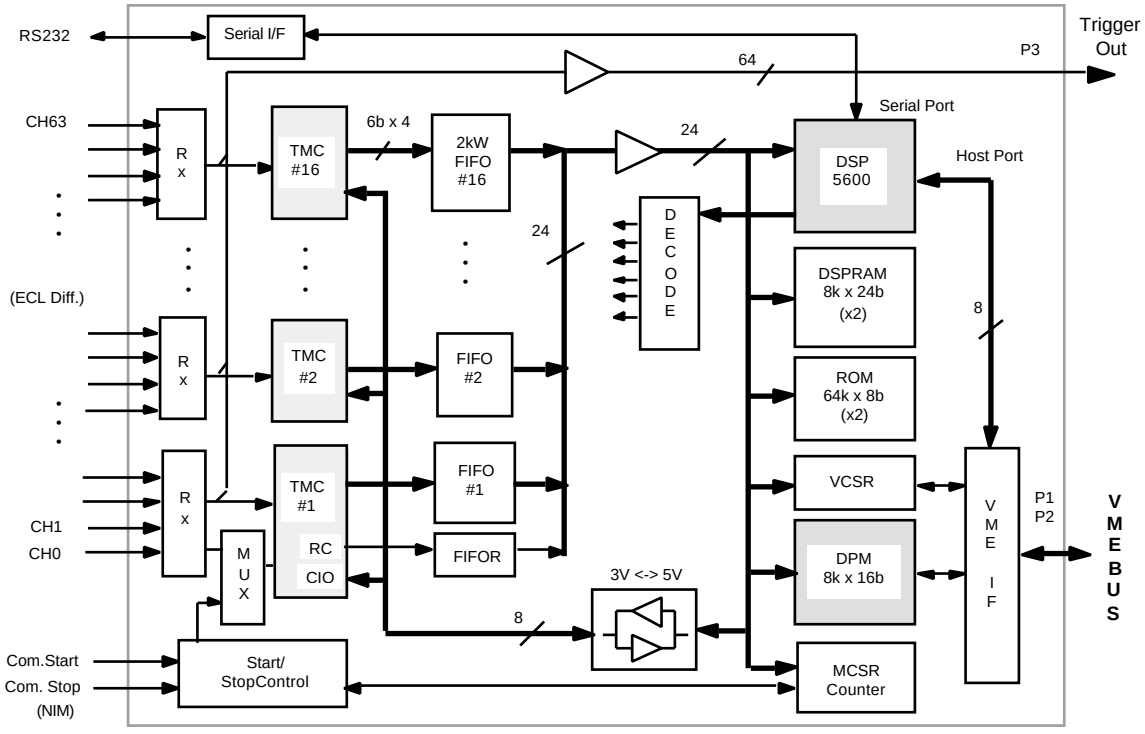
[1] Y. Arai and M. Ikeno; "A 64-ch Time Memory Cell Module witha DSP and a VME Interface", IEEE Nuclear Science Symposium, San Francisco, Nov. 1993. KEK Preprint 93-151.
[2] Y. Arai and T. Matsumura and K. Endo; "A CMOS 4 ch x 1 k Time Memory LSI with 1 ns/bit Resolution", IEEE Journal of Solid-State Circuits, Vol.27, No.3, March 1992, p359-364.
[3] "TMC1004 specification"
[4] "TMCBUG User's Manual"
[5] "TMCDAQ Program Manual"



64-Ch 9U TMC-VME Module

- 64 channels in 9U x 400 mm, Single-width VME module
- 1ns / bit least count, sigma = 0.52 ns time resolution
- 64 usec Full Scale
- Common stop or Common start operation
- Fast DSP56002 (31.25 MHz) for Data Formatting
- Serial I/F to DSP
- Rising/Falling edge detection and 6 bit encoded data output for each 32 ns data, or raw data dump for full data
- Stable operation for temperature, voltage variation
- VME Slave module (Dual Port Memory & Host I/F)
- ECL differential input for signal
- NIM level start / stop signal input
- NIM level trigger output
- TTL level output from P3 connector for trigger card
- OnCE Debugger Port

(This front-panel drawing is not scaled.)



TMC-VME Module Block Diagram

Specifications

Signal Inputs :	64 Channel. ECL-differential. Input Impedance 100 Ω. Four 34-pin Flat Cable Connector. Input signal is stretched to about 32 ns internally if the width is less than 32 ns.
START Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Start mode.
STOP Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Stop mode.
SYNC Output :	Lemo-type connector; NIM level. Generate synchronous output pulse with internal clock when started. Used for test purpose.
Trigger Output:	Stretched (32ns) input signal output. 64 signals. TTL low assert signals.
Least Time Count :	1 ns/bit
Maximum Time Range :	64 (ext. mem)+ 1 (TMC chip) μsec
Double Hit Resolution :	32 ns
Timing Measurement Error :	σ = 0.52 ns (including digitization error)
Integral Linearity Error :	< 1.5 bit
Differential Linearity :	< 0.2 ns
Variation of Slope : (time-to-digital conversion factor)	< 0.1 % (2.6 - 3.4 V) < 0.1 % (15 - 55 ˚C) < 0.1 % (chip to chip)
VME Base Address :	Base address of A16..A23 is switch (front panel) selectable.
Backplane connectors :	P1 = VME Bus, P2 = VME + Power pins P3 = Trigger output.
Packaging :	Euro Card 9U x 400 mm, single-width module.
Power Requirement :	+5 V x 3 A, -5.2 V x 1 A, 3.3 V x 1.2 A < 24 W

Input Connector Pin Assignment

Upper Connector (FJ1)

Pin No.	Assignment	Pin No.	Assignment
1	GND	2	GND
3	Ch 0 +	4	Ch 0 -
5	Ch 1 +	6	Ch 1 -
7	Ch 2 +	8	Ch 2 -
9	Ch 3 +	10	Ch 3 -
11	Ch 4 +	12	Ch 4 -
13	Ch 5 +	14	Ch 5 -
15	Ch 6 +	16	Ch 6 -
17	Ch 7 +	18	Ch 7 -
19	Ch 8 +	20	Ch 8 -
21	Ch 9 +	22	Ch 9 -
23	Ch 10 +	24	Ch 10 -
25	Ch 11 +	26	Ch 11 -
27	Ch 12 +	28	Ch 12 -
29	Ch 13 +	30	Ch 13 -
31	Ch 14 +	32	Ch 14 -
33	Ch 15 +	34	Ch 15 -

Upper Middle Connector (FJ2)

Pin No.	Assignment	Pin No.	Assignment
1	GND	2	GND
3	Ch 16 +	4	Ch 16 -
5	Ch 17 +	6	Ch 17 -
7	Ch 18 +	8	Ch 18 -
9	Ch 19 +	10	Ch 19 -
11	Ch 20 +	12	Ch 20 -
13	Ch 21 +	14	Ch 21 -
15	Ch 22 +	16	Ch 22 -
17	Ch 23 +	18	Ch 23 -
19	Ch 24 +	20	Ch 24 -
21	Ch 25 +	22	Ch 25 -
23	Ch 26 +	24	Ch 26 -
25	Ch 27 +	26	Ch 27 -
27	Ch 28 +	28	Ch 28 -
29	Ch 29 +	30	Ch 29 -
31	Ch 30 +	32	Ch 30 -
33	Ch 31 +	34	Ch 31 -

Lower Middle Connector (FJ3)

Pin No.	Assignment	Pin No.	Assignment
1	GND	2	GND
3	Ch 32 +	4	Ch 32 -
5	Ch 33 +	6	Ch 33 -
7	Ch 34 +	8	Ch 34 -
9	Ch 35 +	10	Ch 35 -
11	Ch 36 +	12	Ch 36 -
13	Ch 37 +	14	Ch 37 -
15	Ch 38 +	16	Ch 38 -
17	Ch 39 +	18	Ch 39 -
19	Ch 40 +	20	Ch 40 -
21	Ch 41 +	22	Ch 41 -
23	Ch 42 +	24	Ch 42 -
25	Ch 43 +	26	Ch 43 -
27	Ch 44 +	28	Ch 44 -
29	Ch 45 +	30	Ch 45 -
31	Ch 46 +	32	Ch 46 -
33	Ch 47 +	34	Ch 47 -

LowerConnector (FJ4)

Pin No.	Assignment	Pin No.	Assignment
1	GND	2	GND
3	Ch 48 +	4	Ch 48 -
5	Ch 49 +	6	Ch 49 -
7	Ch 50 +	8	Ch 50 -
9	Ch 51 +	10	Ch 51 -
11	Ch 52 +	12	Ch 52 -
13	Ch 53 +	14	Ch 53 -
15	Ch 54 +	16	Ch 54 -
17	Ch 55 +	18	Ch 55 -
19	Ch 56 +	20	Ch 56 -
21	Ch 57 +	22	Ch 57 -
23	Ch 58 +	24	Ch 58 -
25	Ch 59 +	26	Ch 59 -
27	Ch 60 +	28	Ch 60 -
29	Ch 61 +	30	Ch 61 -
31	Ch 62 +	32	Ch 62 -
33	Ch 63 +	34	Ch 63 -

Backplane Connector Pin Assignment

P1 : VME Bus

Pin	ROW A	ROW B	ROW C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

+5 V = 4 pins, -12 V = 1 pin, +12 V = 1pin,
GND=8 pins

P2 : VME Bus + Power/GND (92.12.4 revised)

Pin	ROW A	ROW B	ROW C
1	-2 V	+5 V	(reserved)
2	-2 V*	GND	(reserved)
3	-2 V	(reserved)	GND*
4	GND*	A24	-5.2 V*
5	dsig1+	A25	-5.2 V
6	dsig1-	A26	-5.2 V
7	-5.2 V*	A27	GND*
8	GND	A28	(reserved)
9	sig1	A29	(reserved)
10	GND*	A30	GND*
11	sig2	A31	-2 V
12	sig3	GND	-2 V
13	-5.2 V*	+5 V	-2 V*
14	GND	D16	-2 V
15	sig4	D17	-2 V
16	GND*	D18	GND*
17	sig5	D19	(reserved)
18	sig6	D20	GND
19	-5.2 V*	D21	-5.2 V*
20	dsig2+	D22	-5.2 V
21	dsig2-	D23	-5.2 V
22	GND*	GND	GND*
23	sig7	D24	+3.3 V
24	+5 V	D25	+3.3 V
25	+5 V*	D26	GND*
26	+ 5 V	D27	+3.3 V
27	+5 V	D28	+3.3 V
28	GND*	D29	GND*
29	sig8	D30	+3.3 V
30	GND	D31	GND*
31	GND*	GND	+3.3 V
32	+3.3 V	+5 V	+3.3 V

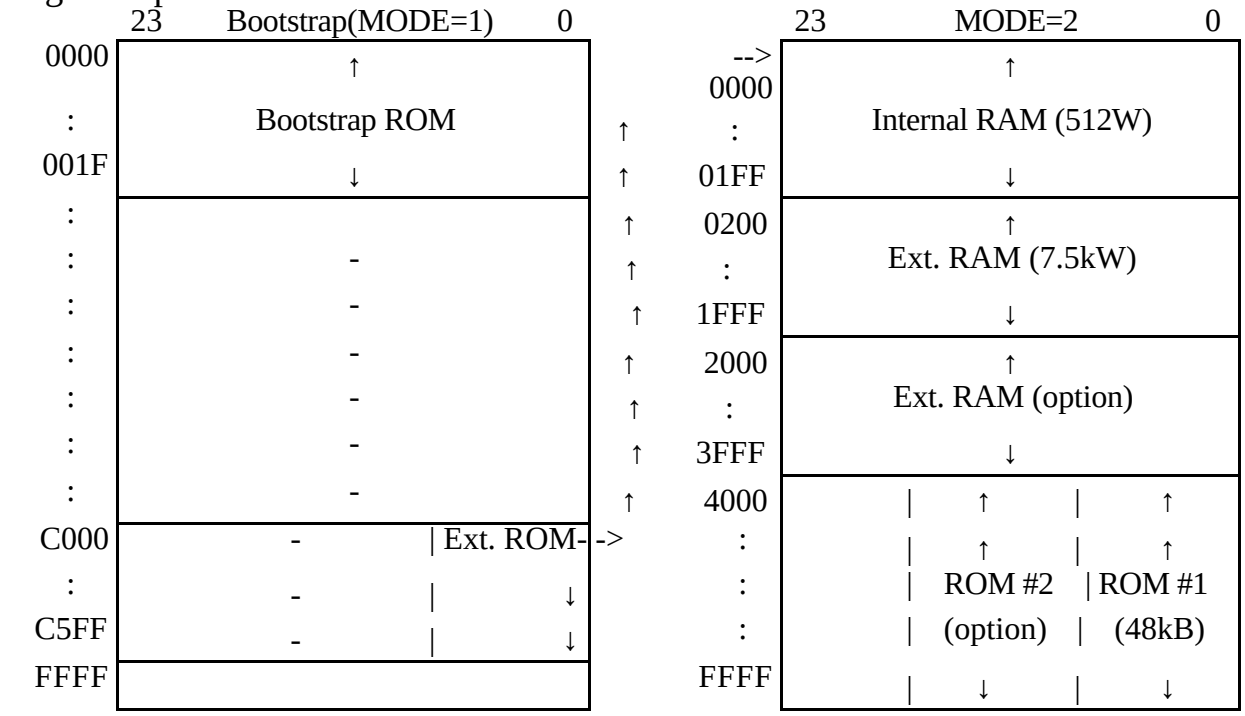
+5 V = 8 pins, -2 V = 8 pins, -5.2 V = 9 pins, +3.3 V = 8 pins, GND= 22 pins, 2 diff signal pairs, 8 single-end signals.
* : VXI standard power pins.

P3 : Trigger Output

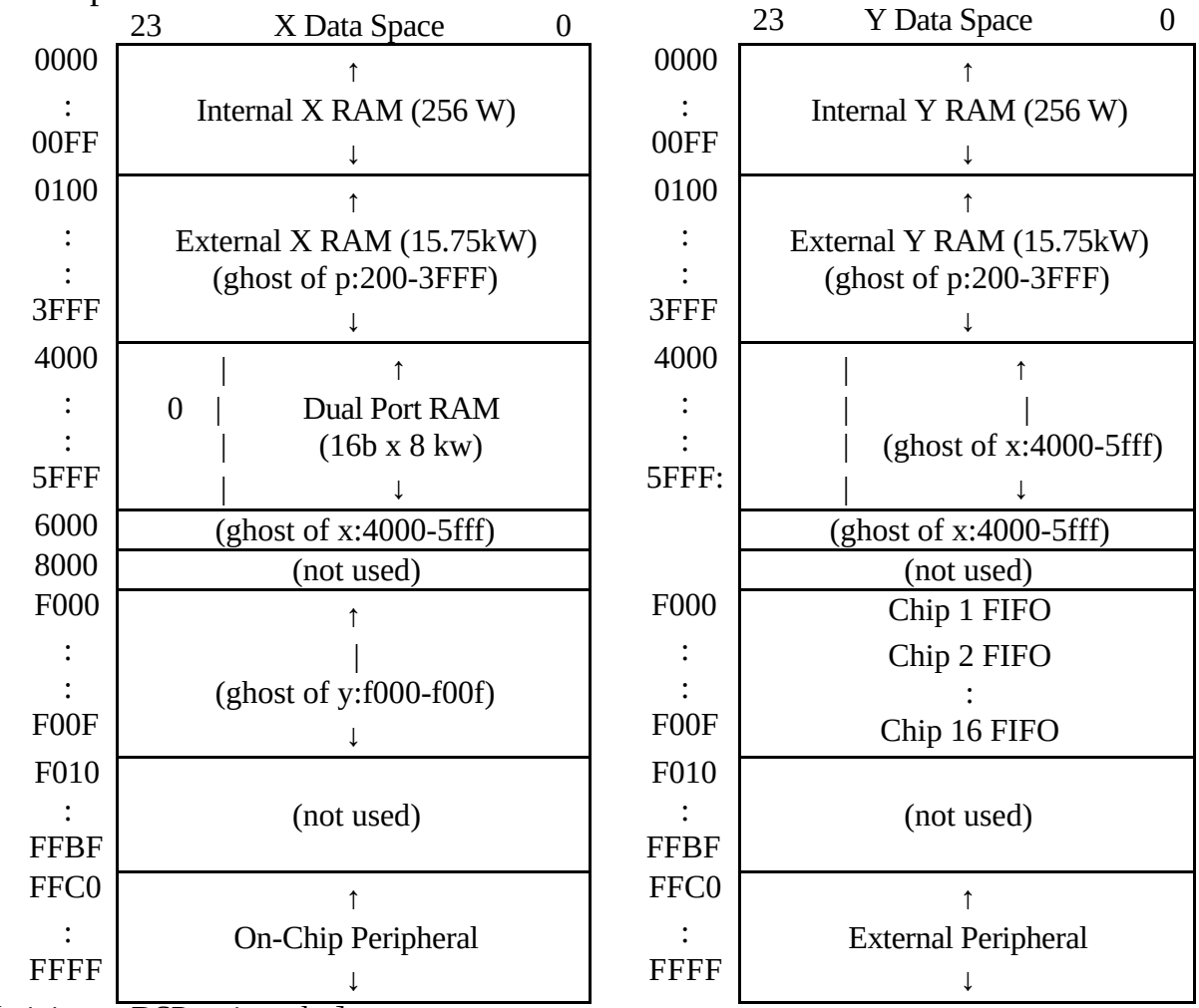
Pin	ROW A	ROW B	ROW C
1	CH 0 Out	GND	CH 1 Out
2	CH 2 Out	GND	CH 3 Out
3	CH 4 Out	(not used)	CH 5 Out
4	CH 6 Out	(not used)	CH 7 Out
5	CH 8 Out	GND	CH 9 Out
6	CH 10 Out	GND	CH 11 Out
7	CH 12 Out	(not used)	CH 13 Out
8	CH 14 Out	(not used)	CH 15 Out
9	CH 16 Out	GND	CH 17 Out
10	CH 18 Out	GND	CH 19 Out
11	CH 20 Out	(not used)	CH 21 Out
12	CH 22 Out	(not used)	CH 23 Out
13	CH 24 Out	GND	CH 25 Out
14	CH 26 Out	GND	CH 27 Out
15	CH 28 Out	(not used)	CH 29 Out
16	CH 30 Out	(not used)	CH 31 Out
17	CH 32 Out	GND	CH 33 Out
18	CH 34 Out	GND	CH 35 Out
19	CH 36 Out	(not used)	CH 37 Out
20	CH 38 Out	(not used)	CH 39 Out
21	CH 40 Out	GND	CH 41 Out
22	CH 42 Out	GND	CH 43 Out
23	CH 44 Out	(not used)	CH 45 Out
24	CH 46 Out	(not used)	CH 47 Out
25	CH 48 Out	GND	CH 49 Out
26	CH 50 Out	GND	CH 51 Out
27	CH 52 Out	(not used)	CH 53 Out
28	CH 54 Out	(not used)	CH 55 Out
29	CH 56 Out	GND	CH 57 Out
30	CH 58 Out	GND	CH 59 Out
31	CH 60 Out	(not used)	CH 61 Out
32	CH 62 Out	(not used)	CH 63 Out

Address Map (DSP Space)

Program Space



Data Space



[minimum DSP wait cycles]
X/Y/P-memory = 0, IO = 1, ROM-access = 4. (Recommended BCR = $0001)

External Peripheral(Y Space)

	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	reg. name
FFC0	(unknown) | 1 | Chip 0 CSR0*	CSR00
FFC1	(unknown) | 1 | Chip 1 CSR0*	CSR01
:	:	:
FFCF	(unknown) | 1 | Chip 15 CSR0*	CSR0F
FFD0	(unknown) | 1 | Chip 0 CSR1*	CSR10
FFD1	(unknown) | 1 | Chip 1 CSR1*	CSR11
:	:	:
FFDF	(unknown) | 1 | Chip 15 CSR1*	CSR1F
FFE0	(unknown) | 1 | Chip 1 CSR2*	CSR20
FFE1	(unknown) | 1 | Chip 5 CSR2*	CSR21
:	:	:
FFEF	(unknown) | 1 | Chip 15 CSR2*	CSR2F
FFF0	| Count Reg. (11:0)	CNTR
FFF1	| MCSR (11:0)	MCSR
FFF2	|VCSR(2:0)	VCSR
FFF3	(unknown) | 1 1 1 | FIFOR(4:0)*	FIFOR
FFF4	↑	
:	(not used)	
FFFF	↓	

Address Map (VME Space)

DSP Addr	VME Addr	15 Upper byte 8 7 Lower byte 0	addr. symbol
$4000	x+0	Dual Port Memory	DPM
:	:		
:	:		
$5FF7	x+3FEE		
$5FF8	x+ 3FF0	DPM IRQ Vectors	DPMIRQ
:	:		
$5FFF	x+3FFE		DPME
	x+4000	^	
	:	(not used)	
	x+FEFE	V	
$FFF2	x+FF00	| VCSR .	VCSR
	:	(not used)	
	x+FFEE	V	
	x+FFF0	| Interrupt Control Register	ICR
	x+FFF2	| Command Vector Register	CVR
	x+FFF4	| Interrupt Status Register	ISR
	x+FFF6	(Host Port) | Interrupt Vector Register	IVR
	x+FFF8	| -	
	x+FFFA	| Rx/Tx Byte Register H	RXH/TXH
	x+FFFC	| Rx/Tx Byte Register M	RXM/TXM
	x+FFFE	| Rx/Tx Byte Register L	RXL/TXL

x = 0, $10000, $20000, ..., $FF0000 (upper 8 bit base address is switch selectable)

Module CSR(MCSR) Bit Assignment

Bit	Name	R/W	Contents
0	WSTRT	R/W	Start TMC Running
1	DSTRT	R/W	Start Recording
2	DSTOP	R/W	Stop Recording
3	CSTSP	R/W	Common Start (=1), Common STOP (=0) mode.
4	EMPTY	R	FIFO EMPTY Flag
5	AFAE	R	FIFO AF/AE Flag
6	HFULL	R	FIFO HF Flag
7	FULL	R	FIFO FULL Flag
8	OVWEN	R/W	FIFO Overwrite Enable
9	FRST	R/W	FIFO Reset
10	TRST	R/W	TMC Reset
11	DBG	R/W	Debug Status read / Indicator write

VME CSR(VCSR) Bit Assignment

Bit	Name	from VME BUS	from DSP	Contents
0	MRST	W	W	Reset all circuit in TMC-VME Module
1	INTM	R/W	R/W	INTM status
2	INTMEN	R/W	R/W	INTM Interrupt Enable

TMC CSR Registers

bit	5	4	3	2	1	0
CSR0	MOD1	MOD0	SIO3	SIO2	SIO1	SIO0
CSR1	Read Counter Value [RC]					
CSR2	Write Counter Value [WC]					
CSR3	-					

* CSR0

• SIO3 ~ 0 : Serial I/O bits. These bits are valid only in the serial i/o mode. One bit data for each channel is read/written through this bit from/to the address pointed by the read counter(row position) and the write counter(column position). (read/write)

• MOD0,1 : MODE = [MOD1,MOD0]. MODE = 0 --- Stand alone mode, MODE = 1 --- Slave mode, MODE = 2 --- Serial i/o mode., MODE = 3 Test Pad mode. [read/write]

* CSR1

• RC : Read counter value. The contents of the read counter are set through this register. The value read back indicates present value of the read counter. In Slave mode, the contents of the counter are incremented after the read/write operation. This register also works as a row address register in the serial read/write mode. [read/write]

* CSR2

• WC : Write counter value. The contents of the write counter are set through this register. Present value of the write counter is read back. The counter is incremented by WCLK signal during WSTART is asserted. This register also works as a column address register in the serial read/write mode. [read/write]

Mode

There are 4 modes of operations in the TMC1004. These modes are selected via bits 4 and 5 in the CSR0 register. Operations of these modes are explained below.

• MODE = 0 (Stand alone Mode) : Readout cycle will be synchronous to the write cycle (= clock cycle). Encoded data are read out through DOUTx*pins during the DS* signal is asserted.

• MODE = 1 (Slave Mode) : Readout cycle will be asynchronous to the clock and controlled by the DS* signal. Usually, this mode requires stopping write cycle before starting read cycle. Encoded data are read out through DOUTx* pins.

• MODE = 2 (Serial read/write Mode) : This mode is used mainly for testing each bit in the memory. Data are read/write from/to the address pointed by the CSR1(row address) and CSR2(column address) through bit 0 ~ 3 in the CSR0. Bit 0 corresponds to the data in the CH0 and bit 1 corresponds to CH1 and so on.

• MODE = 3 (Test Pad Mode): This mode is also used for test purpose but only in wafer level test. Addresses are supplied through APAD0 ~ APAD9 and data are read out through CSR0 as same manner as the Serial read/write mode. By setting the TPAD to high level, this mode is automatically selected.

Encoded Data

Internal data of the TMC is not directly appear in the output pins. The data is encoded as shown in the Table 1. Bit position at which the data is changed from "0" to "1" is encoded in the least 5 bits. Most significant bit shows whether the first bit is "0" or "1". When the data has changed from "0" to "1" at the edge of the row, for example all the data in row N is all "0" and all data in row N+1 is all "1", you can recognize it as the encoded data in row N is "000000" and in row N+1 is "100000".

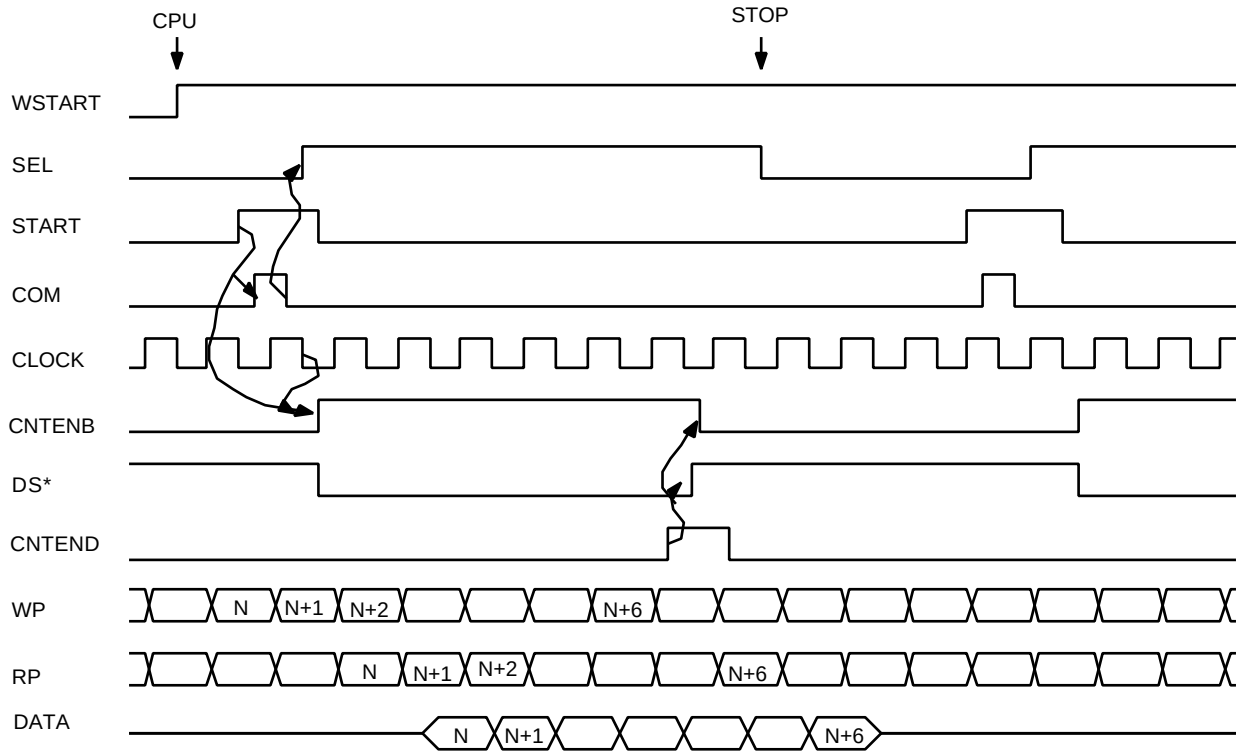
Table 1 Data Encoding

Bit Pattern	Encoded Data					
3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1						
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0	0	0	0	0	0	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0	0	0	0	0	1	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0	0	0	0	0	1	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0 0	0	0	0	1	0	0
:	:					
:	:					
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	1	1	1	1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	0	0	0	0	0
(not appear)	1	0	0	0	0	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 1	1	0	0	0	1	0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x 1	1	0	0	0	1	1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x x 1	1	0	0	1	0	0
:	:					
:	:					
1 0 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1	1	1	1	1	1	1

x..xx..x = 0..01..1

Timing Diagram

[Common Start Mode]



[Common Stop Mode]