Submitted to the IEEE Transactions on Nucl. Sci., IEEE Nuclear Science Symposium, San Francisco, Oct. 1995.

A VME 32 ch Pipeline TDC Module with TMC LSIs

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Abstract

A new 32-channel pipeline TDC module, which implements custom-developed Time Memory Cell LSIs, has been developed for high-rate wire-chamber applications. The module has achieved a 370 ps time resolution, and records data for a period of 3.2 µsec. To handle the large data size, a digital signal processor (DSP56002) is implemented in the module. Most of the control logic is implemented in two complex PLDs to achieve a density of 32 channels in a single-width, double-height VME module.

I. INTRODUCTION

Pipeline TDC modules with less than a 1 ns time resolution have been in demand for wire-chamber readout in recent high-rate experiments. Since our development of a 64-channel pipeline TDC module on a 9U x 400 mm board [1], we have received many requests for a further reduction of the cost and a module of the standard double-height VME size.

The 9U TDC module utilized a Time Memory Cell (TMC) chip of TMC1004 [2, 3,], which is a full-custom chip developed with 0.8µm CMOS technology and has a σ=520ps time resolution. Since the TMC1004 has only a 1 µsec buffer within the chip, we added an external FIFO to the TMC1004 in order to increase the time range. The module has been working successfully and has been used in several test experiments. However, the large board size and the relatively high cost of the TMC1004 and the FIFO are preventing any further spread.

On the other hand, we developed a new TMC chip called the TMC-TEG3 [4] using Toshiba's 0.5 µm CMOS Sea-of-Gate process. The cost of the chip was reduced by almost one order due to commercial gate-array technology, and the time range has been increased to 3 ~ 10 µsec, depending on the clock frequency. Furthermore, the chip can record both rising- and falling-edge timings, and achieved a resolution of σ=250ps.

We have thus decided to develop a new 32-channel TMC-VME module (Fig. 1) using the TMC-TEG3 chip. To increase the data-transfer speed and to manipulate data, a high-speed digital signal processor (DSP), the Motorola DSP56002, is used. The board is 6U x 160 mm single-width, double-height VME size. We use two complex PLDs (Lattice ispLSI) to reduce the board area of the control circuits, and have achieved a density of 32 channels in the module. The module has a VME slave interface with a block-transfer capability and a dual-port memory (DPM) which can be accessed both from the DSP and the VME bus. The power consumption is less than 8W.

The circuit design is given in section II. The software environments for the ispLSI and DSP programs are described in section III. Finally, the performance of the module is described in section IV.

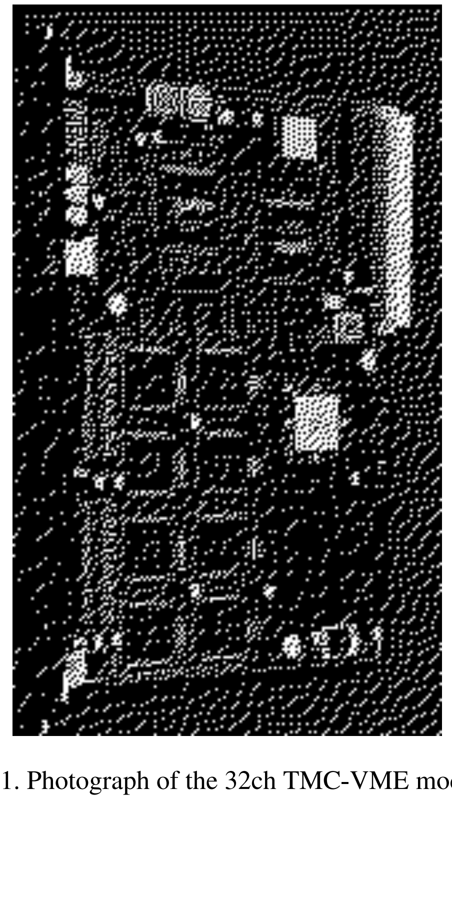

Fig. 1. Photograph of the 32ch TMC-VME module.

II. CIRCUIT DESIGN

A. TMC-TEG3 chip

The module has 8 TMC-TEG3 chips, which are operated at a 3.3 V power-supply voltage. The chip contains 4 channels of circuit. A conceptual view of each channel is shown in Fig. 2. An asymmetric ring oscillator is controlled with a phase-locked loop (PLL), and generates 32 precise timing signals, each of which is delayed by 1/32 of the clock cycle. The frequency lock range of the PLL is between 10 MHz and 50 MHz. Both the rising- and falling-edge times are encoded and stored in 128-word dual-port memories (DPM). Although the TMC records all of the timing information, a second edge which appeared within the same cycle will be neglected at the encoding stage.

Depending on a clock frequency, we could have a high resolution with a shorter time range or vice verse. At a 40 MHz clock, TMC has a least count of 0.78 ns/bit, a time resolution of σ=250ps and a time range of 3.2μsec.

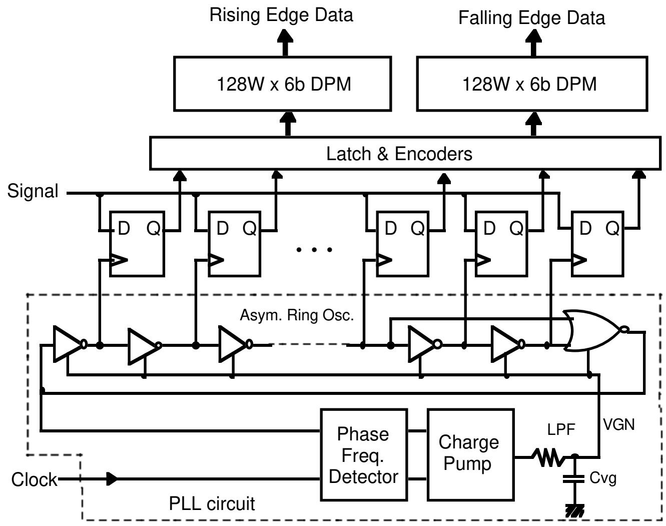

Fig 2. Conceptual view of the TMC-TEG3 chip.

B. Module Structure

The specifications of the TMC-VME module are summarized in table 1. We used the same DSP (DSP56002) as that used in the 9U TMC-VME module. The DSP can perform 20 MIPS at 40 MHz clock, and up to 3 instructions can be executed in a single instruction cycle. The DSP has 56-bit accumulators, a 24-bit external data bus and three address space: Program (P-), X-data, and Y-data space. Figure 3 shows a memory map of the DSP.

There are two external RAMs (DSPRAM: 8k x 24 bit) which can be accessed from the DSP without a wait cycle. Since there is plenty of address space, the DSPRAM is mapped to all three spaces as much as possible. The user can assign the address space of the RAM as either P-, X- and/or Y- data space in the software. This flexibility of mapping is useful for improving the performance. The monitor software is programmed in a PROM (64k x 8 bit). There are three PROM sockets in total. A dual-port memory (DPM: 16kB), which can be accessed from both the DSP and VME, is provided as a data buffer.

TMC data consist of 6bit: a hit bit plus 5 bits of fine timing. Coarse timing is derived from the location of the data. By using the hit-bit information, a fast scan of data will be possible.

A block diagram of the TMC-VME module is shown in Fig. 4. Since the TMC operates at 3.3 V, there are 3.3V/5V-level converters between the TMC and DSP bus. On the other hand, since the output signals of the TMC chip have a sufficient voltage swing to drive the TTL device, these are connected directly. Although both the TMC and the DSP operate at 40 MHz clocks in the default setting, the clock frequency of the TMC can be changed independently of the DSP frequency by replacing the crystal oscillator.

The module has a serial (RS-232C) port at the front panel and an 8-bit parallel host port in the VME space. Input signals are received by fast comparators (MAX901) which receive ECL or small differential signals (> Δ100mV) in a common voltage range of $\pm$3V.

The expansion bus timing for the P-, X-, Y-, and I/O space can be programmed individually in the DSP56002. In this module, all of the memory, except for the I/O space, ROM and TMC, can be accessed without a wait cycle. One wait cycle is required for access to the I/O space and TMC, and several wait cycles for access to the ROM.

There are several interrupt sources to the DSP. In addition to the interrupt created within the DSP chip (stack error, software interrupt, etc.), the serial port and host port can cause interrupts to the DSP.

For an interrupt to the VME, there is an interrupt signal (INTM), which is controlled by bits 1 and 2 of the VME control and status register (VCSR). This interrupt is provided to communicate with the VME master for handling event data.

Table. 1. Specifications of the TMC-VME module

• TMC chip	TMC-TEG3 (10 - 50 MHz)
• DSP	DSP56002 (40 MHz)
• DSP RAM	MCM56824 (8kx24b)x2 [0 wait]
• ROM	27512 (64kB) x 3 [4 waits]
• Dual-Port Memory	IDT7025 (16kB) [0 wait]
• I/O	Serial and 8-bit host port
• Signal Inputs	32ch (ECL) differential.
• Start/Stop Inputs	NIM level. Lemo connectors.
• Time Resolution	σ = 370 ps
• Least Time Count	0.78 ns/bit (@40MHz)
• Max. Time Range	3.2 μsec (@40MHz)
• Two Hit Resolution	< 25 nsec (@40MHz)
• VME I/F	P1 connector. A24/D16 Interrupt to/from VME Block transfer
• Packaging	6U x 160mm (double-height), single-width
• Power Consumption	< 8W (-12Vx0.16A, +5Vx1.4A)

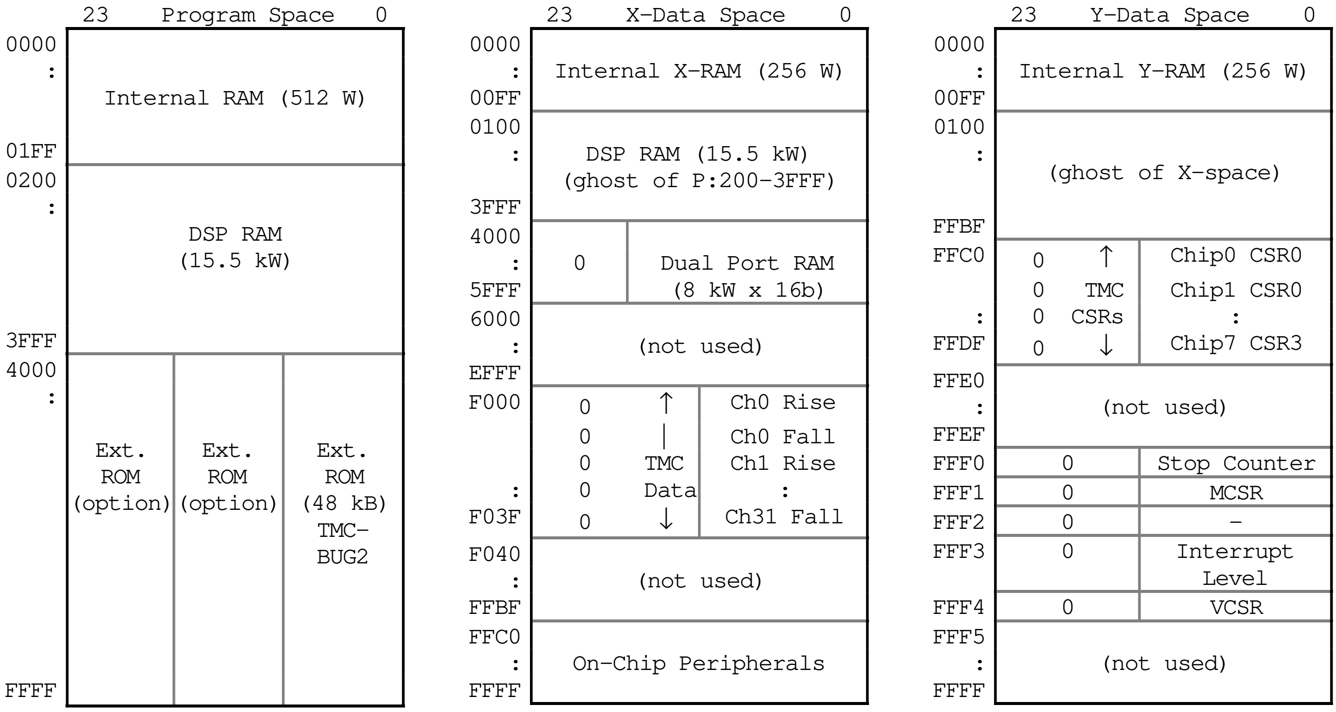

Fig.3. DSP memory address map.

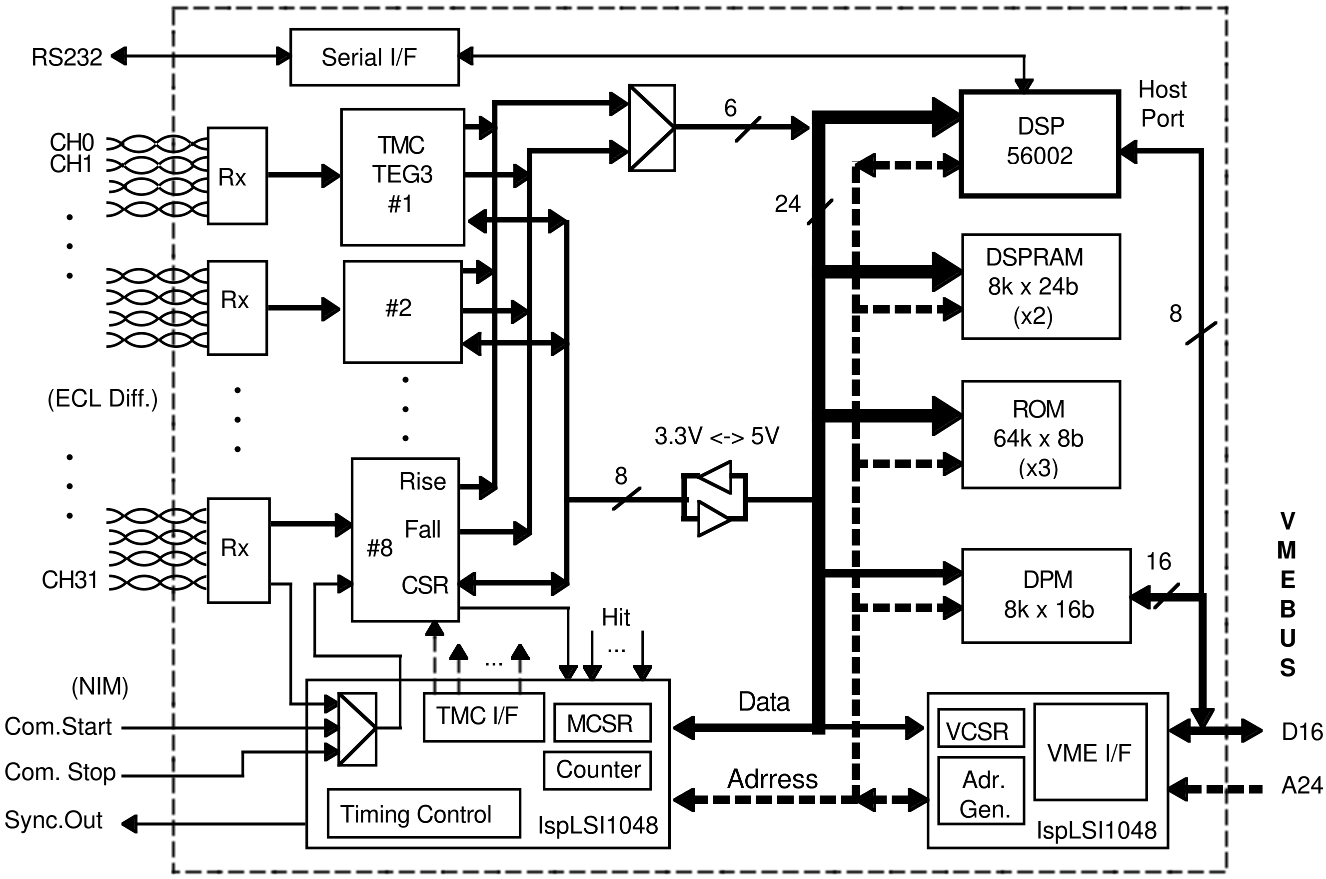

Fig. 4. Block Diagram of the 32 ch TMC-VME module.

The interrupt vectors of the module interrupt are set at the last 8 addresses of the DPM. The host port can also generate a VME interrupt from the DSP.

C. TMC Interface

The TMC interface part is implemented in an ispLSI, and functions as a DSP address decoder, a TMC start/stop controller, a module control and status register (MCSR), a time counter and a common timing multiplexer.

The input of the channel 31 is connected to the common timing multiplexer, and is used to record both the CH31 signal and a common stop (or start) signal.

In a common stop mode, an external signal is recorded in the TMC until the common stop signal arrives. When the stop signal arrives, the multiplexer is changed so as to select the stop signal. Then, the stop signal is recorded in the last two words of the channel 31 data.

In the common start mode, the common start signal is recorded in the first two words of the channel 31 data. The multiplexer is then changed so as to select the CH31 signal. There is a 7-bit stop counter which is used for counting the recording time (number of TMC clock cycles). The data recording stops when the count reaches zero. The user can also keep on recording external signals while the stop counter is not running. The counter starts a count down when the common start signal arrives. Thus, the user can obtain signal information prior to the start signal, as in a logic analyzer.

Table 2 shows the bit assignment of the module control and status register (MCSR). The COMST bit selects the common stop or the common start mode. The TRUN bit indicates that the TMC is running (recording). In the common stop mode the WRUN bit shows the same status as the TRUN, while in the common start mode it indicates that the common start signal has arrived and the counter is counting down. The DSTART bit is used to start data recording from the DSP, or as a replacement of the common start signal. The DSTOP bit is used to stop data recording from the DSP, or as a replacement of the common stop signal..

D. VME Interface

The module has an A24/D16 address/data size. The base address of the module is set by switches for the upper 8-bit address signals (A16-A23). Thus, the module uses a 16-bit address space. An address map of the VME space is shown in Fig. 5. The lower 16k bytes are assigned to the DPM, and the higher 16 addresses are used for the host port registers.

The VME interface is implemented in another ispLSI, and have the functions of a VME slave controller, an interrupt handler, a block-transfer controller and a VME control and status register (VCSR). To generate an internal address in the VME block-transfer mode, an 8-bit counter is implemented. Table 3 shows the bit assignment of the VCSR. A reset signal is asserted by setting the MRST bit of the VCSR. This register can be accessed from both DSP and VME.

Address	15 UpperByte 8		7 Lower Byte 0
xx0000 : xx1FF0	Dual Port Memory (16 kB)		
xx1FF2	-		Level 1 Interrupt Vector
:	-		:
xx1FFE	-		Level 7 Interrupt Vector
:	-		
xxFF00	0		-
xxFF02	0		Interrupt Level
xxFF04	0		VCSR
:	-		
xxFFF0	0	↑	Interrupt Control Reg.
xxFFF2	0	|	Command Vector Reg.
xxFFF4	0	|	Interrupt Status Reg.
xxFFF6	0	Host	Interrupt Vector Reg.
xxFFF8	0	Port	-
xxFFFA	0	|	Rx/Tx Byte Reg. H
xxFFFC	0	|	Rx/Tx Byte Reg. M
x+FFFE	0	↓	Rx/Tx Byte Reg. L

Fig. 5 VME-space address map. The base address ‘xx0000’ is set by switches for the upper 8-bit address bit (A16-A23)

Table 2. Module control and status register (MCSR) bit assignment.

Bit	Name	R/W	Common stop mode (COMST=0)	Common start mode (COMST=1)
0	DEBGSW	R	Debug switch status	
1	DEBLED	R/W	Debug LED	
2	TRUN	R	TMC is running	
3	WRUN	R	TMC is running	Count down
4	DSTART	R/W	Start TMC	Com.start signal
5	DSTOP	R/W	Com.stop signal	Stop TMC
6	COMST	R/W	Recording Mode	
7	TRST	R/W	Rest TMC	

Table 3. VME control and status register (VCSR) bit assignment.

Bit	Name	R/W	Contents
0	MRST	W	Reset all circuits
1	INTM	R/W	INTM interrupt status
2	INTMEN	R/W	INTM interrupt enable

III. SOFTWARE ENVIRONMENT

A. ispLSI programming

The ispLSI is programmed on board through an isp download cable from a personal computer. The programming language ABEL (Data I/O Co.) is used to describe the functions of the chip. This flexibility of the logic design led us to the first successful PC board. The first PC board required only one patch.

The ispLSI1048 has 8000 PLD gates, 192 macrocells and 96 I/O pins. We used 70% and 80% of the gate in the TMC and the VME interfaces, respectively.

B. DSP Program

We used a cross assembler to develop DSP programs. The assembler runs on a Macintosh or a personal computer, and produces object files. These files are down loaded to the TMC-VME module through the serial or the host port.

A monitor program "TMCBUG", which was developed for the 9U TMC-VME module, was transferred to the present module, and named "TMCBUG2". The monitor program handles read(write) from(to) memory and registers, sets breakpoints, traces, downloads programs, and handles terminal and host port I/O's. The TMCBUG2 is programmed in a ROM, and a bootstrap program moves the main codes from the ROM to the DSPRAM at the startup time. To minimize the required RAM area, some routines are loaded into an overlay area at the execution time. Several custom commands used to check the contents of TMC's have also been added. The present "TMCBUG2" occupies only 3k words of the program RAM space.

A prototype data-acquisition program has been developed. The program runs in the common start or common stop mode, and can handle multiple hits in a channel. The program obtains run parameters from the terminal or the DPM, and waits for an event. When event data are available, the DSP searches the start (or stop) timing from the Ch31 data. Then, DSP searches the hit point from all channels. If the DSP finds a hit point, DSP writes the time of the hit to the DPM. Optionally, a user can subtract offset values channel by channel. When the data transfer is finished, the DSP sets a flag (or cause interrupt) to notify the VME master.

IV. PERFORMANCE

A.. Time Resolution

The timing resolution of the TMC-TEG3 chip is 250 ps RMS for a single hit at a clock frequency of 40 MHz. Since we need both the start/stop time and the hit time for a complete measurement, the timing resolution is cumulative of two measurement errors.

Figure 6 shows the timing resolution of the TMC-VME module from a measurement of the time between a common start signal and a hit. The theoretical error distribution becomes triangular in shape, as shown in the Fig. 6.

Although the expected resolution from the TMC chip is 354 ps (250 ps x $\sqrt{2}$), we obtained an experimental value of 370 ps. Thus, although some additional errors are added in the module, they are almost negligible in an actual measurement.

B. Data Processing Time

Although the TMC chip is designed to operate without any deadtime, this paticular module requires some data-processing time, since the bandwidth of the VME is not sufficient to transffer all of the data in real time.

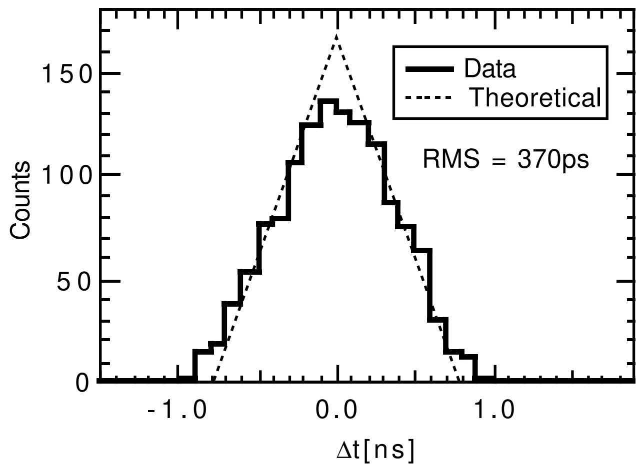

Fig. 6. Time resolution from a measurement of the time between a common start and a hit signal. The frequency of the TMC clock is 40 MHz and a LSB is 0.78 ns.

The data-processing time also depends greatly on the software, especially in a DSP. Here we give an example of the time to process all of the hit information in the TMCs and to write necessary data into the DPM.

The data-taking speed depends on the number of hits, channels and time range. The processing time to obtain rising-edge timing was measured and can be equated as follows :

$$\text{Time} \approx 0.4\mu\text{sec x (\#Ch) x (\#Rcycle)} + 4\mu\text{sec x (\#Hit)},$$

where #Ch is the number of channels to read, #Rcycle is a recorded cycle in the TMC, and #Hit is the number of hits in the data. For example, if we handle 32 channels inputs, 100 cycle of recording (2.5 μsec) and 32 hits, the data processing time will be about 1.4 msec.

ACKNOWLEDGMENTS

The authors wish to thank T. Kondo and T. K. Ohska for their continuous support and encouragement during this project.

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