LOI Progress Report

– Ready for first beam test at the SP6 in February 2011 –

March 9, 2011

1. Introduction

Problems in the last experiments in November, 2010 on the current trip and overshoot of the buck regulator output current were solved by sufficiently mating the LOI HPD with the cavity. Stable operation was then established in a swept mode with 4.8kV-peak at the gap voltage. Although there are remaining tasks on the LOI such as cavity tuning at later acceleration cycle and establishing cavity lock system, the LO became almost ready for the beam test on the beam induced voltage. Machine time was for the first time allocated from 0:00am-8:00am on Friday, February 25. However, unfortunately, beam was not injected into synchrotron due to an unexpected beam loss at the Linac Tank 2.

In the following sections are reported, investigation of current trip and overshoot of the buck regulator in section 2, experimental setup in section 3, experimental results in section 4, minimization of triode anode current (calculation) in section 5, faults and remedies in section 6, and discussions & conclusions in section 7.

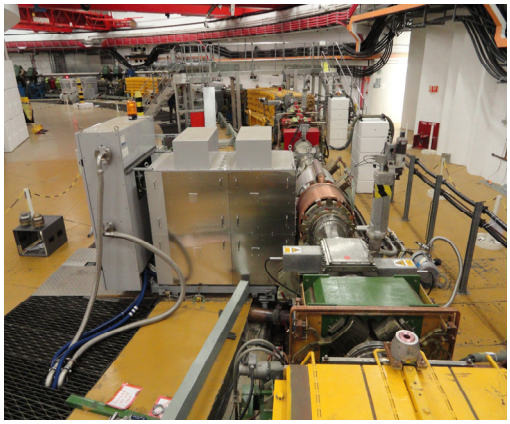


Fig. 1
LOI ready for beam test at the SP6.

2. Investigation of current trip and overshoot of the buck regulator

In the previous experiment, waveform of the buck regulator output current presented an unexpected overshoot at the grid switching. Also, the gap voltage could not reach higher than 1.5kV-peak due to the current trip of the buck regulator. During the investigation of relevant waveforms at the onset of current trip, Andy and Ian found insufficient mating of the LOI HPD with cavity through coaxial connector in January 25, 2011.

As suggested in the report, LOI-9, Nakanishi and Irie examined the impedance around the triode by the network analyser, HP4195A in January 28-30. However, no suspicious resonant peak could be found around 20~30kHz and 130~180kHz.

The reason is not clear, but overshoot and current trip at the lower gap voltage disappeared anyway after sufficient mating of the HPD with the cavity (fig. 2).

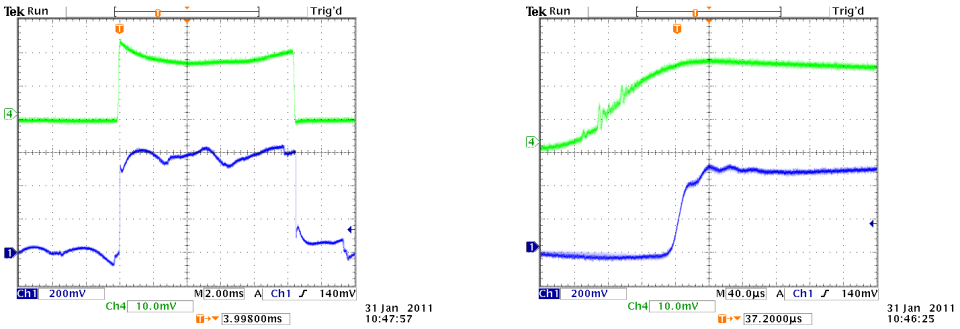


Fig. 2: (left) Tetrode (upper, 10A/10mV) and Triode (lower, 35A/V) anode currents. (right) those in a magnified scale. No overshoot can be seen for the triode current.

3. Experimental setup

§ 3-A Zgk and Zpg

Only the impedance of the newest feedback coil (FBC) at the triode circuit was given in the previous experiment. Zpg as well as Zgk were measured in this experiment (figs. 3-4), where the measurement procedure is given in LOI-6 [1]. Shorted turn number (N2) of the FBC was changed from 6 to 9 in order to move the fundamental resonant frequency to a slightly higher one, i.e. from 1.78MHz to 1.94MHz.

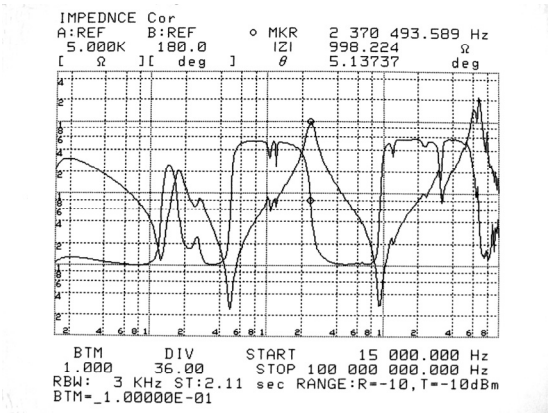


Fig. 3: Zgk.
Fundamental resonance peaks at 2.370MHz with 998ohms.

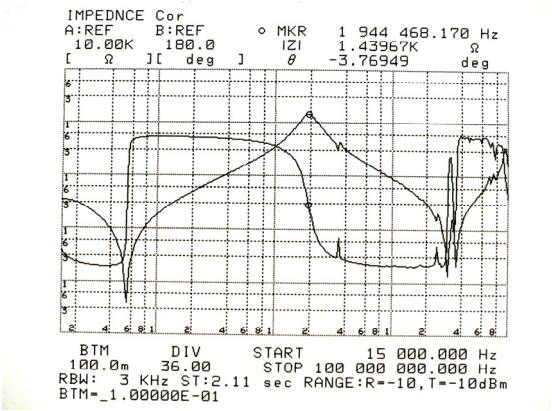


Fig. 4: Zpg.
Fundamental resonance peaks at 1.944MHz with 1.44kohms. FBC with N2=9.

§ 3-B Surge absorber at the grid switcher (fig. 5)

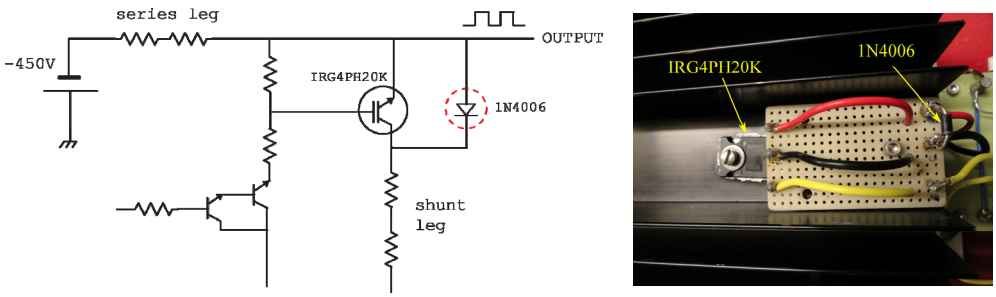


Fig. 5: Surge absorber (1N4006) attached across the IGBT switch (IRG4PH20K).

§ 3-C "LOI Ready" signal to SP6 interlock system

The “LOI Ready” signal was meant for “DC voltage ON” to the buck regulator (BR). However, it is necessary to shut off the solid-state amplifier in the driver stage (AR amplifier) when the BR trip occurred. Such trip status is incorporated into the “LOI Ready” signal in series with the “DC voltage ON” status as shown in fig. 6.

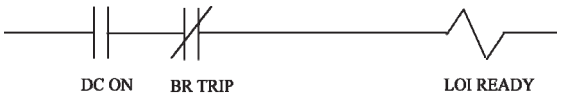


Fig. 6: New “LOI Ready” sequence.

§ 3-D Change of valve quiescent values

Grid switching was intended so far for complete cut-off of the anode currents during the non-accelerating cycle. However, since the CAV TUNE module requires some voltages of gap and grid for phase comparison during non-accelerating cycle, grid bias voltages have been changed to allow some currents in the anodes. Also, in order to avoid rapid decrease in gap voltage at the end of accelerating cycle, the switching period for conduction is extended from 10.5msec to 11.5msec. The new parameters are shown in the Table.

§ 3-E Ancillaries

Following the suggestions from the ISIS radiation control supervisor, thickness of the LOI HPD side panel was increased from 3mm to 6mm. This was done by overlapping another 3mm-thick aluminium panel upon the present 3mm-thick panel (fig. 1).

In order to secure firm mating between the LOI HPD and cavity, a metal fitting was attached at the girder (fig. 7).

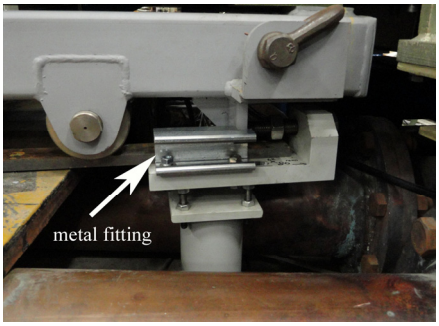
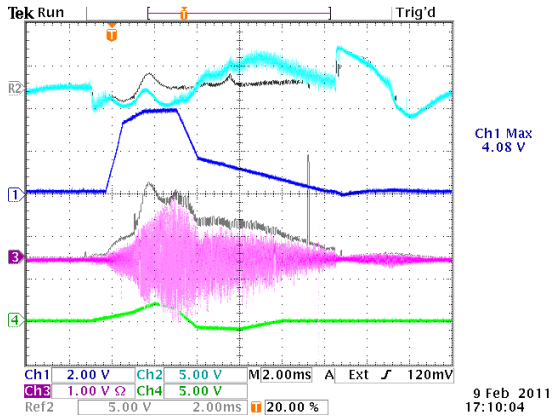


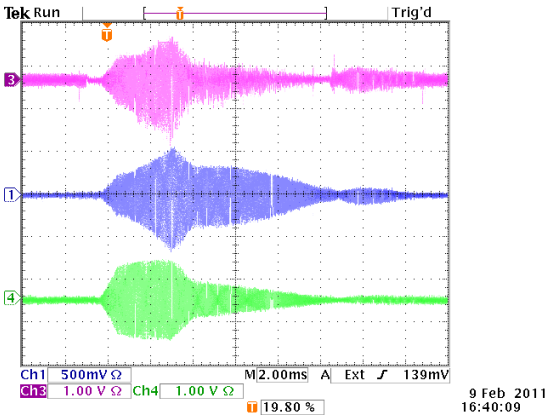
Fig. 7:
Metal fitting at the girder of the LOI mounting base.

4. Experimental results

Fig. 8 show the experimental results with the cavity tuning loop, where the gap and grid voltages are compared. The oscillations were stable, and 5KV-peak was obtained at the cavity gap around 2msec. In the figure, the AVC demand for gap voltage was decreased after 3msec. If the demand has a shape of longer flat top like the present 2RF system, the gap input current will exceed 50Amp-peak in the later acceleration cycle, and it will trip the buck regulator. Fine tuning of the ferrite bias current was tried in order to decrease the gap input current. However, it was not successful. If the present biasing is correct on tune, the cavity impedance looks like 70ohms at 10msec (Feb. 5, 2011), which is inconsistent with that obtained in ref. 2, i.e. 330ohm at 6.2MHz (?)



Ch1: Gapvolts envelope (× 1.2k)
Ch2: Cavity tune phase detector output (1V/10deg)
Ch3: Cavity input current RF (0.1V/2Amp)
Ch4: Phase demand "loi_biaspd_2"
(black line in ch's 2 and 3: taken with no phase demand at gapvolts 2.95Vmax)



Ch1: Triode input current (0.1V/2Amp)
Ch3: Gridvolts (arb.)
Ch4: Gapvolts RF (arb.)

Fig. 8: Experimental results.

5. Minimization of triode anode current (calculation)

From view point of the triode power efficiency, it is necessary to take into account both the final anode choke and feedback impedance as the triode load. The simulation code, TopSpice, was used to calculate the triode anode current (fig. 9). The RF frequency was then searched which gives a minimum triode anode current with a given cavity inductance. The results are shown in figs. 10-11. It is seen in fig. 10 that lower cavity inductance is required to give a minimum triode current than that for a cavity resonant condition, because the final anode choke and feedback impedance (Zpg) behaves as a capacitance above 2.8MHz.

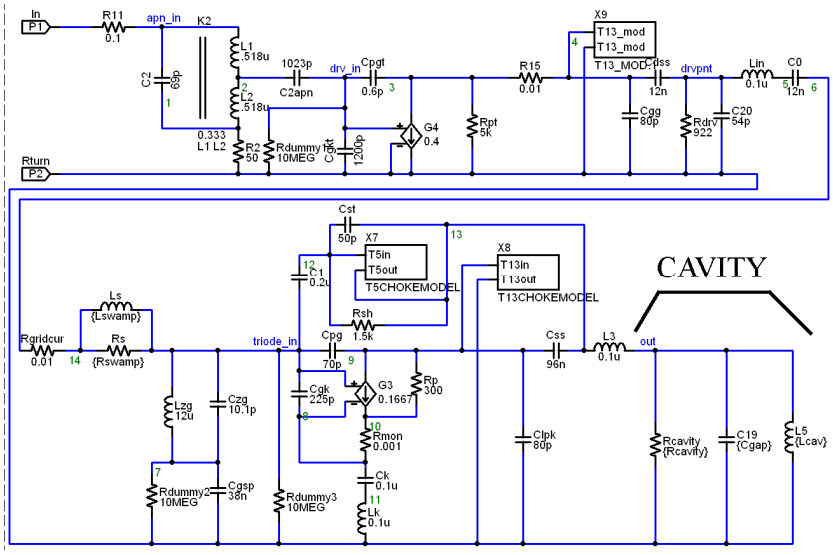


Fig. 9:
LOI model for Spice simulation. Triode anode current flows through "Rmon", Cgap=1,760pF and Rcavity=538ohm.

Fig. 11 shows the phase difference to achieve minimum current between gap and grid voltages, and between gap voltage and grid input current. Since the grid voltage is highly deformed above 5MHz [3], the grid current should be used for phase comparison in the bias tuning loop.

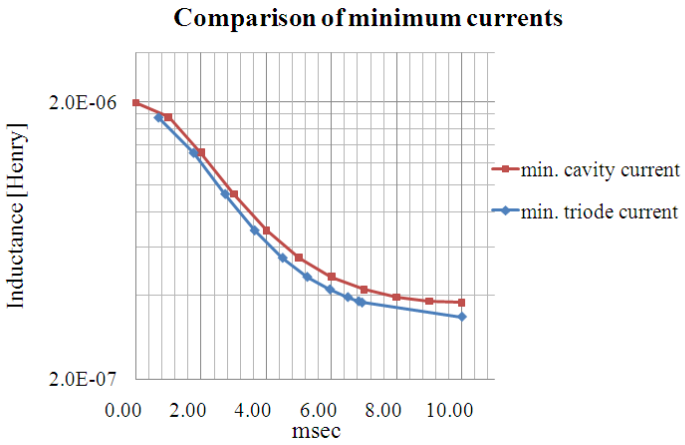


Fig.10:
Comparison of cavity inductance to give minimum cavity current and triode anode current.

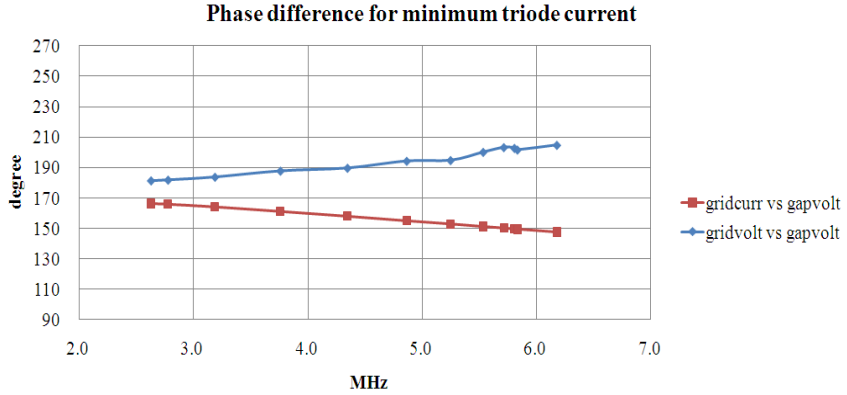


Fig. 11:
Comparison of phase difference to give minimum triode anode current.

6. Faults and remedies

(1) Grid switcher

Two high power resistors (R3 and R4, 50ohm each) in the series leg and another two (R7 and R9) in the shunt leg were damaged. The reason is not clear. But, one possible reason is that we have run the grid switcher for a long time with only one fan at the bottom instead of two due to fan damage. These resistors were replaced with spares. However, the new ones were also damaged when mistuning of the bias current and the flow interlock on 4648 valve occurred almost simultaneously. Because there was no spare resistor available, new high power resistors were ordered and fixed to the cooling plate (fig. 12). In the meantime, a surge absorber was attached across the IGBT switch (see section 3-B).

(2) Grid input resistor

Grid input resistor was installed in January 2011 in order to stabilize the system, when the reason of buck regulator current trip was being investigated. The resistor comprises six 12ohm-3W resistors in parallel. However, the resistor was not effective in preventing the trip. After the LOI test with higher duty operation (see section 3-D), these resistors as well as the copper lead and Pearson CT were burnt (fig. 13). The grid input circuitry was then repaired without the grid input resistor.

(3) DC supply for SP6 bias regulator

Fan fuse of the DC power supply for the SP6 bias regulator was burnt. The reason is thought to be overheating due to incorrect embedding of fuse into the fuse holder rather than over-current in the fan. As seen in fig. 14, the fuse is sitting on the bottom of fuse holder, and the other side of the metal cap barely touching the fuse holder socket.

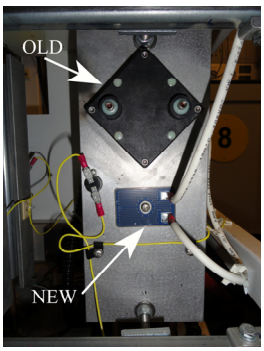


Fig. 12:
New high power resistor in the shunt leg of the grid switcher.

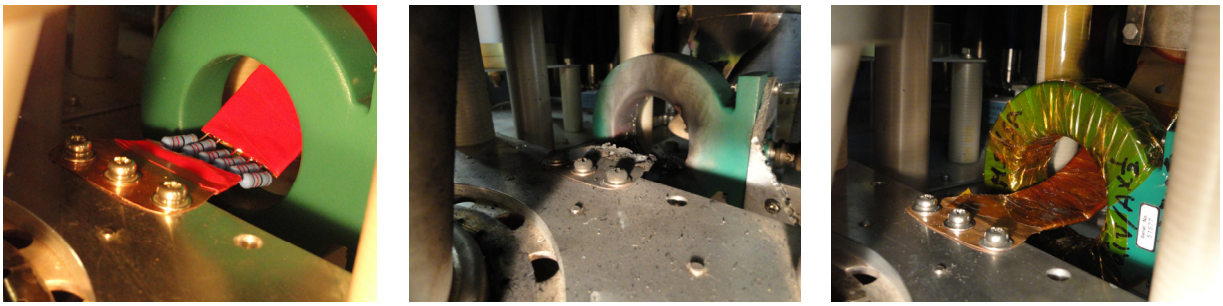


Fig. 13: Grid input resistor before burning (left) and after (middle). Grid input circuitry was repaired without grid input resistor and using a used current transformer, Pearson model 110 (right).

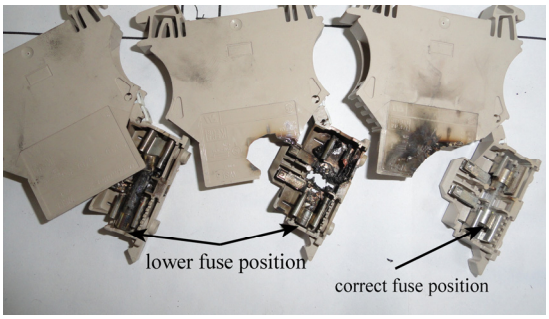


Fig. 14:
Burnt fuse holder. Two fuses from left are put in the incorrect position. Metal cap is sitting on the bottom of fuse holder, and the other side barely touching the fuse holder socket.

7. Discussions and conclusions

Currently, water to LOI is fed from the SP5 and SP6. When more than three of the 2RF systems are to be operated in the future, it is highly required to reinforce the cooling water system so that R&D or tuning of the LOI can be performed independently.

Following subjects are also to be studied before the beam test, such as improvement of the waveform distortions, fine cavity-tuning for minimum triode current and phase-locked operation with fundamental cavity. As for the waveform distortion at grid voltage, it is essential to remove the sub-harmonic component in the RF law signal [3].

References:

[1] LOI Progress Report LOI-6, http://www-accps.kek.jp/Low-Impedance_Cavity/LOI-6.pdf
[2] LOI Progress Report LOI-2,
http://www-accps.kek.jp/Low-Impedance_Cavity/LOI02.August.05.pdf
[3] LOI Progress Report LOI-8, http://www-accps.kek.jp/Low-Impedance_Cavity/LOI-8.pdf

TABLE LOI Parameter Log

Parameter	Description	10/29/2009	4/1/2010	11/20/2010	1/31/2011	2/8/2011				
Driver Heater Current				1,655.0	1,650.0					
Final Heater Current				542.0	541.0					
Driver G1										
High [V]				-88 ~ -106	-82.0					
Low [V]				-276.0	-167.0					
Duty [%]			≳ 52.5		≳ 57.5					
Driver G2										
Volt [kV]				1.4	1.3					
Current [A]				2.48 ~ 2.50	2.7 ~ 2.9					
Driver Anode										
Volt [kV]				6.8	6.6 ~ 6.7					
Current Peak [A]										
Current Ave. [A]				10.5	13.5 ~ 15					
Duty [%]										
Final G (Grid Switcher)										
DC [V]				-500.0	-450.0					
DC Current [A]				0.89	0.86 ~ 0.89					
Shunt Leg (R11) Dial				58.0	58.0	10 (196ohm)				
Series Leg (R5) Dial				48.5	48.5	48 (124ohm)				
Duty [%]			52.5		57.5					
Final Anode										
DC [V]				32.0	32.0					
Anode Volt [kV]				15.0	14.5					
Current Peak [A]										
Current Ave. [A]				10.0	12.5†					
Duty [%]										
Trip Level	6: 30Amps-pk	6 ---> 7								

Grid level changed
Switching period changed
†) absolute maximum is 16Amps.