December 23, 2004

LOI progress summary

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by the ISIS/ANL/KEK

Our original work plan at the MICE Hall, which was discussed at the 9th meeting held at Argonne National Laboratory in July 2004, was modified by the delay of the insulating oil: oil shock! However, thanks to the great efforts by everyone involved, we could almost recover the time. Although the preparations of LOI in the MICE Hall, which we call 'Phase I', has new aspects, such as grid switching, higher voltage and current, compared to those at KEK, we could achieve 10.0 KV-peak per cavity gap with fixed frequency at 2.2MHz on December 22, 2004 (Figs.1, 2). Because of limitation for the cooling water available, the duty factor of operation was 25%. The parameters used are listed in Table I.

After the preparations mentioned below, we need to further test the LOI to generate 10.0 KV-peak per cavity gap in a bias swept mode using the Low-Power RF (LPRF) from the MCR. It will take 4-6 months for preparations.

Further works:

(1) ac fuses
- 400V (3p) ac input current to the tetrode is beating +-40%. reconsider the fuse capacity,
- triode step-start is provided with 700Amp fuse: the upstream fuse is 500Amps. reconsider the discrimination law.

(2) Bias regulator
- fix water leaks from the current shunts,
- cable for current control and monitoring.

(3) Fast plate-current monitor for tetrode
- install Tektronix DCCT in the plate supply chassis

(4) Chiller supply to grid switcher and buck regulator
- 3.8 l/min for grid switcher, and 19-38 l/min for buck regulator

(5) Increase the cooling power to the liquid resistor shunt
- when generating 9KV-peak across 500ohms shunt initially, the temperature rapidly increased to more than 65 degree C, and the resistance decreased to 250ohms. The power dissipation is then 40KW.

(6) Prepare the Low-Power RF (LPRF) control signal from the MCR

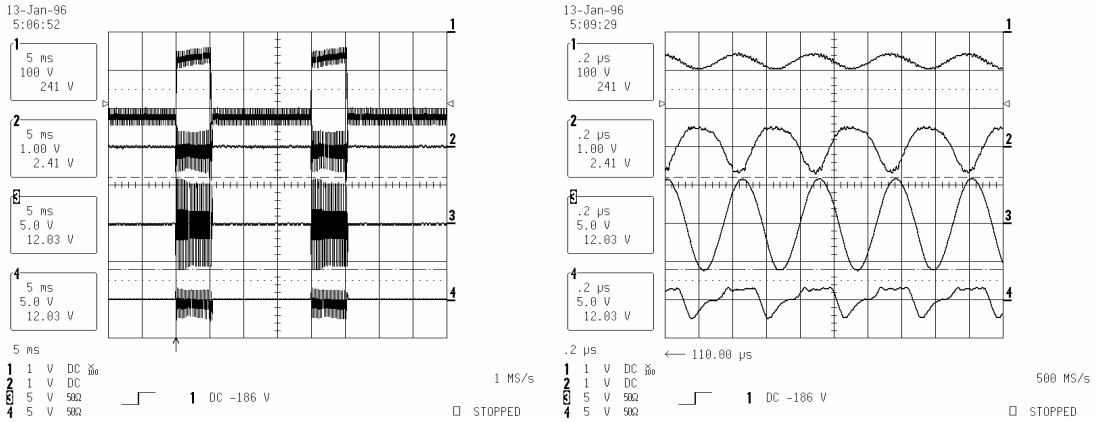
Discussions on the installation into the Synchrotron are required regarding,

(1) civil engineering in the synchrotron hall: a hole-drilling through the shield wall for cables and water supply for LOI,

(2) budget, and

(3) physics by one LOI system out of the four 2nd harmonic systems.

Figure 1. Achievement of 10KV-peak per cavity gap at fixed frequency 2.2MHz.
(date in the scope should be read as 22-Dec-2004!)



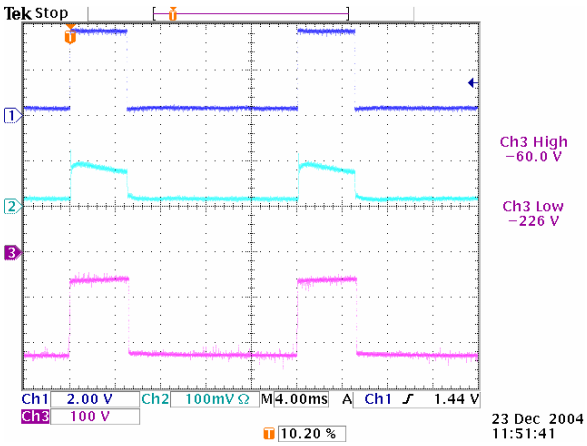
Ch.1 G1 voltage to tetrode

Ch.2 grid input to triode (x 1/1000)

Ch.3 cavity gap voltage (x 1/1,660): 12.03Vp-p corresponds to 10KV-peak at the cavity gap

Ch.4 cavity input current (10Amps/0.5V)

Figure 2. Grid switching signals



Ch. 1 TTL trigger to triode grid switcher

Ch. 2 Buck regulator output current (uncal.)

Ch. 3 Tetrode grid input voltage

Table 1. Parameters of LOI as of December 22, 2004

Driver stage	
plate voltage	6KV
plate current	5~6Amps (20~24Amps-peak)
G1 voltage	-68V(high), -236V(low): 25% duty
G2 voltage	1.2KV
G2 current	0.5Amps
Final stage	
plate voltage	16KV
plate current	6Amps (24Amps-peak)
G voltage	-340V(high), -500V(low): 25% duty