SOI Pixel Developments in a 0.15 μm Technology

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KEK Detector Technology Project : [SOIPIX Group, http://rd.kek.jp/project/soi/]

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#

OUTLINE

- **Introduction**
- **Features of SOI Pixel Detector**
- **SOI Pixel MPW run**
- **Test Results**
- **Summary**

N20-3 : TCAD Simulation for SOI Pixel Detector
N20-5 : A SOI Implementation of a 5th generation CAP
N44-6 : TID for 0.15um FD-SOI CMOS Tr

Introduction : KEK SOIPIX R&D History

'05. 7: Start Collaboration with OKI Elec. Co. Ltd. for SOI Pixel detector R&D .

'05.10: FY05 TEG submission in OKI MPW (Multi Project Wafer) run with *0.15μm* technology.

'06. 3: Fabrication was finished.

FY05 TEG chips are successfully tested.
Response to Light and β-ray is confirmed.

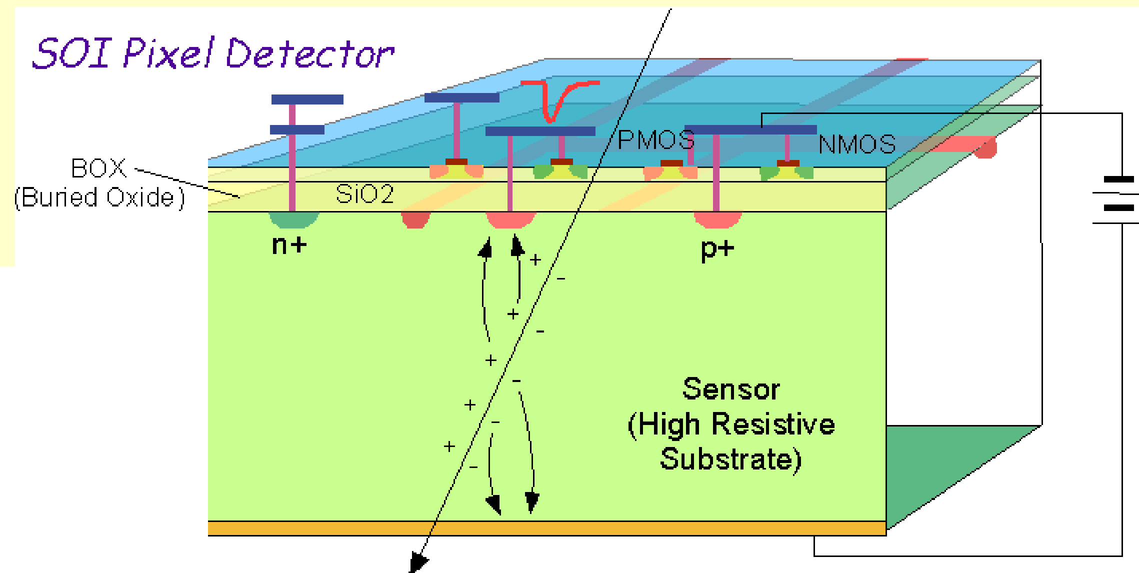
'06.12: First MPW run hosted by KEK with 17 designs which includes submissions from US lab/univ.

'07. 4 : Fabrication was finished.

'08.1: Second KEK MPW run is scheduled.

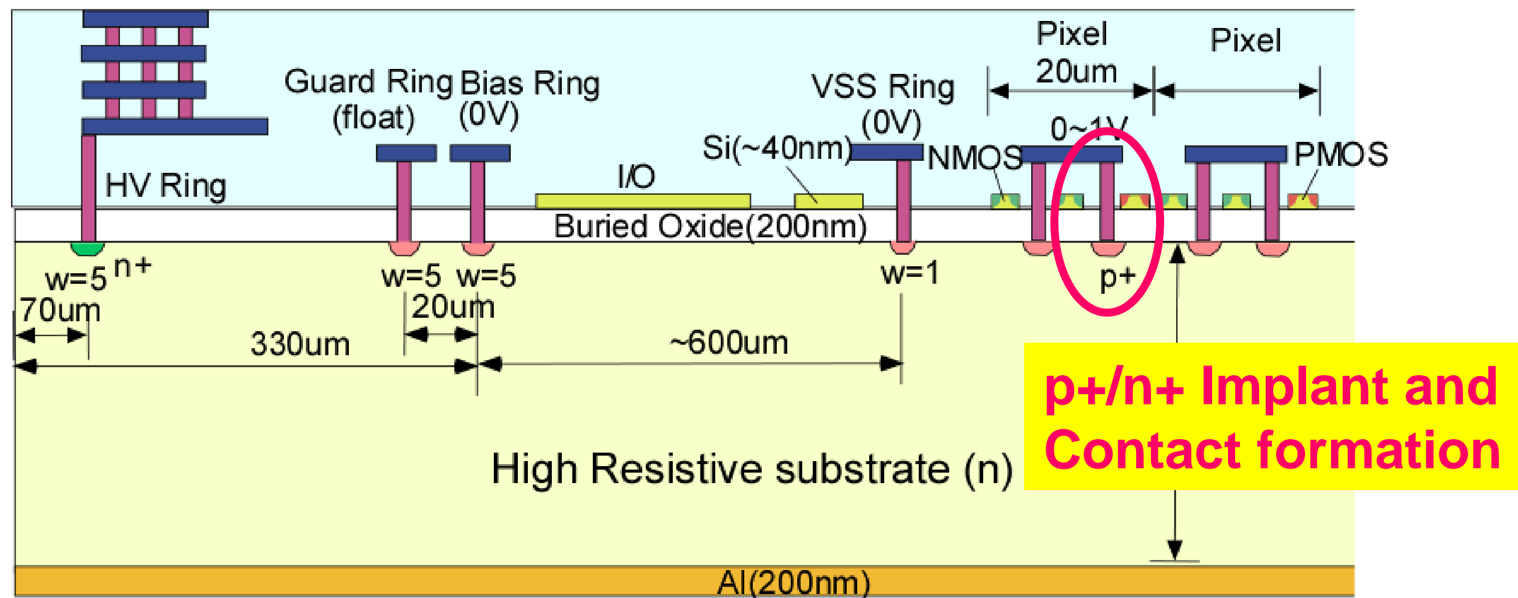
Features of SOI Monolithic Pixel detector

- Bonded Wafer (High Resistive Substrate + Low Resistive Top Si).
- Standard CMOS Electronics (NMOS, PMOS, MIM Cap etc.).
- Monolithic Detector, No Bump Bonds (Lower cost, Thin Device).
- High density (Smaller Pixel Size is possible).
- Small capacitance of the sense node (~10fF, High gain V=Q/C)
- Industrial standard technology (Cost benefit and Scalability)
- No Latch Up
- Low Power
- ...

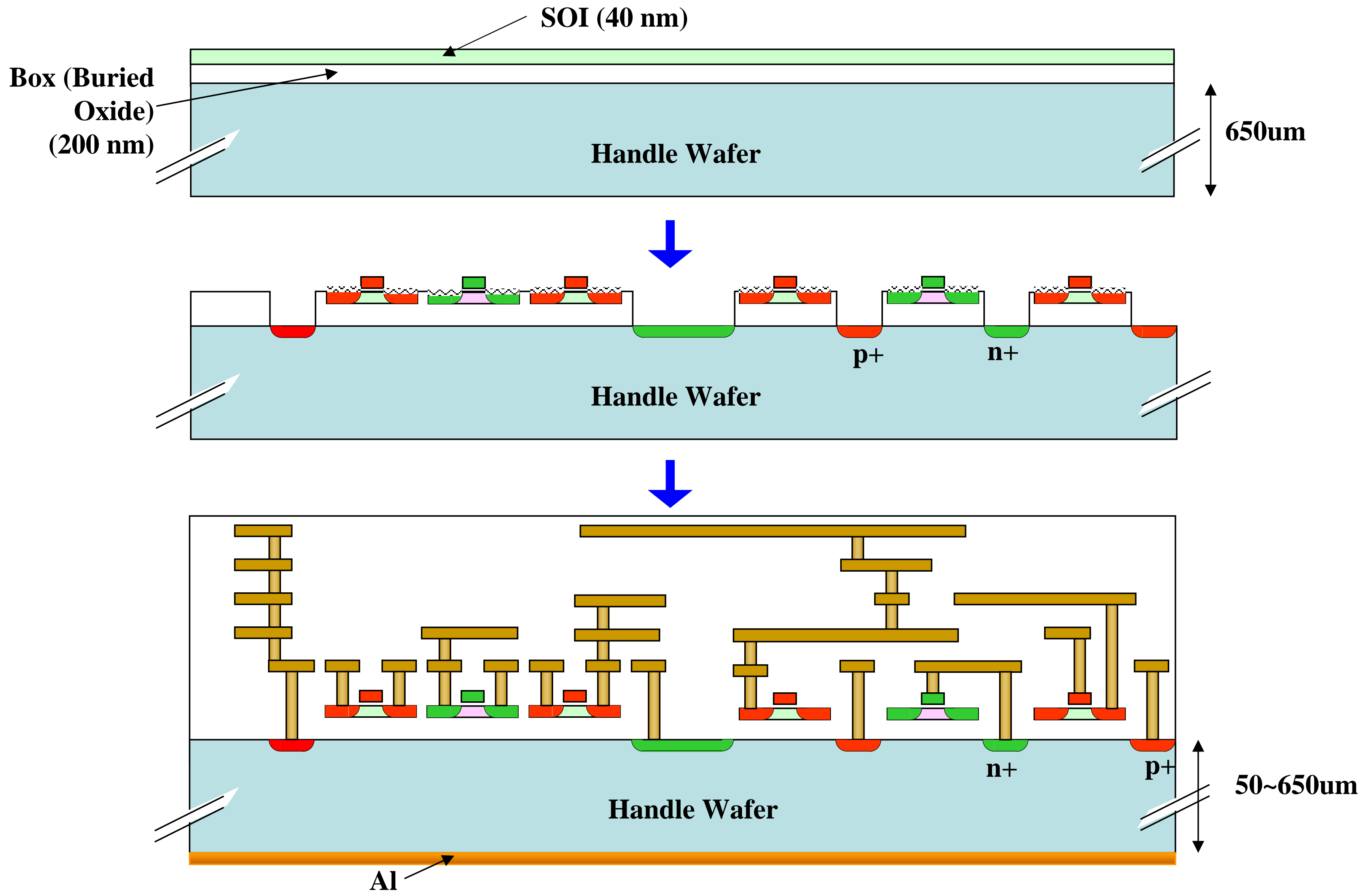


0.15 μm SOI Pixel Process

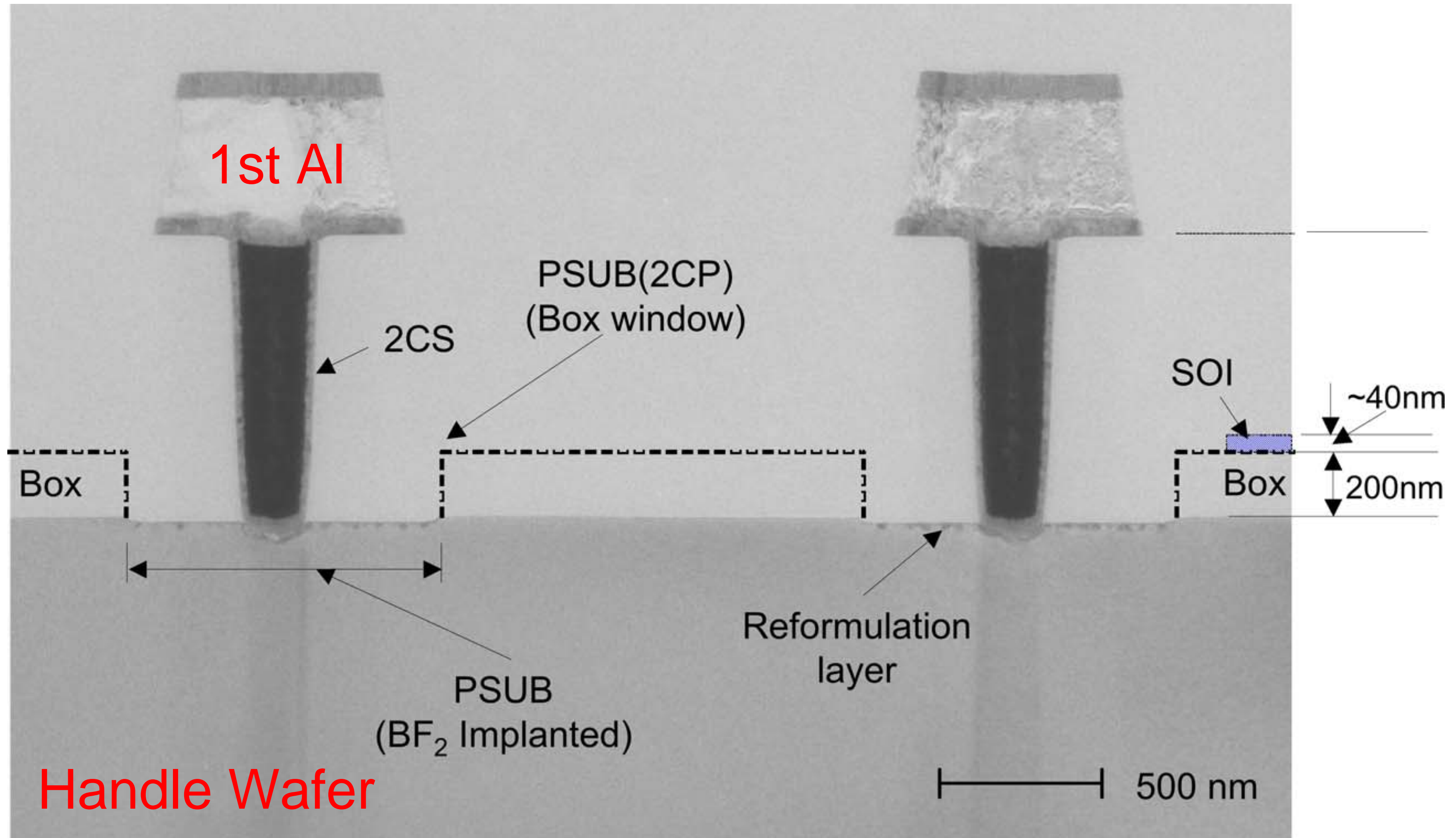
Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type)*, 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).



SOI Pixel Process Flow



Metal contact & p+ implant



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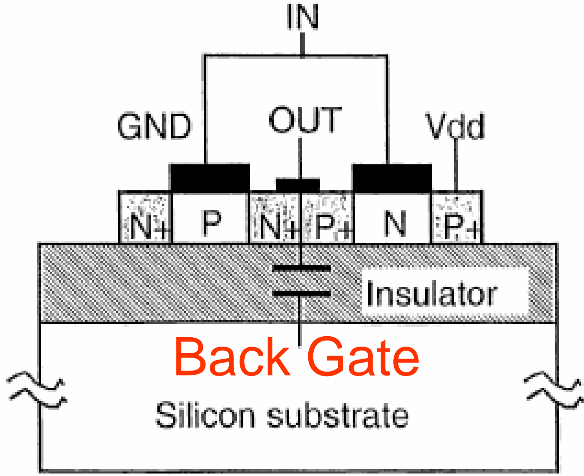
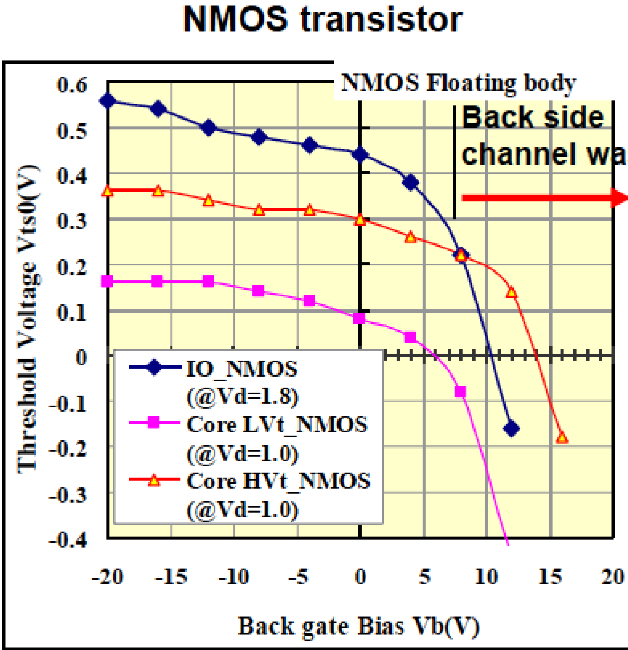
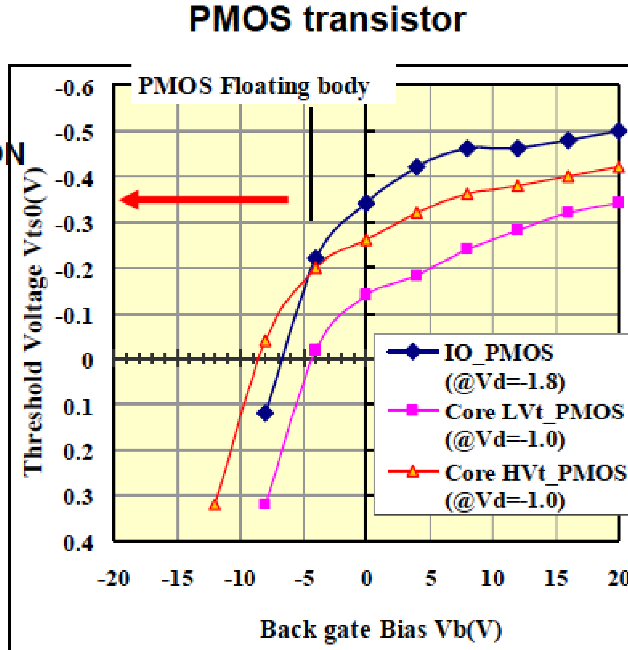
Back Gate Effect

Substrate Voltage act as Back Gate,
and change transistor threshold.



Threshold Variation





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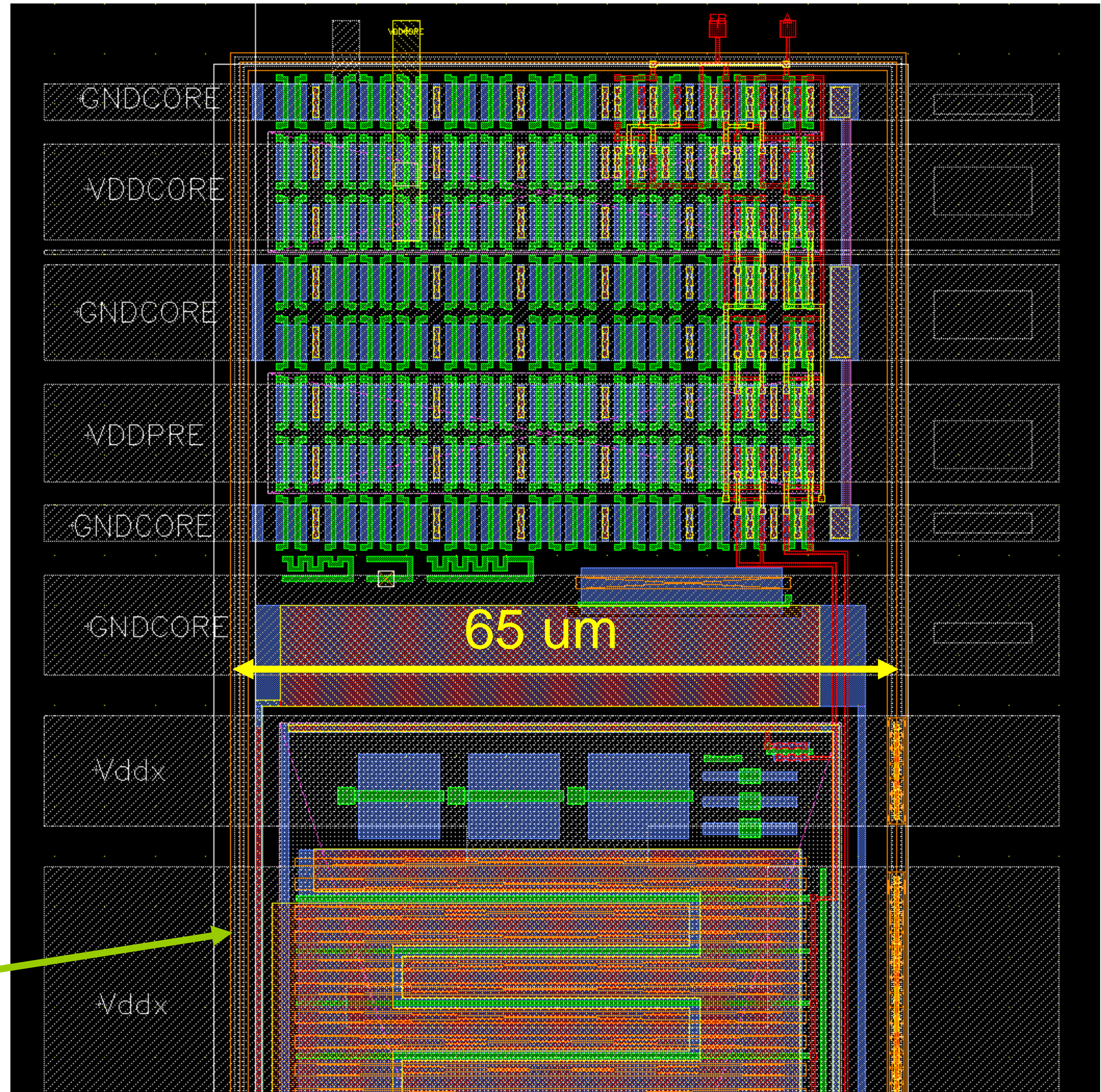
p+ Guard for I/O Buffer

It is hard to re-design I/O buffers, so we just surround the buffer with p+ ring.



p+ ring

with p+ ring = 0V

10MHz Clock

without p+ ring

Signal Input

Signal Output

15V

15.5V

16V

0V

M 100ns Ch3 ∫ 660mV

Ch3 500mV

Ref4 500mV 100ns

Vdet=10V

Out

In

40V

FY06 KEK MPW Run

17 designs were submitted on Dec. 5, 2006

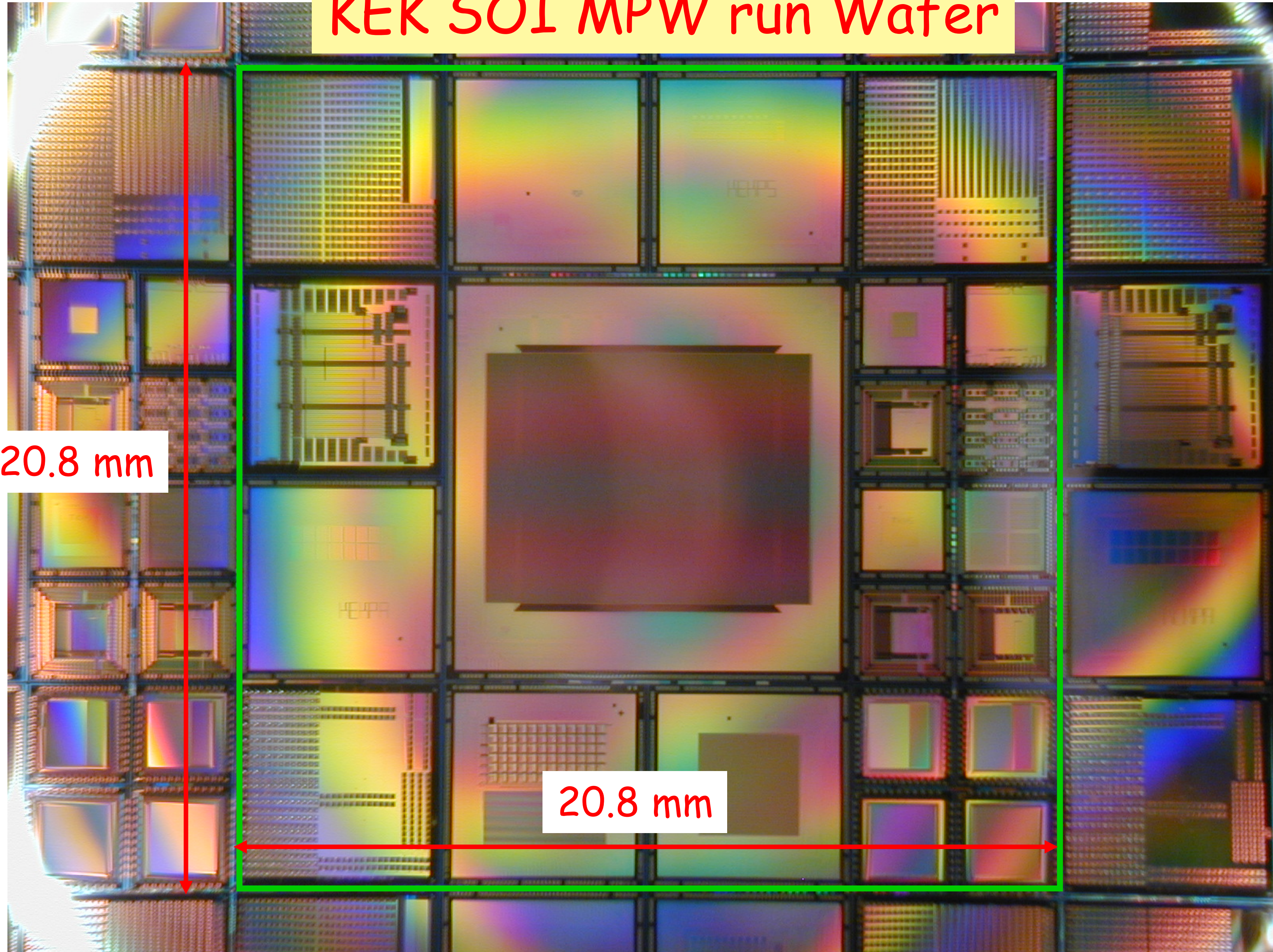
$2.4 \times 2.4\ mm^2$ --- 10 chips
$5.0 \times 5.0\ mm^2$ --- 6 chips
$10.2 \times 10.2 mm^2$ --- 1 chip

Top Cell Name	Chip size	Affiliation
VARPIXEL	2.4 mm	Osaka Univ.
TOPPIXN	2.4 mm	KEK
OKI0612	2.4 mm	Tokyo Univ.
Achip	2.4 mm	LBL
OKI_TOP	2.4 mm	FNAL(BNL)
ATEG	2.4 mm	JAXA/ISAS
BTEG	2.4 mm	JAXA/ISAS
CTEG	2.4 mm	JAXA/ISAS
isas_set0612	2.4 mm	JAXA/ISAS
RADFET1	2.4 mm	KEK
HawaiiNSUBSTRATE	5.0 mm	U. of Hawaii
detectorPOLY	5.0 mm	KEK
TOP_PIXELSTRIP	5.0 mm	KEK
TOP_8PREAMP	5.0 mm	KEK
TOPTEG2	5.0 mm	KEK
TOPINTPIX	5.0 mm	KEK
TOPCOUNT	10.2 mm	KEK

N20-4 ←------ (HawaiiNSUBSTRATE)

N44-6 ←------ (TOPTEG2)

KEK SOI MPW run Wafer



KEK : I-V characterisitic of the detector

2.5 x 2.5 mm^2 chip

FY05

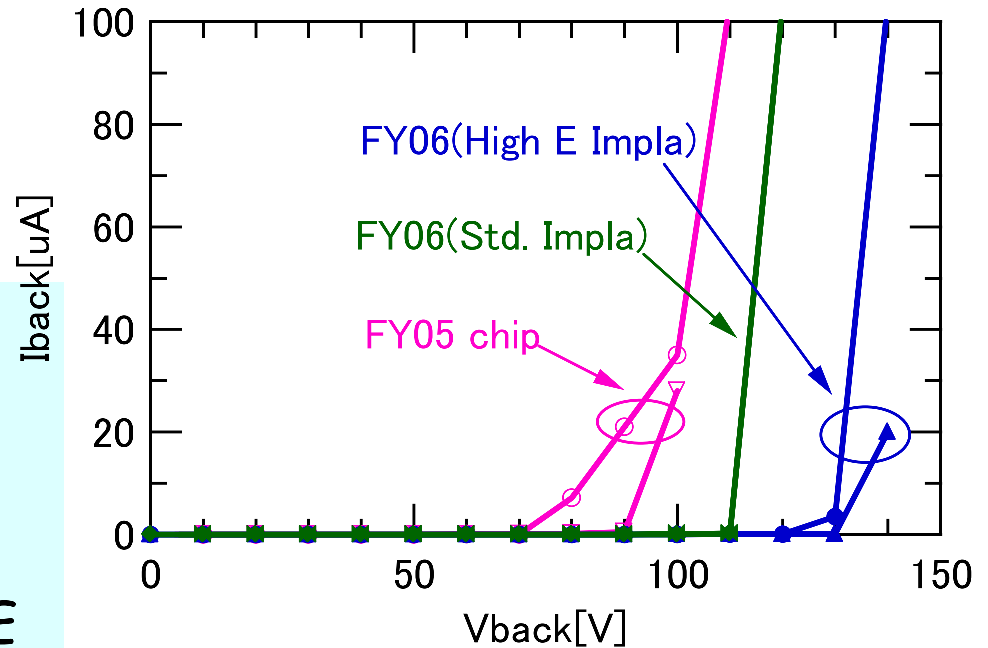
↓ Round the corner of bias ring.

FY06(Std.)

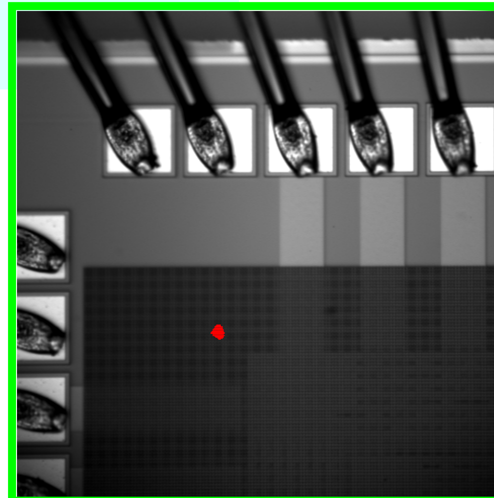
↓ p+/n+ implant with higher E (~x4.7 deep).

FY06(HE)

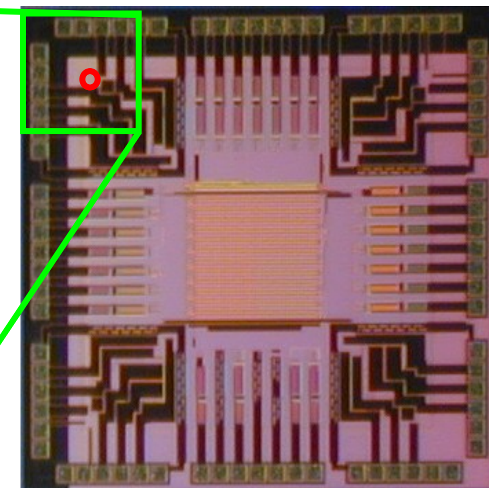
become better, and reached to ~130V.



Micro Discharges are observed with infrared camera



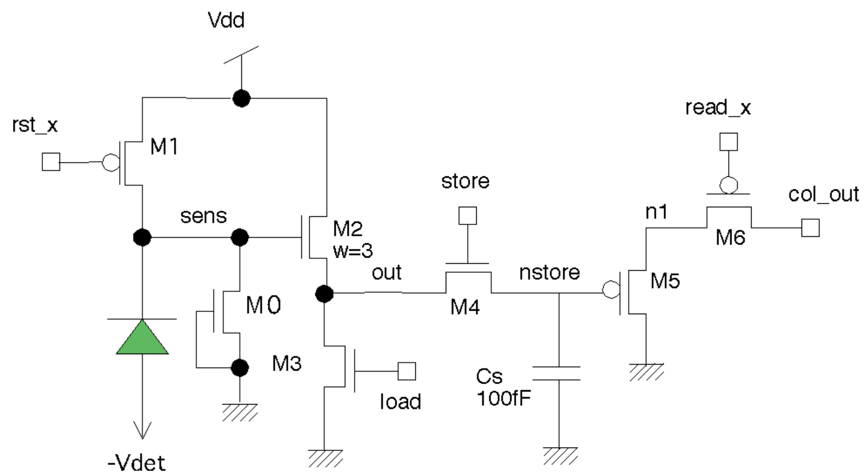
I = 40 μA, T = 1 min

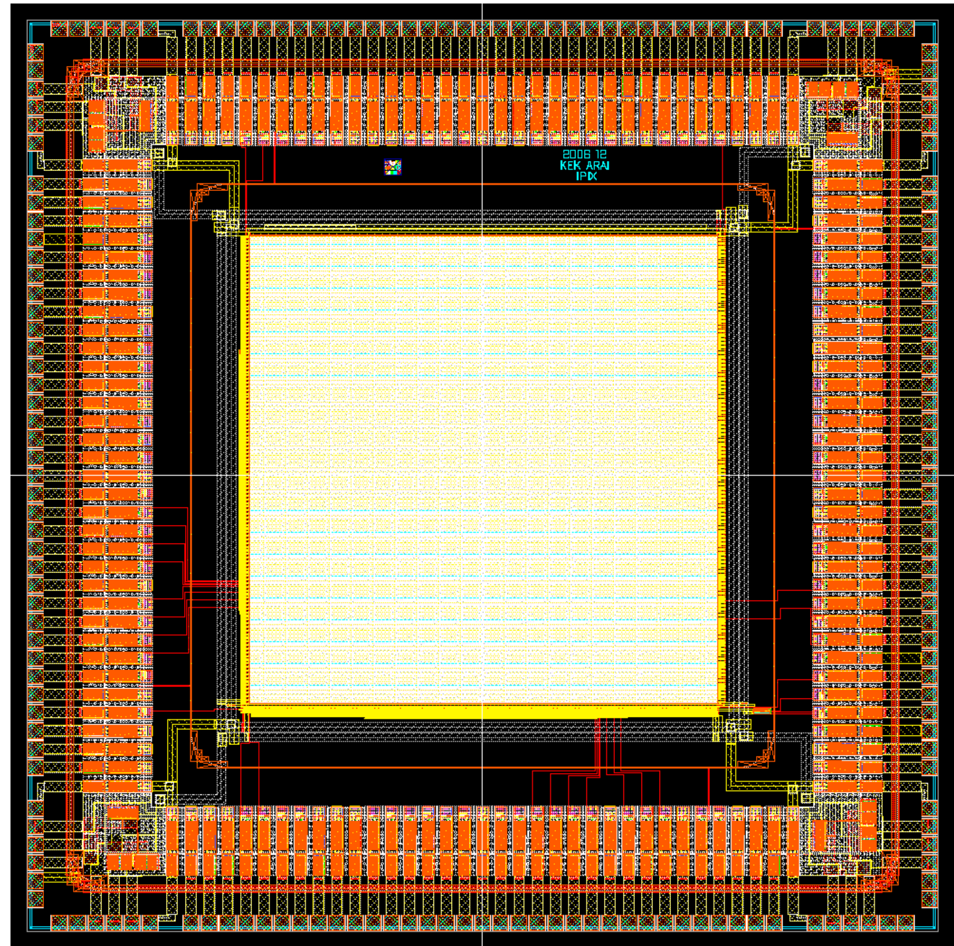


Corner of the bias ring

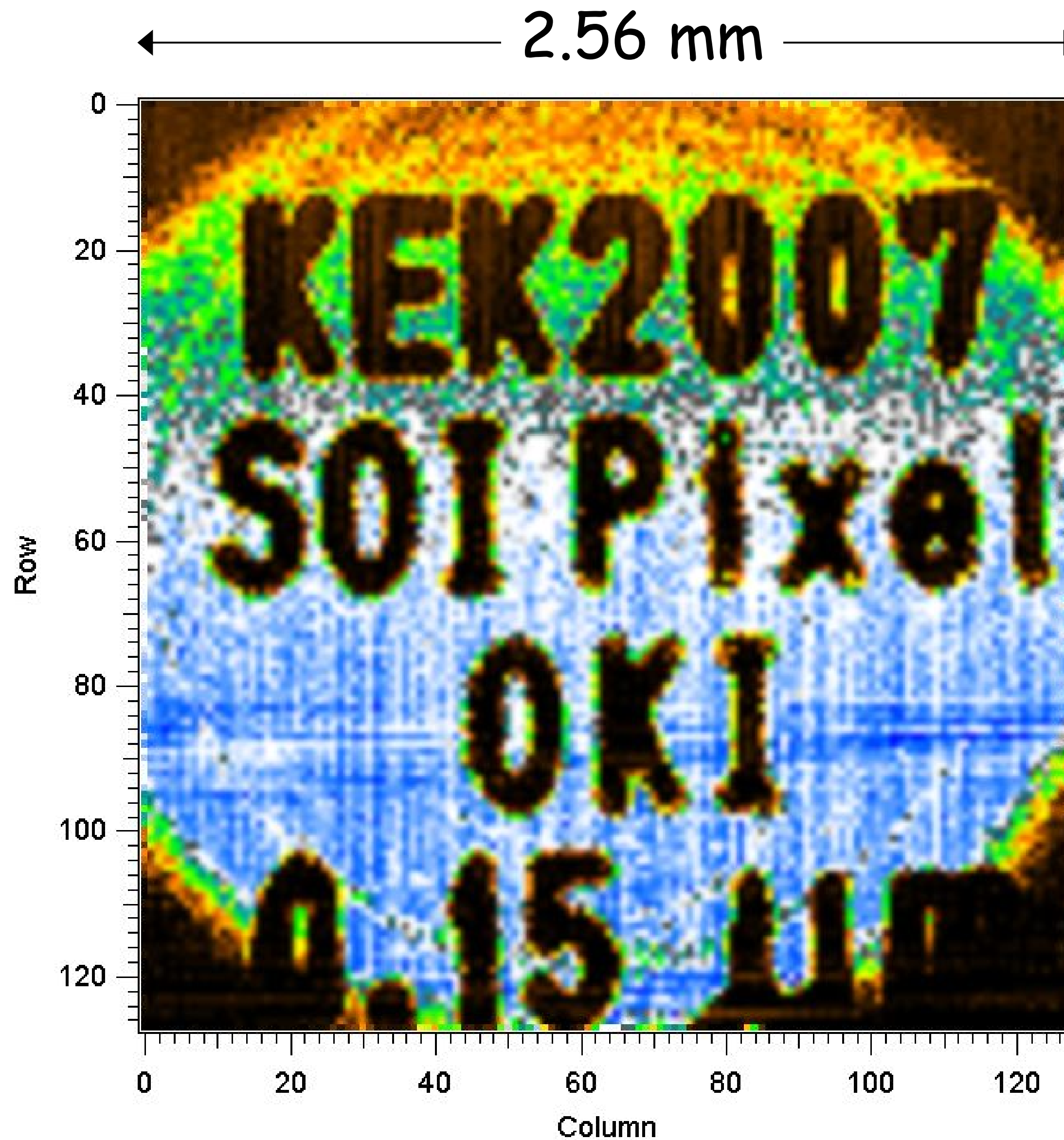
KEK : Integration Type Pixel (INTPIX)

- 20 μm x 20 μm pixel (Standard APS type pixel)
- 128 x 128 pixels
- 5x 5 mm^2 chip





INTPIX : Laser Image



Plastic Mask for PCB is infront of the pixel.

Red Laser Illumination

λ=670 nm, ϕ~3mm

FY07 Submission Plan

- Next submission is scheduled on Jan 5th 2008.
- Due to OKI process movement, we will use 0.2 μm process at the next run.

	0.15 μm	0.2 μm
Wafer Diameter	6 inches	8 inches
Core (I/O) Voltage	1.0V (1.8V)	1.8V (1.8/3.3V)
Gate Length	0.14 μm	0.2 μm
Gate Oxide Thickness	2.5/5 nm	4.5/7 nm
BOX Thickness	200 nm	200 nm
Ioff	<100 pA/μm	<0.1 pA/μm

Summary

- SOI pixel device has many interesting features to use in HEP and Space applications.
- We successfully confirmed the basic operations of SOI pixel detector with OKI 0.15 μm FD-SOI technology.
- We hosted the SOI pixel MPW run last year, and submitted 17 designs including US and Japan Univ./Labs.
- We are planning the next MPW run in Jan. 2008 with 0.2 μm technology
- We are opening this unique process to everyone who interested in the SOI pixel.