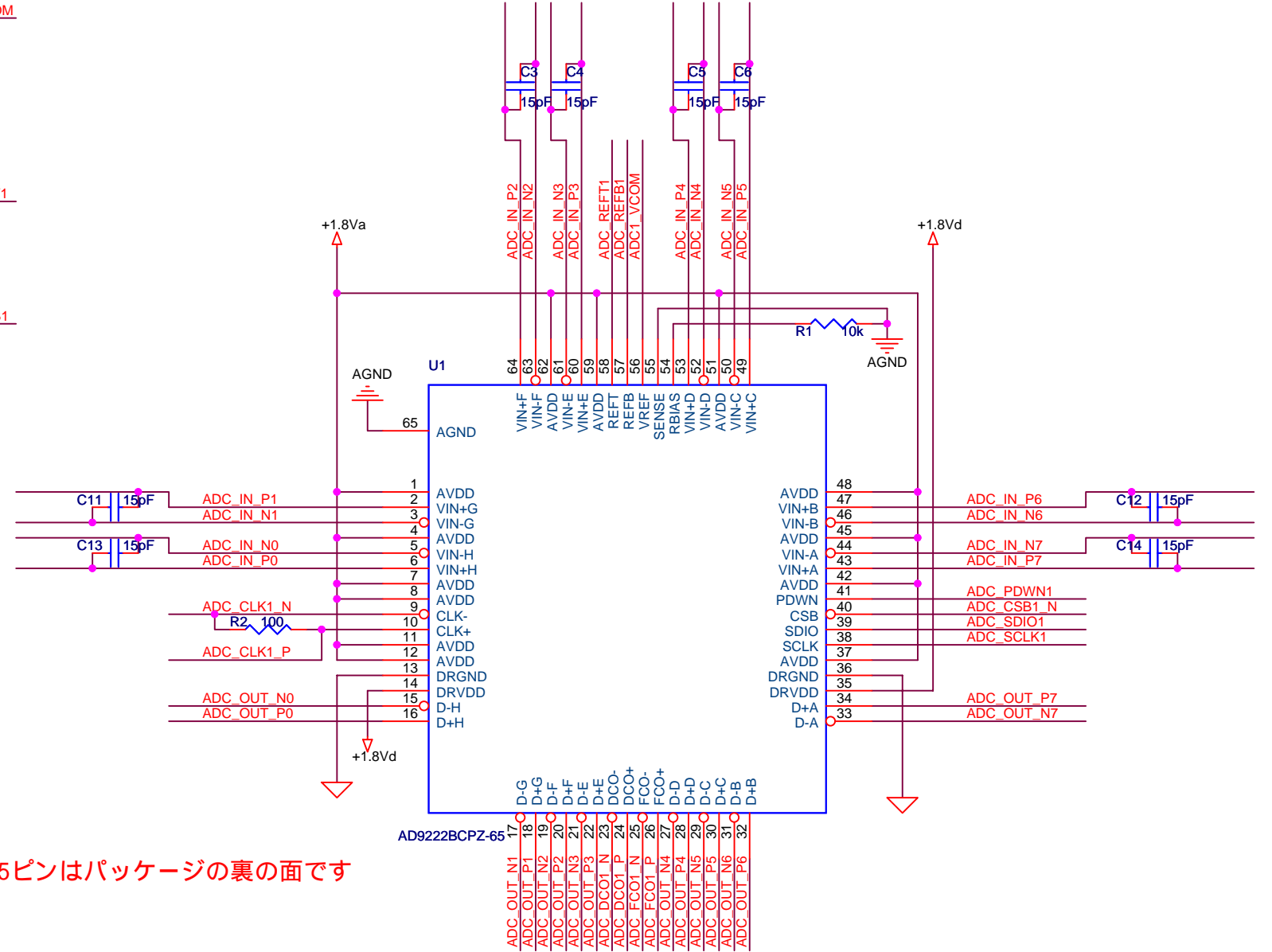
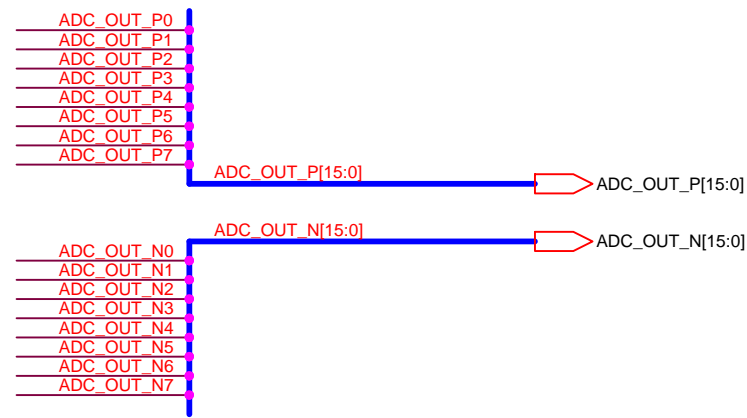
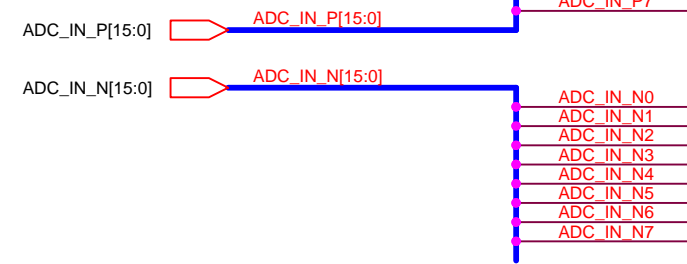
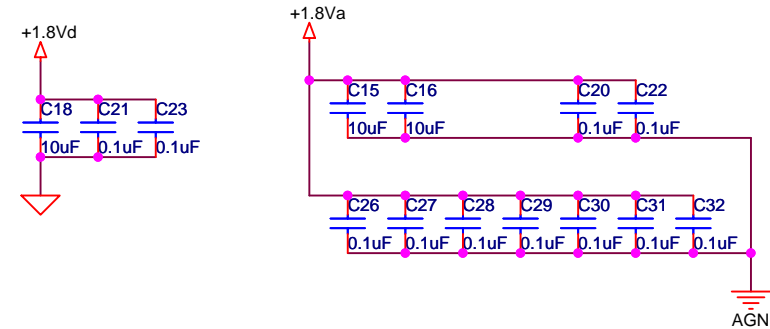


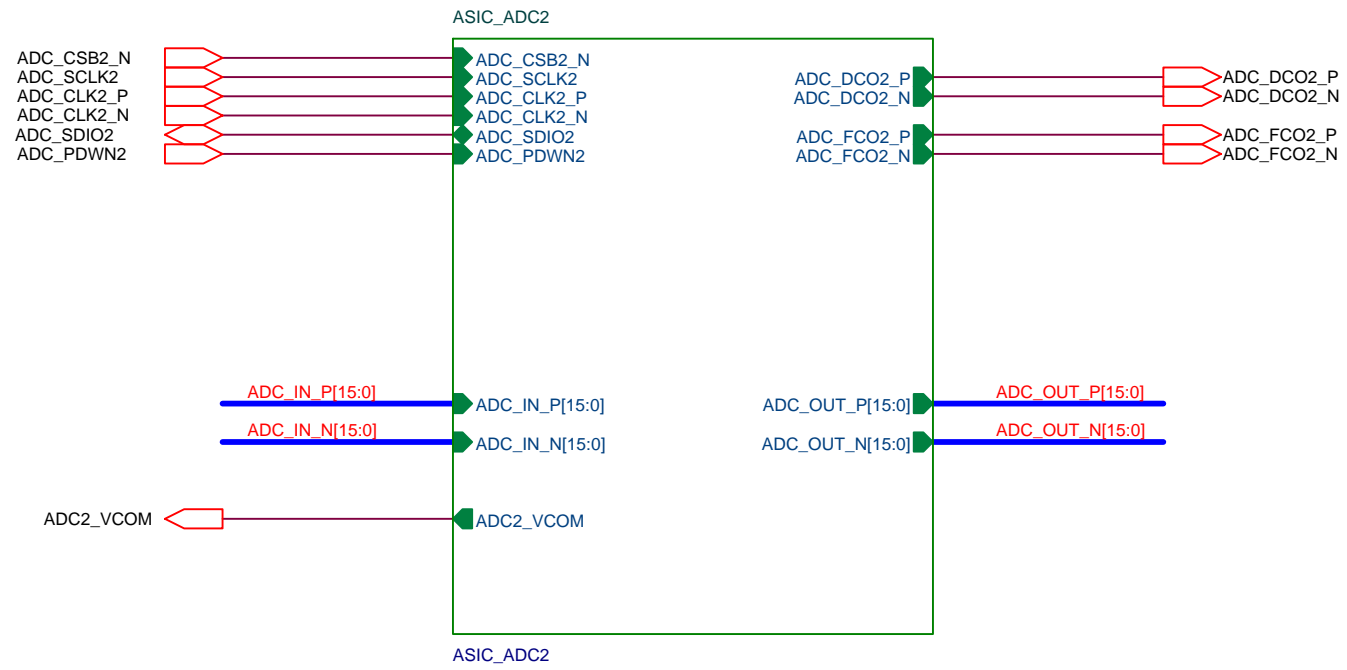
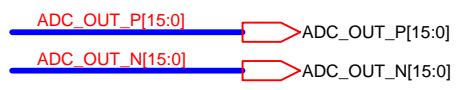
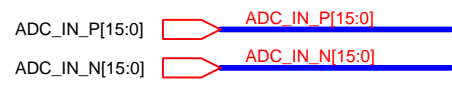
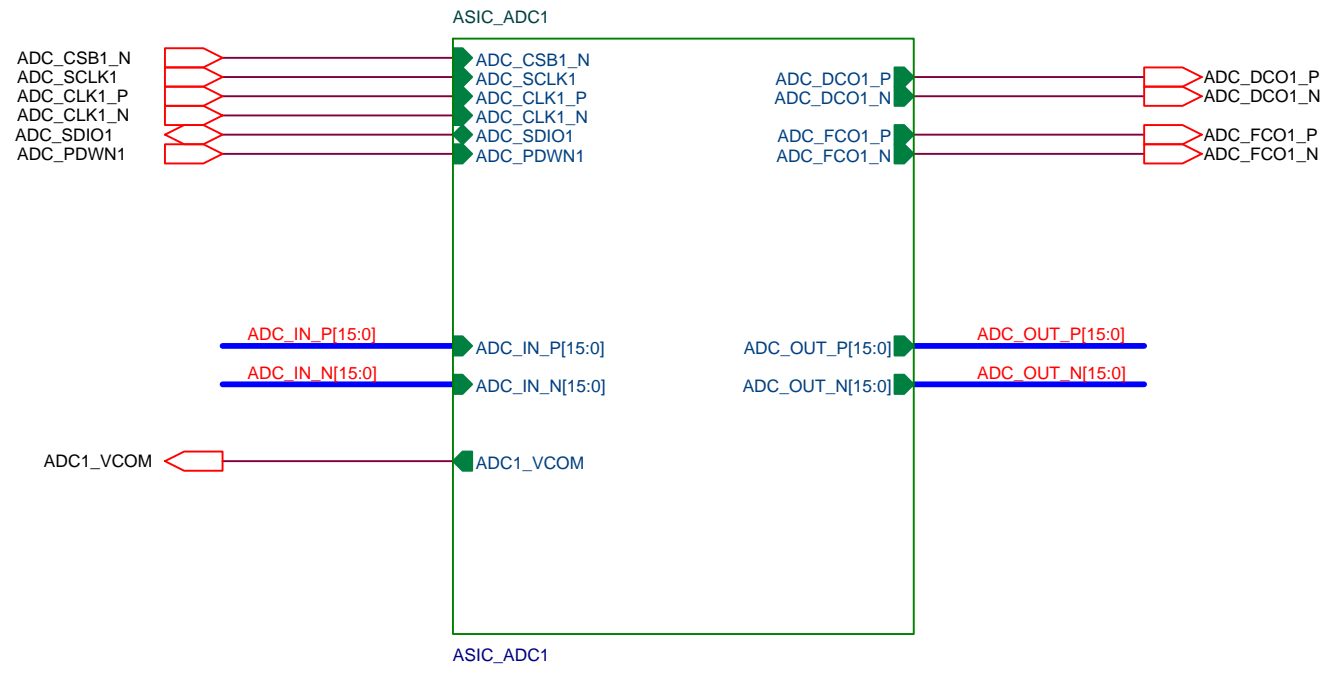
ANALOG DIFFERENTIAL



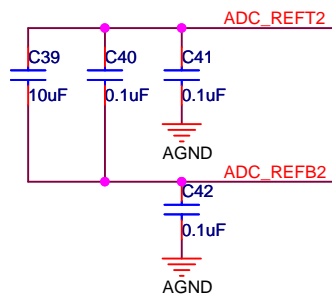
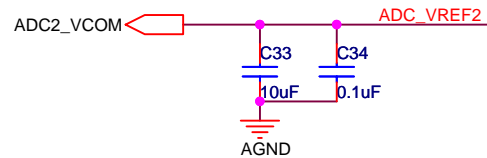
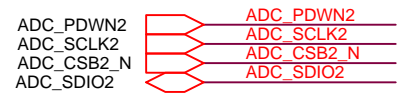
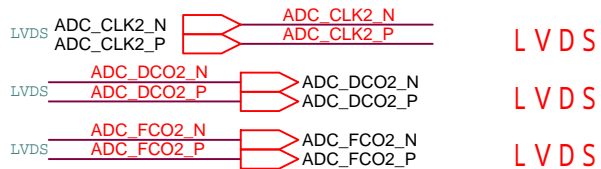
65ピンはパッケージの裏の面です



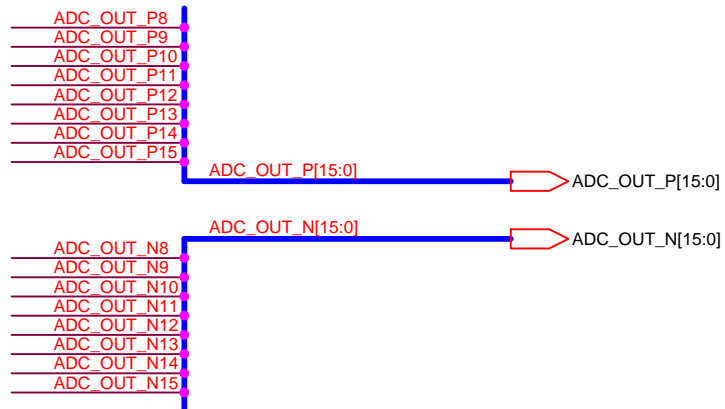
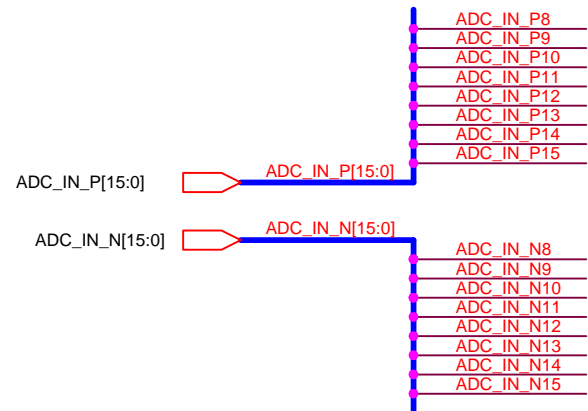
Title		
ASIC_ADC1		
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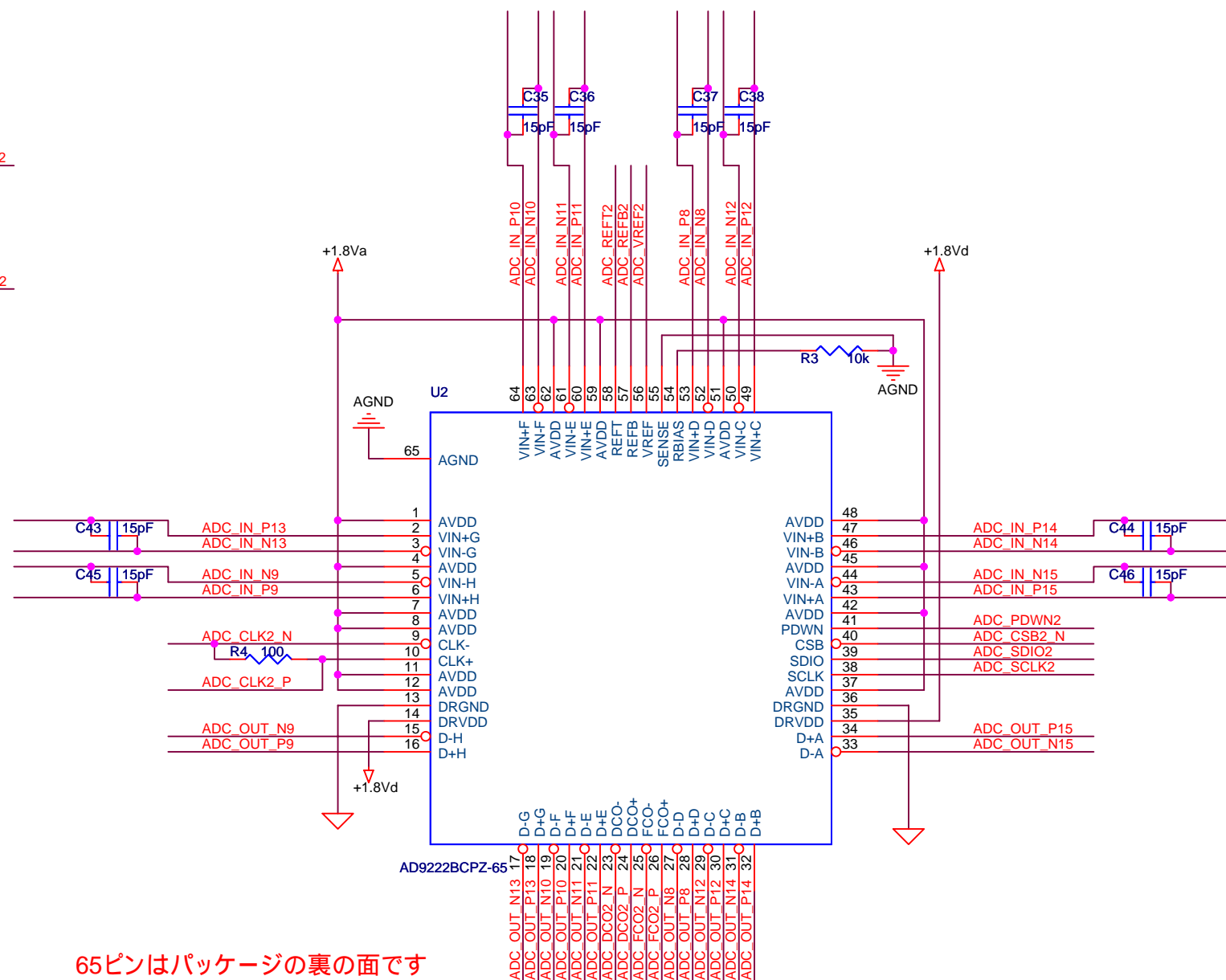
Title		
ASIC_ADC16		
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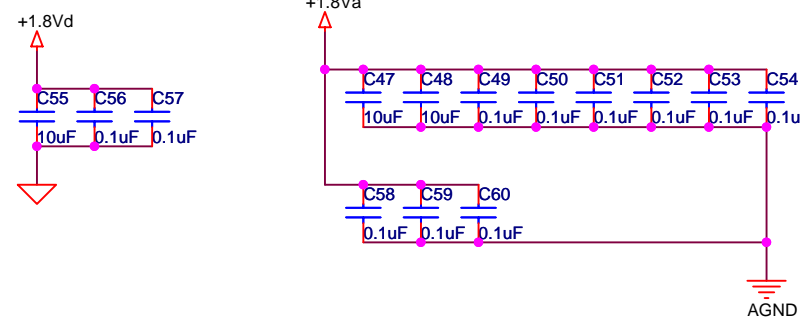
ANALOG DIFFERENTIAL



LVDS

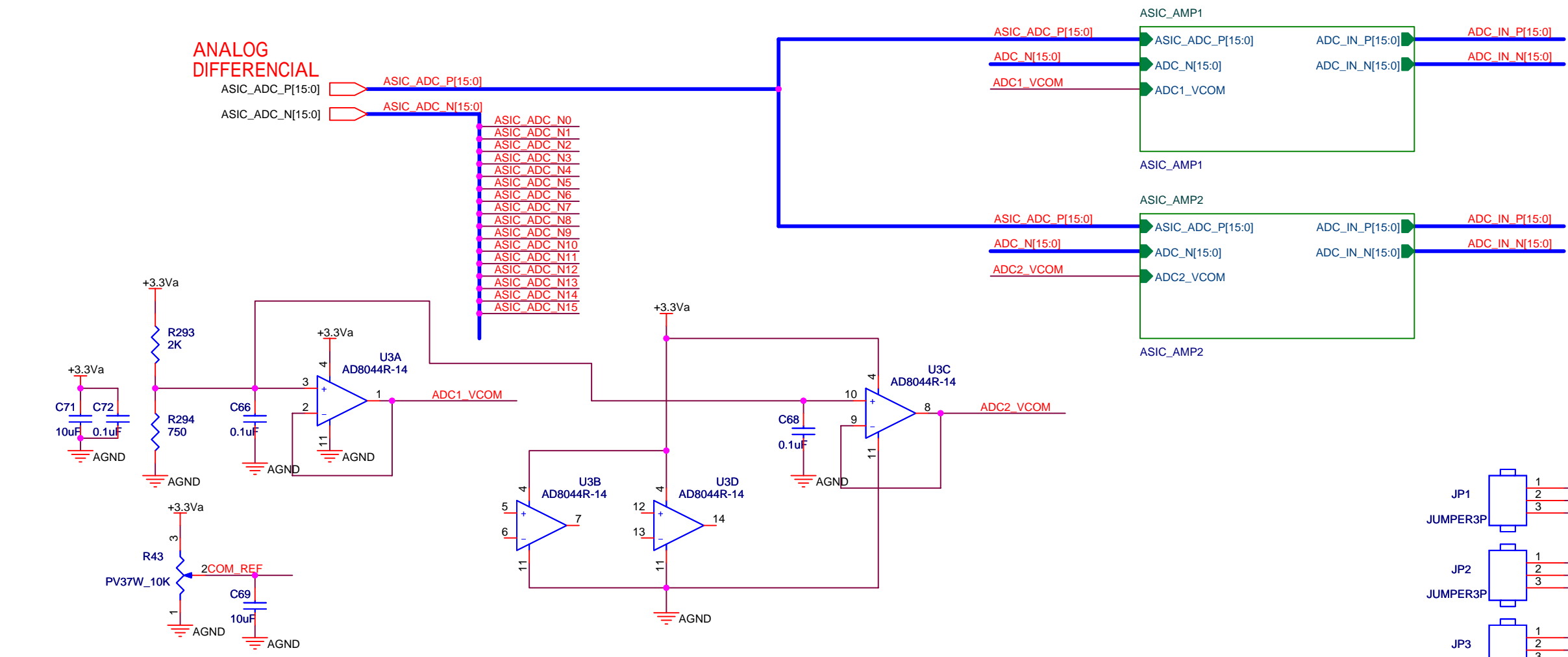


65ピンはパッケージの裏の面です

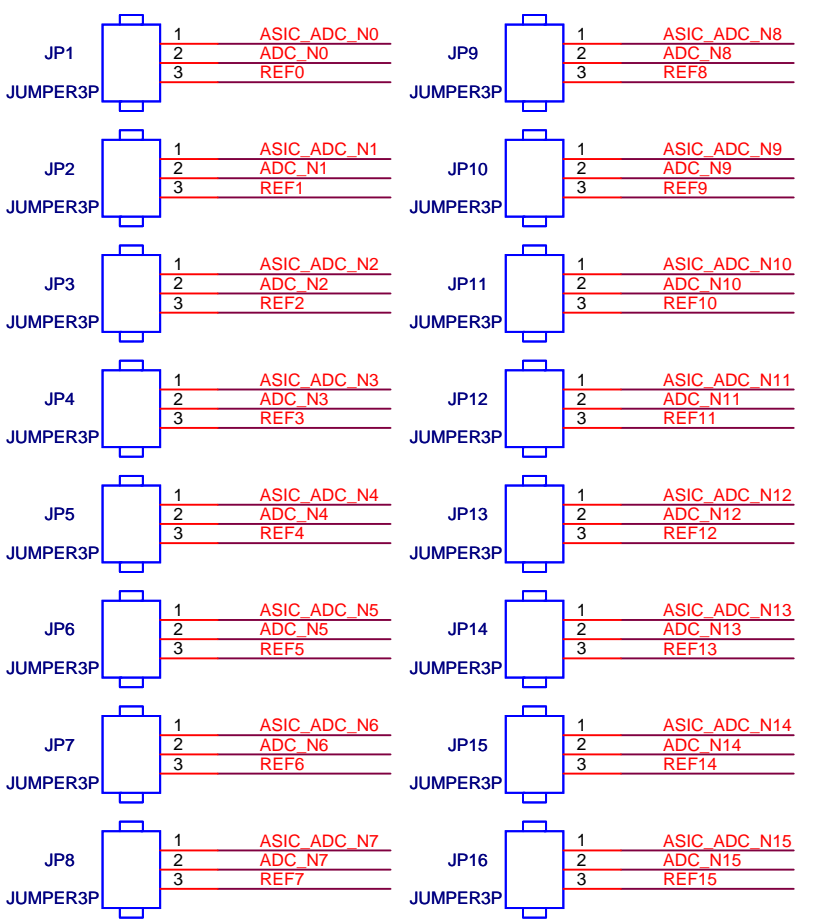
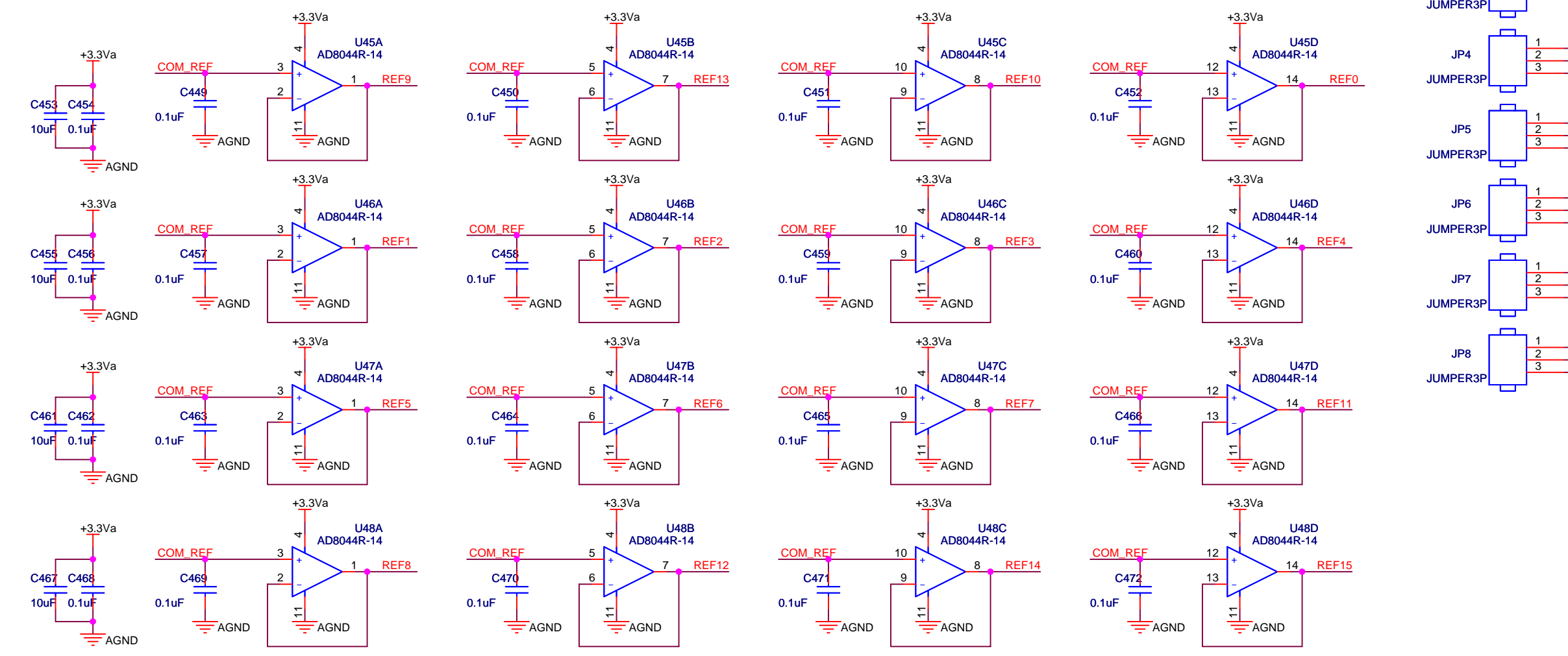


Title ASIC_ADC2		
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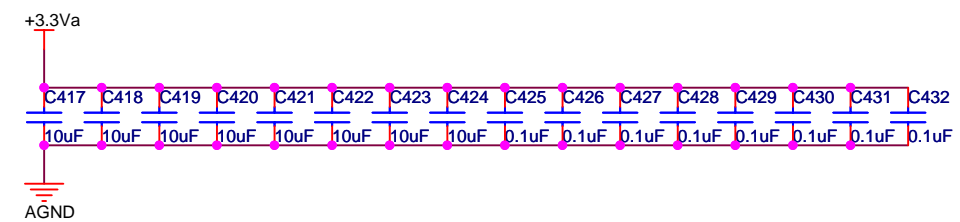
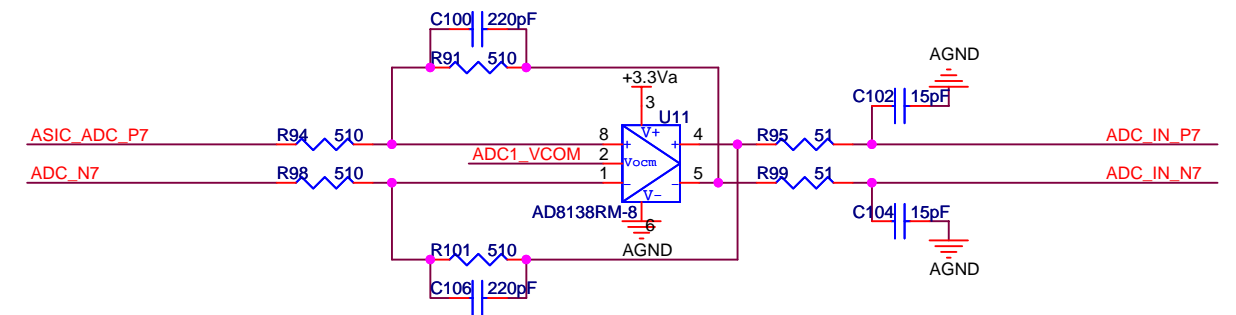
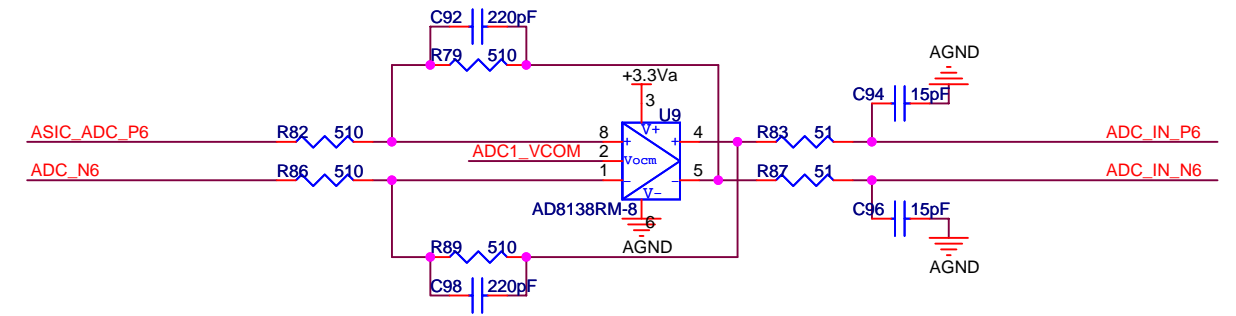
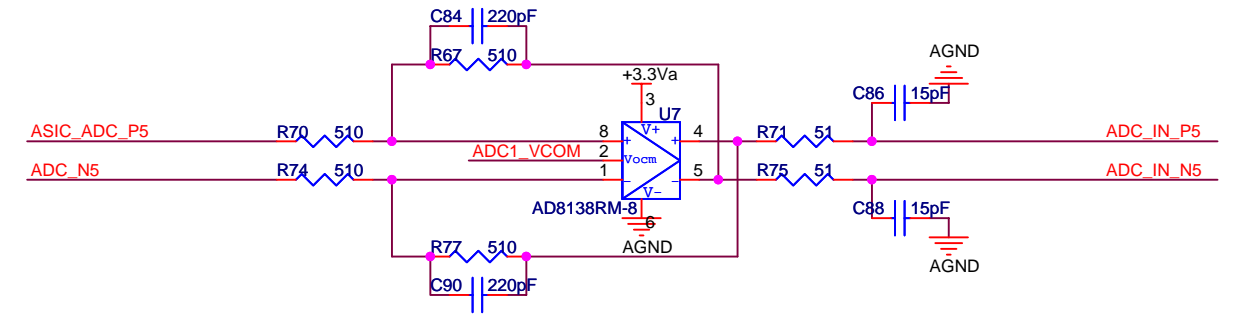
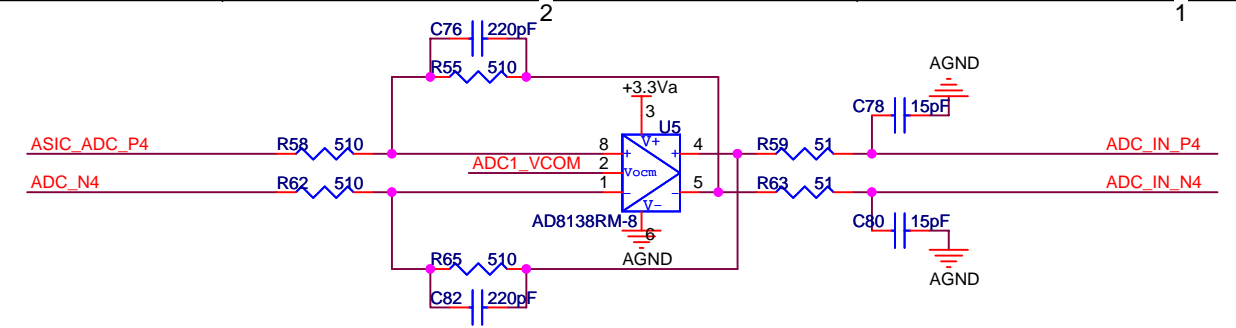
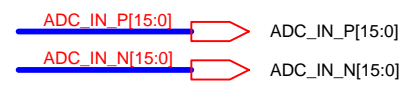
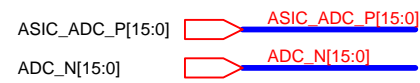
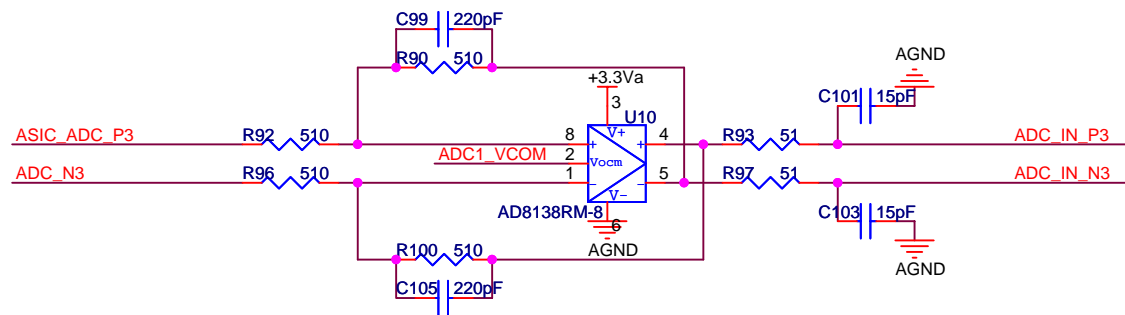
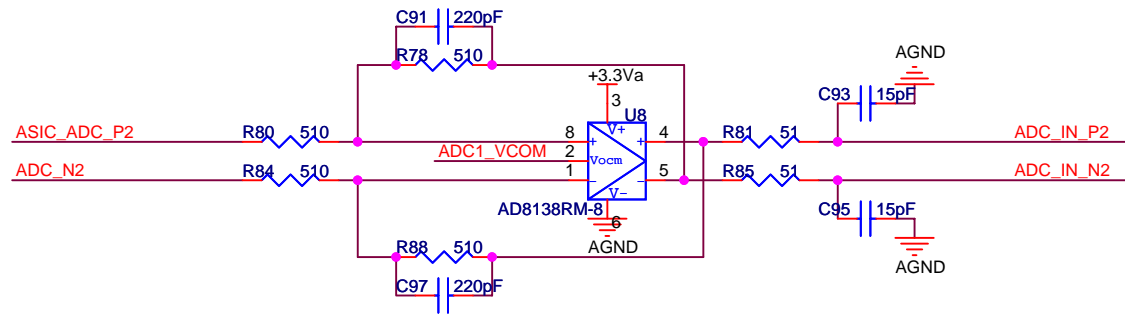
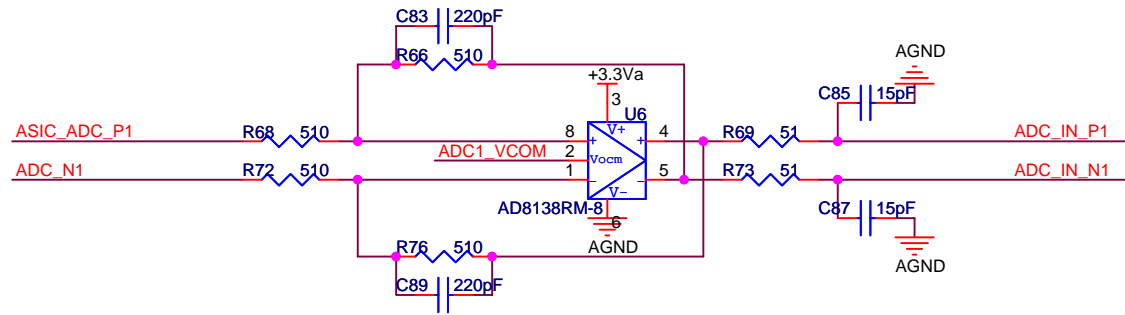
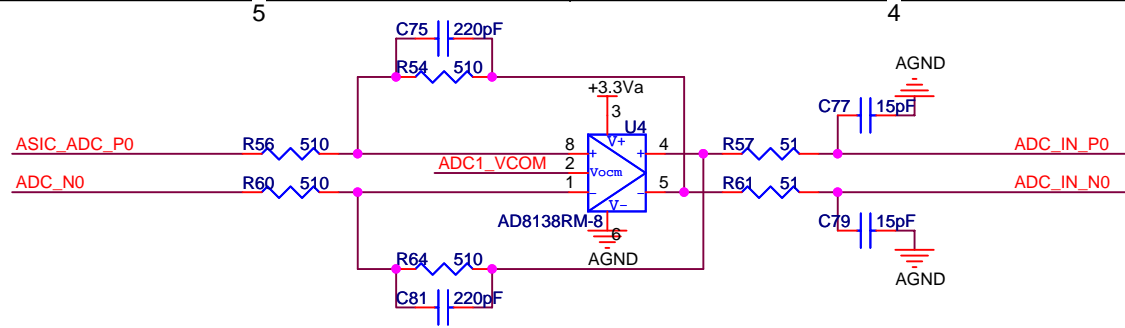
ANALOG DIFFERENTIAL



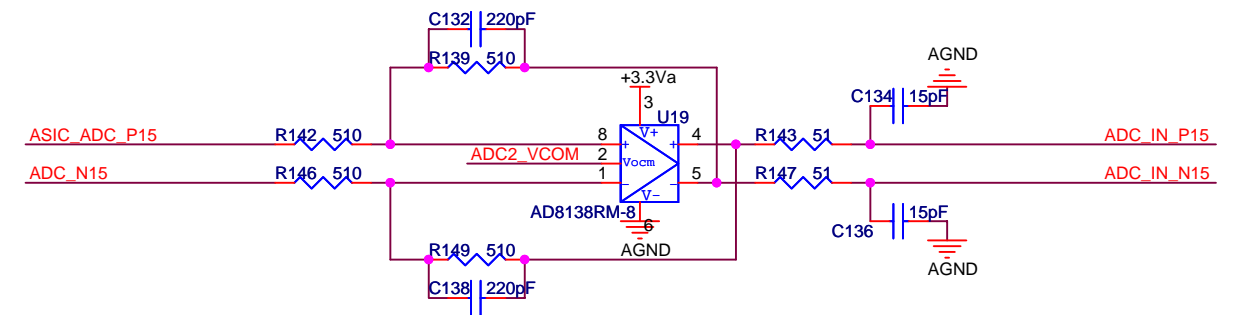
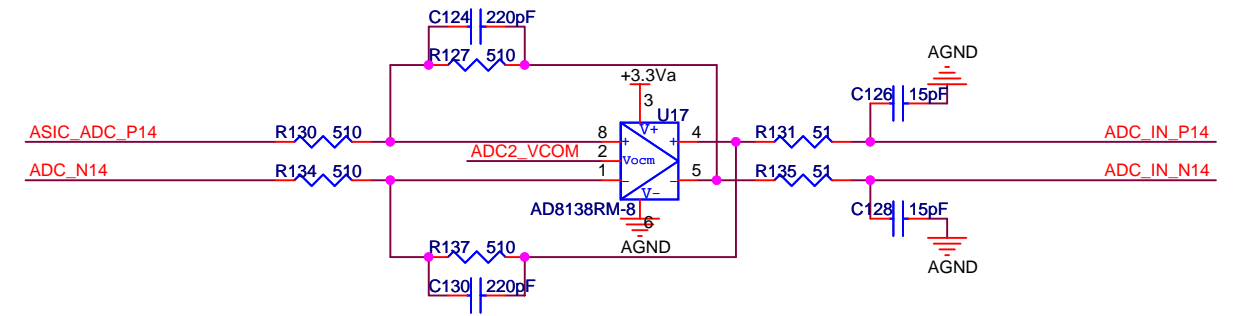
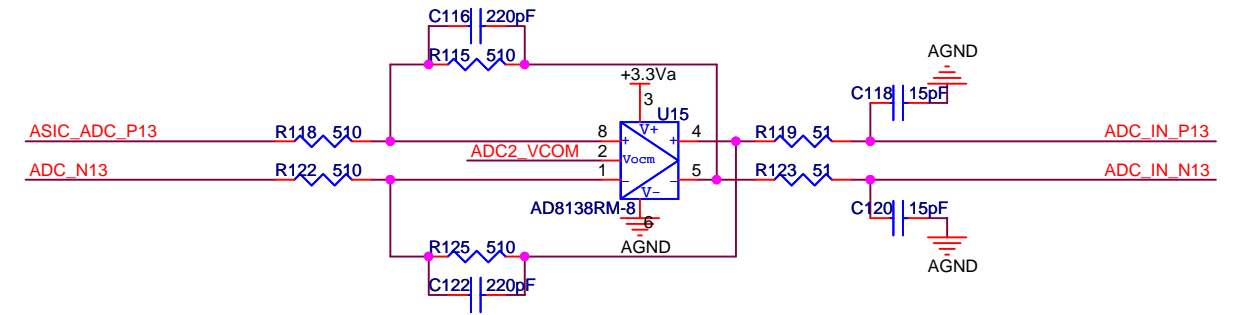
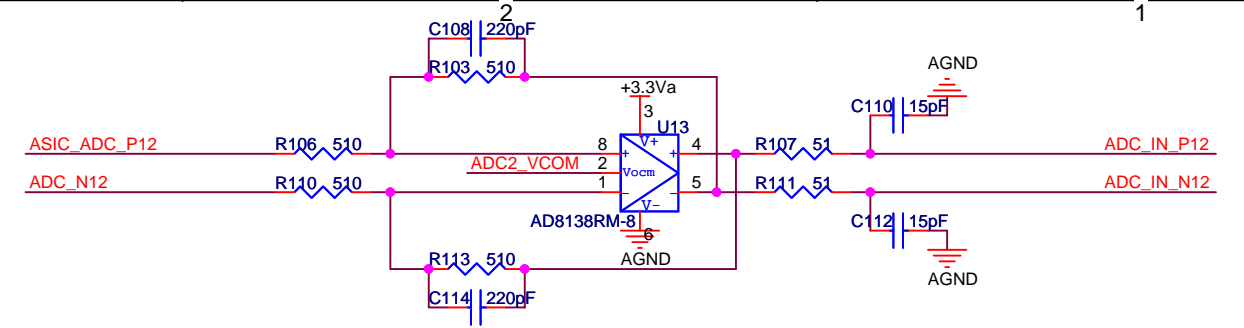
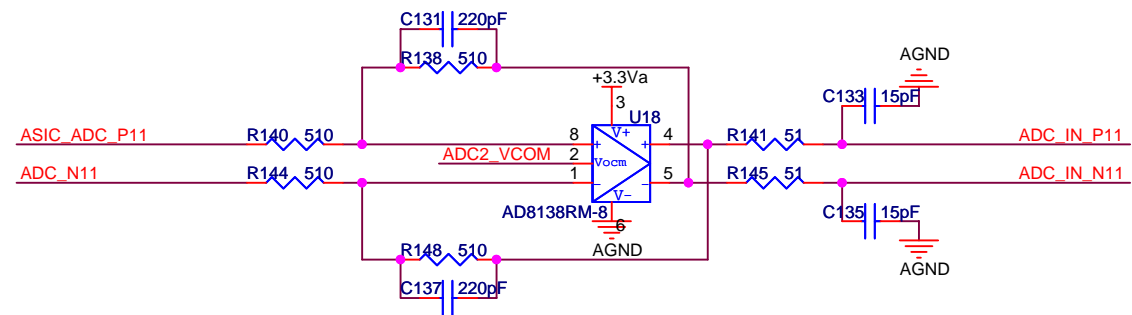
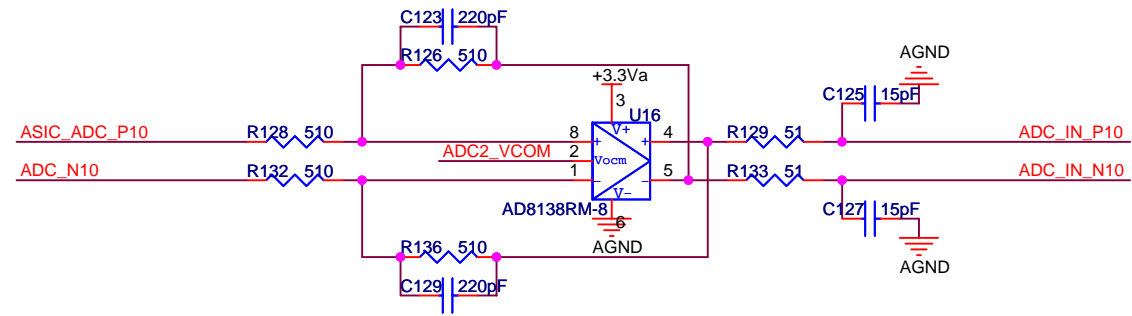
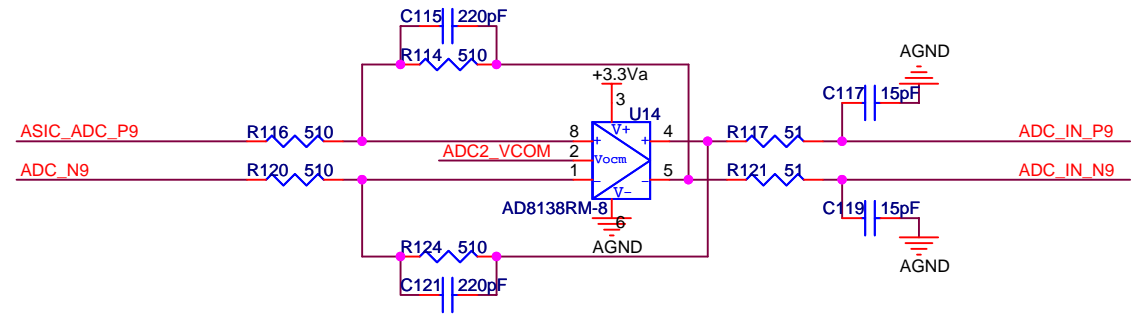
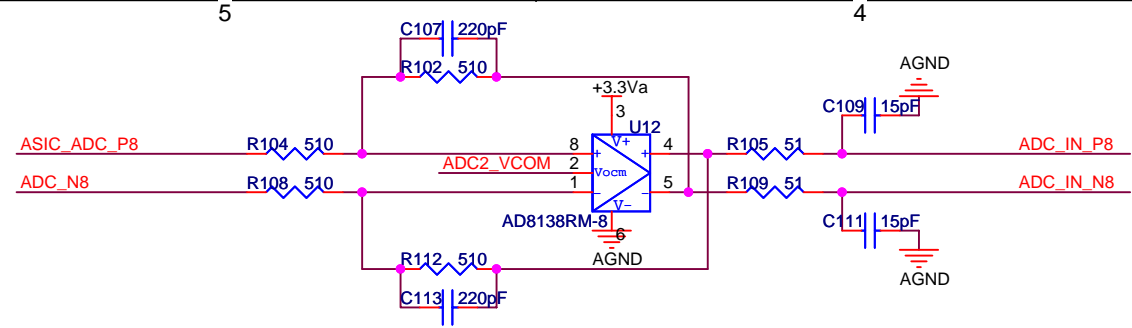
Pedestal SELECT
 1:2=ASIC ADC
 2:3=INT VR



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ASIC_ADC_INPUT		
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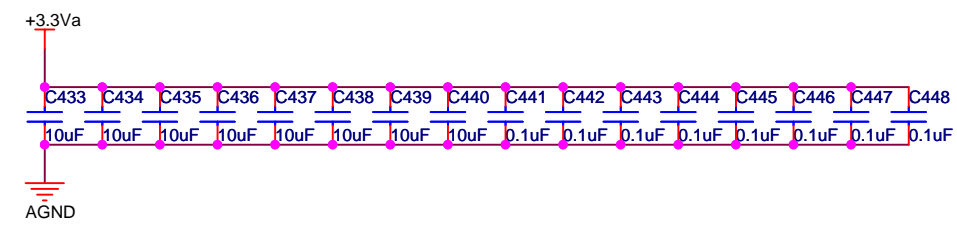
Title		
ASIC_AMP1		
Size	Document Number	Rev
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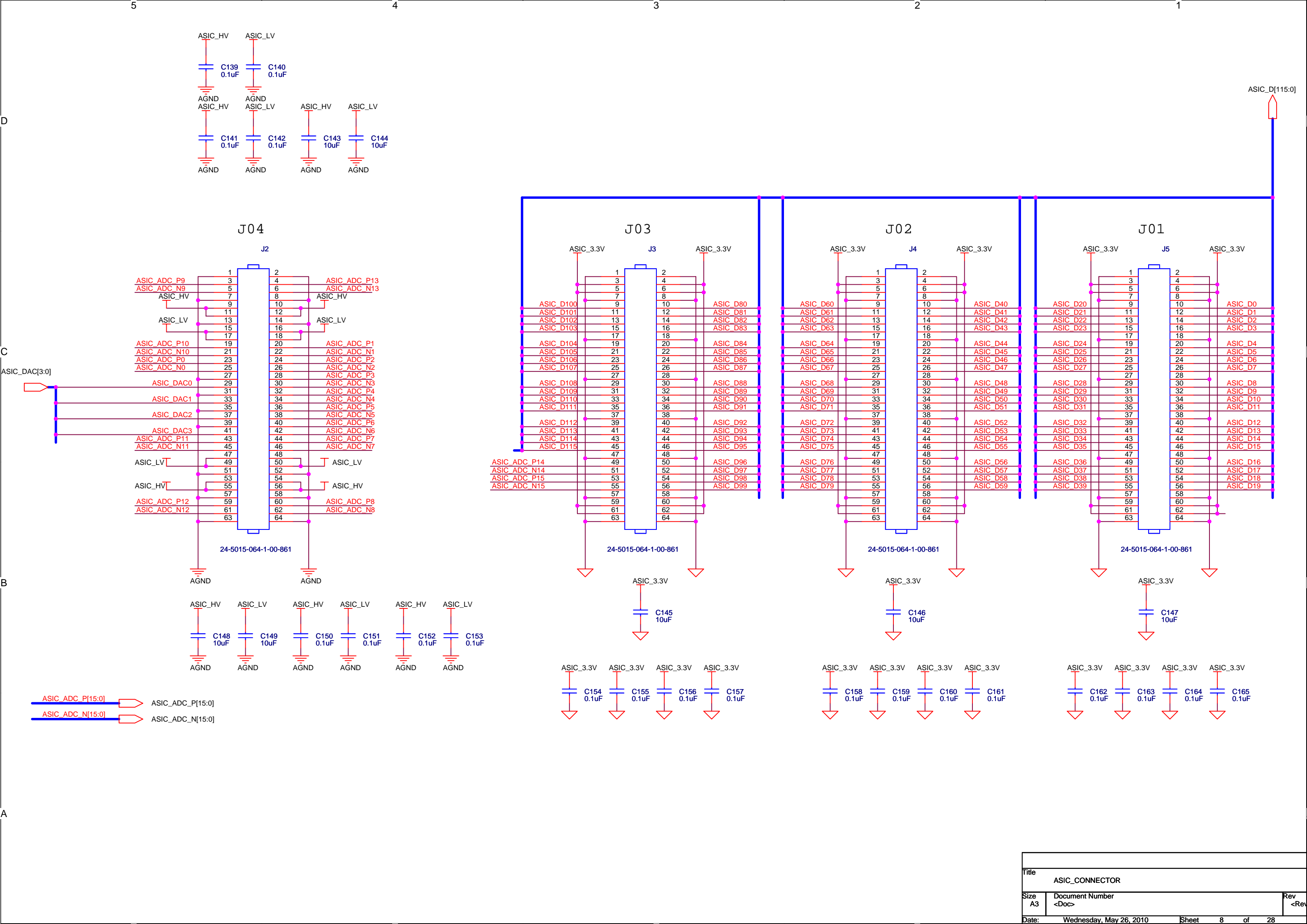
ASIC_ADC_P[15:0] ASIC_ADC_P[15:0]
 ADC_N[15:0] ADC_N[15:0]

ADC_IN_P[15:0] ADC_IN_P[15:0]
 ADC_IN_N[15:0] ADC_IN_N[15:0]

ADC2_VCOM ADC2_VCOM



Title ASIC_AMP2		
Size A3	Document Number <Doc>	Rev <Rev>
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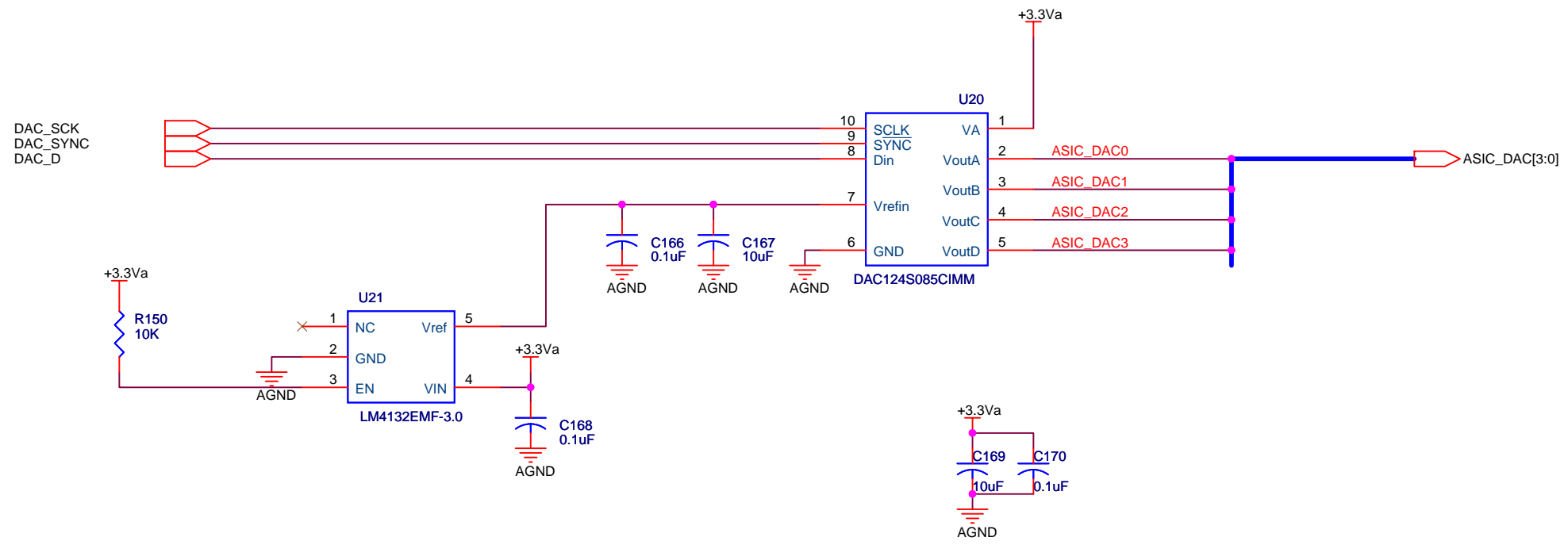


D

C

B

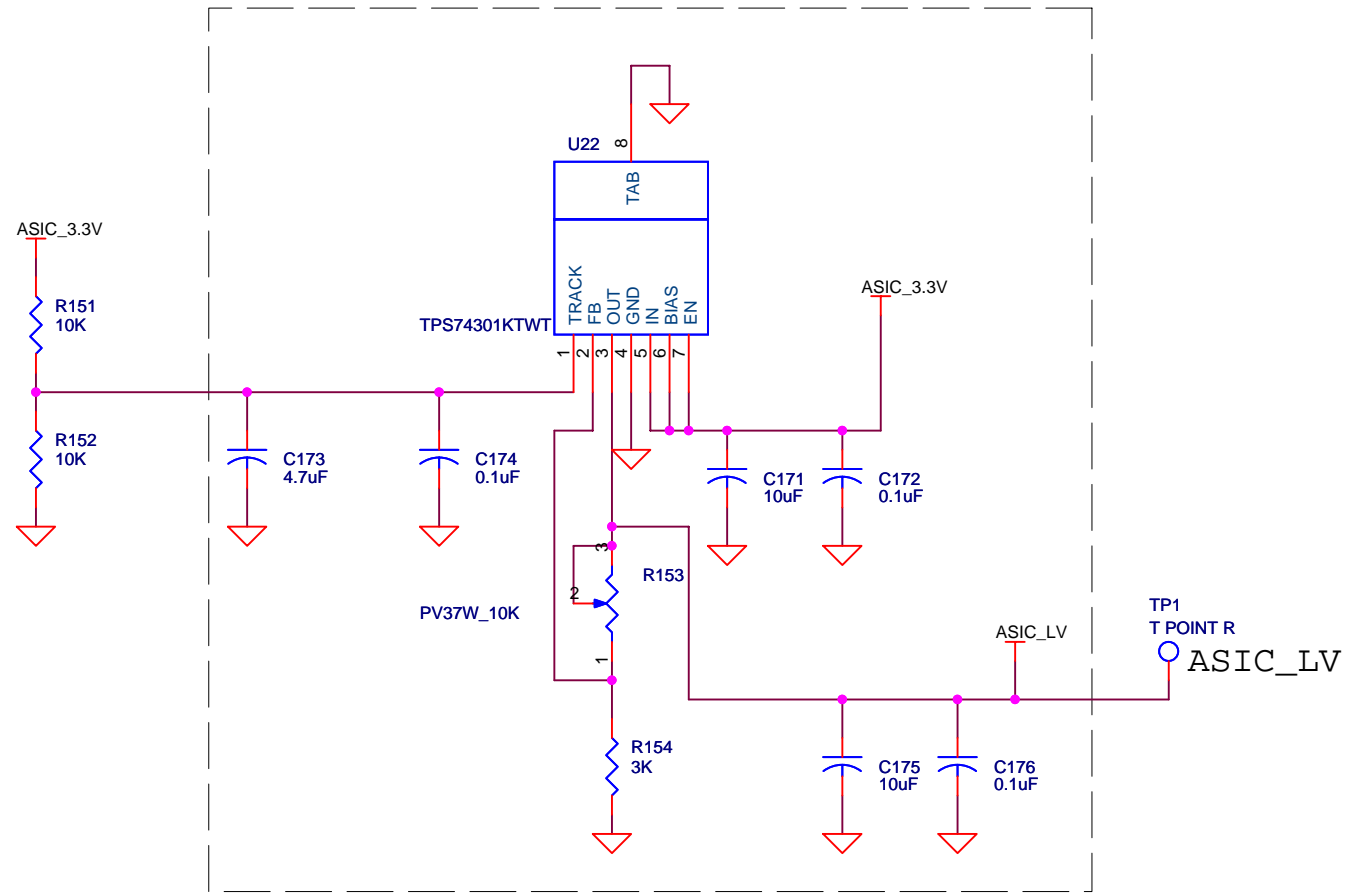
A



Title		
ASIC_DAC		
Size	Document Number	Rev
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For Low Voltage

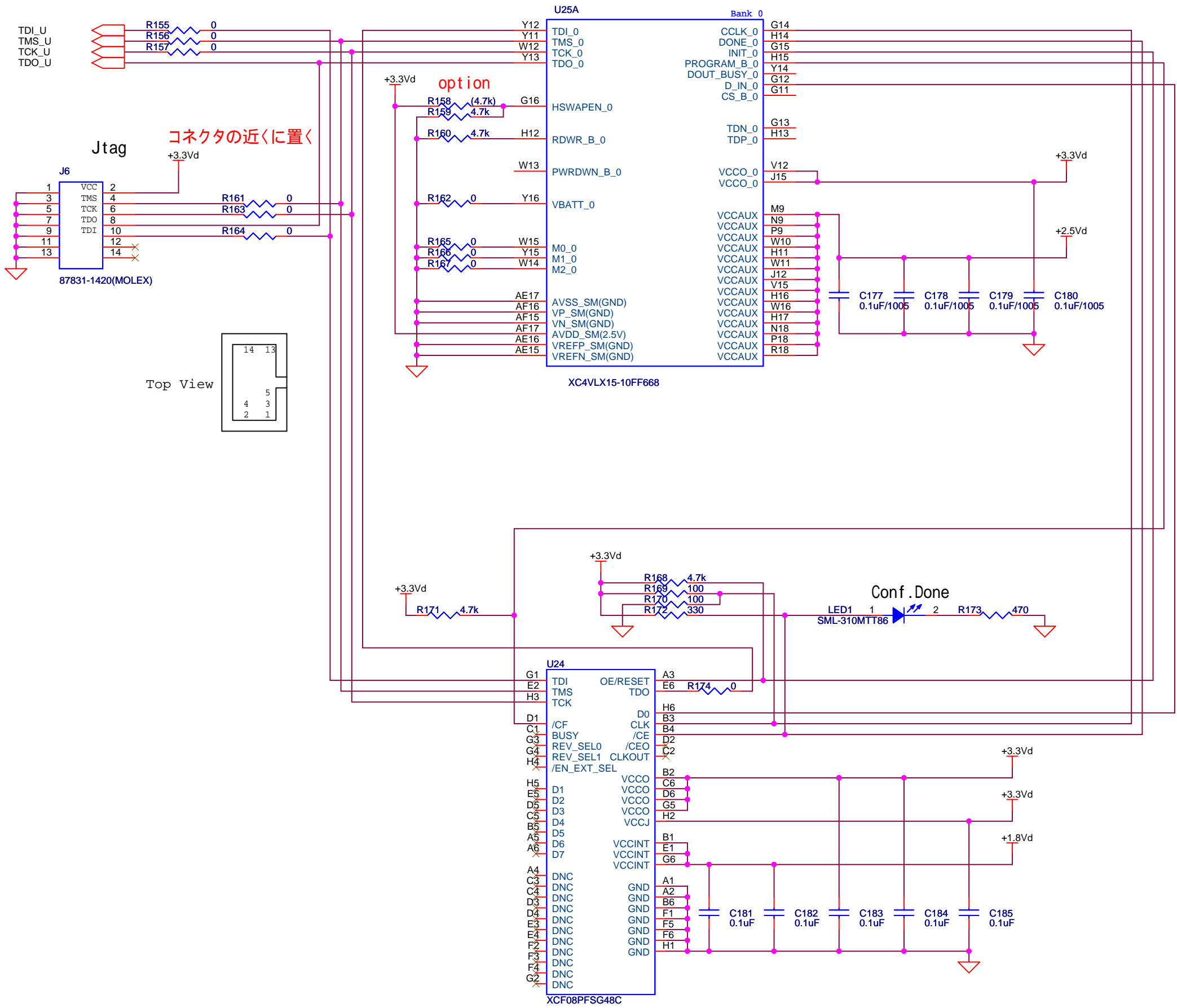
TABは放熱板です
必ず複数ビアで内層GNDへ落としてください。

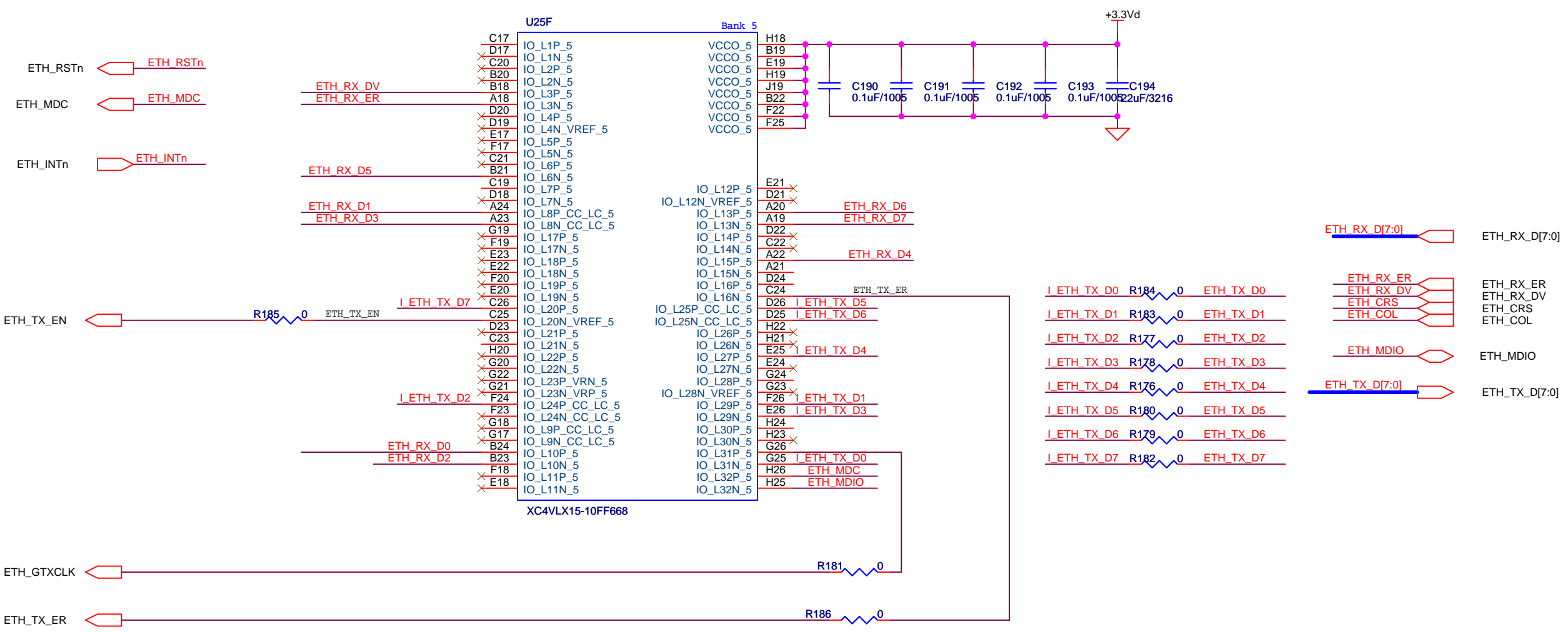
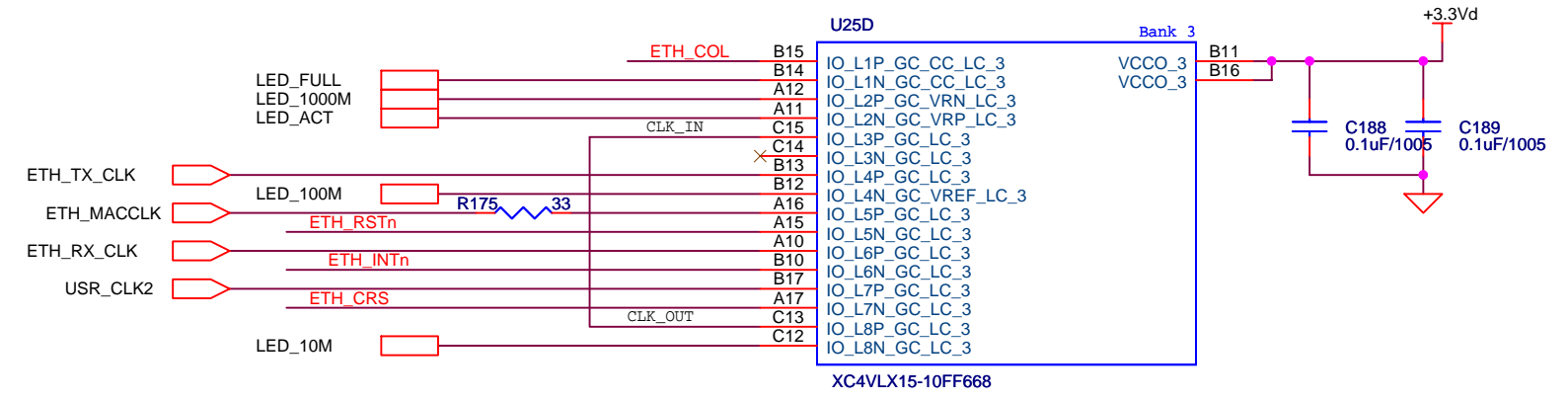
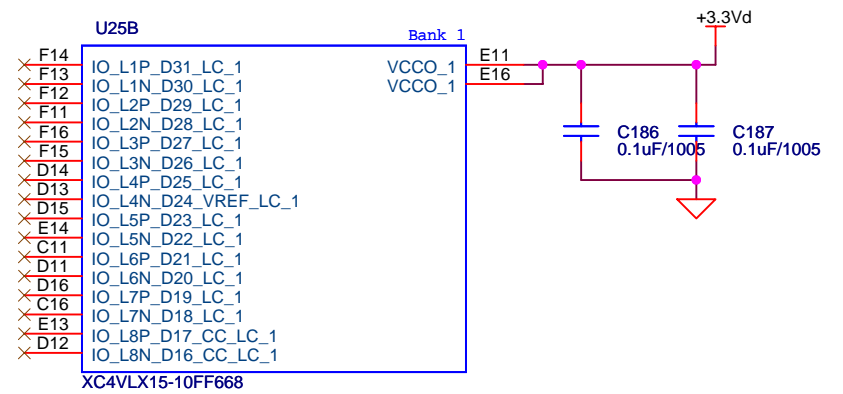


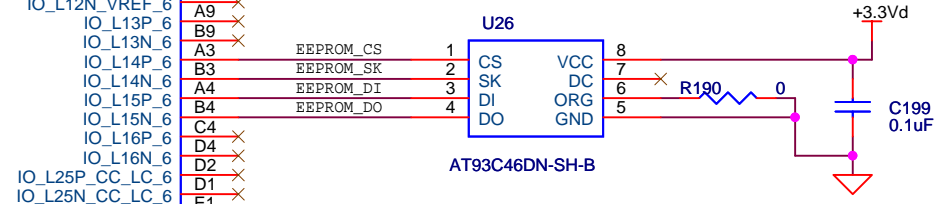
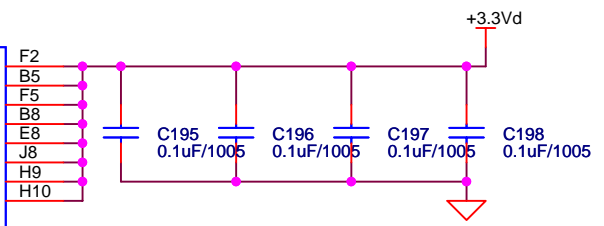
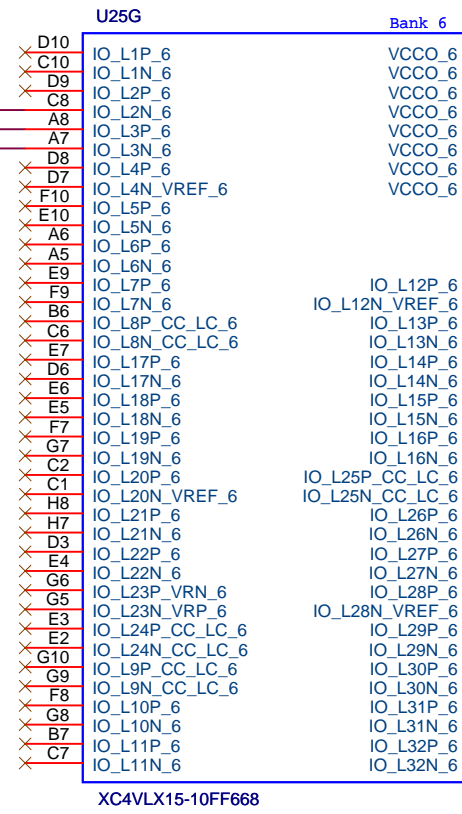
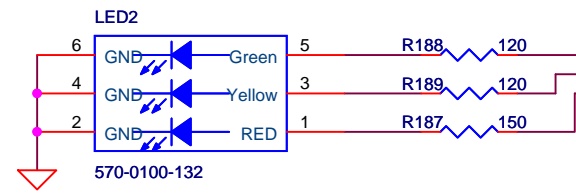
ICの近くに配置
VRは多回転型を使用してください



Title		
ASIC_POWER		
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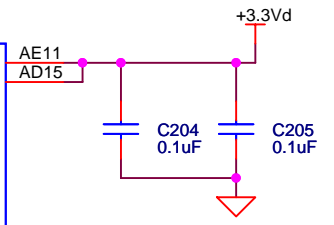
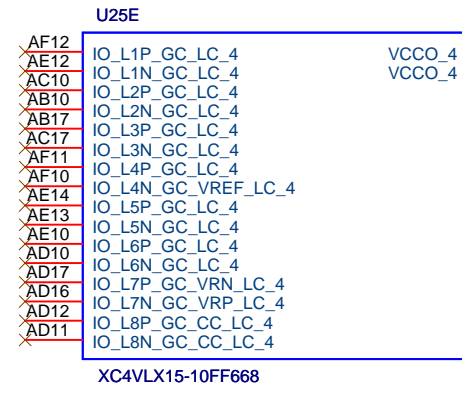
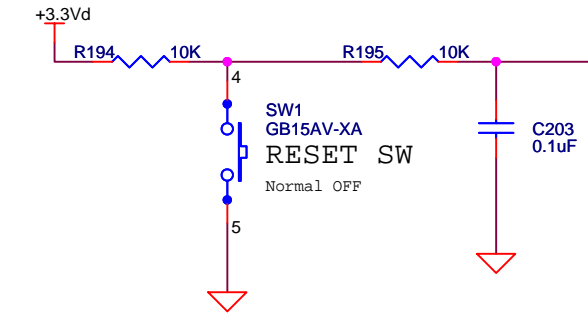
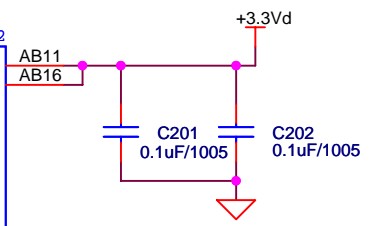
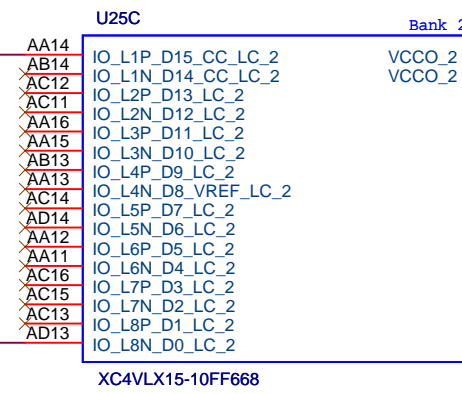
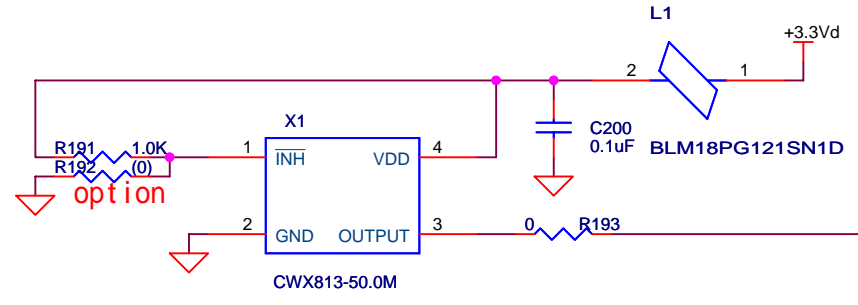


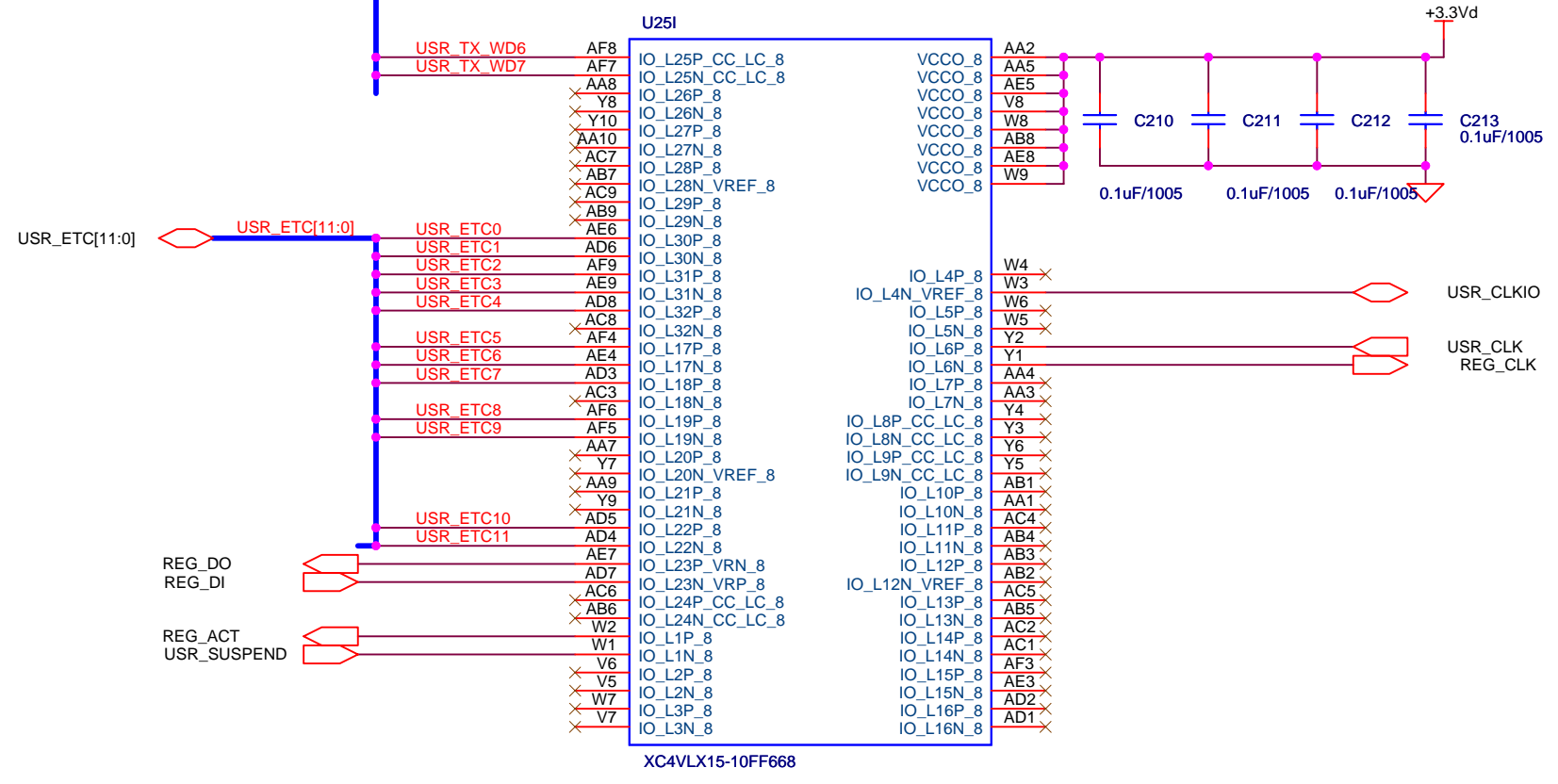
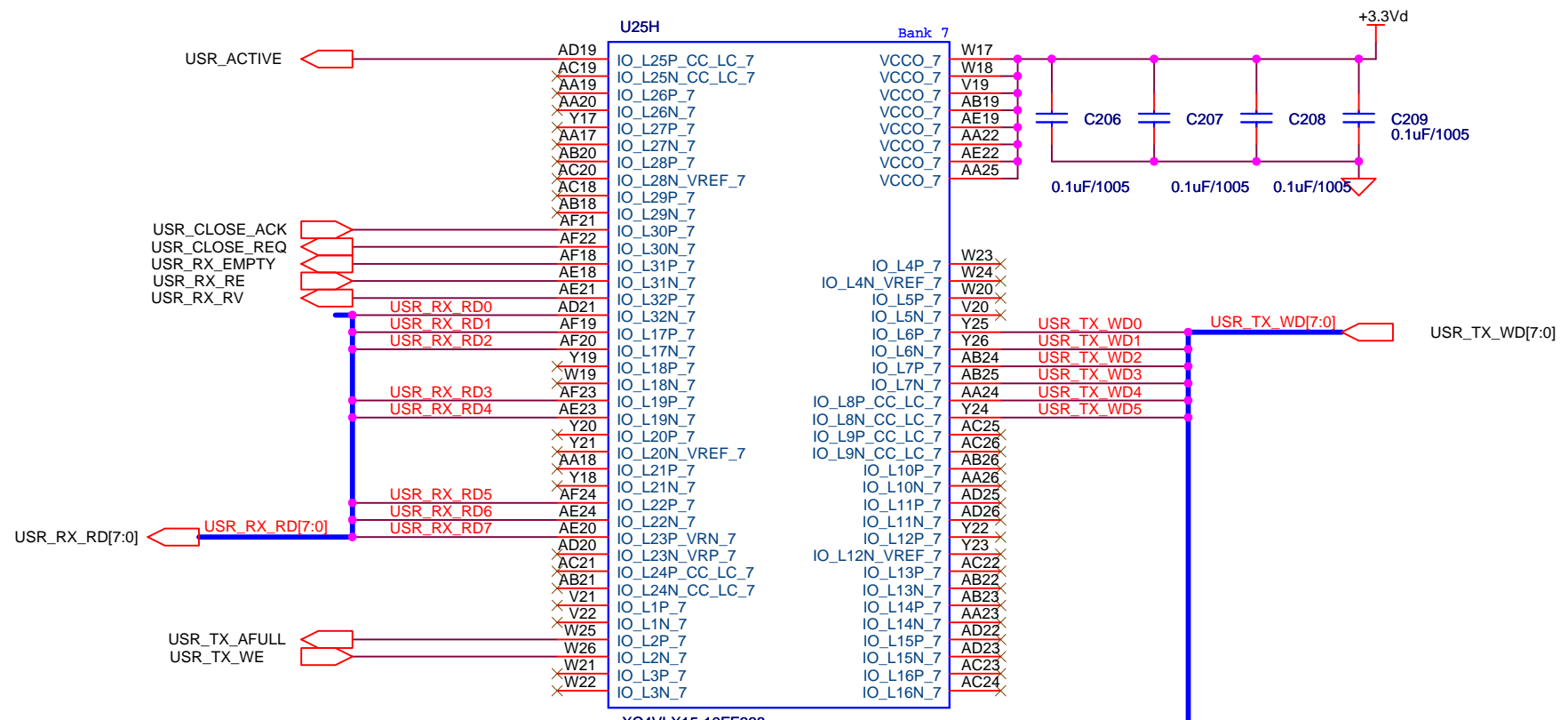


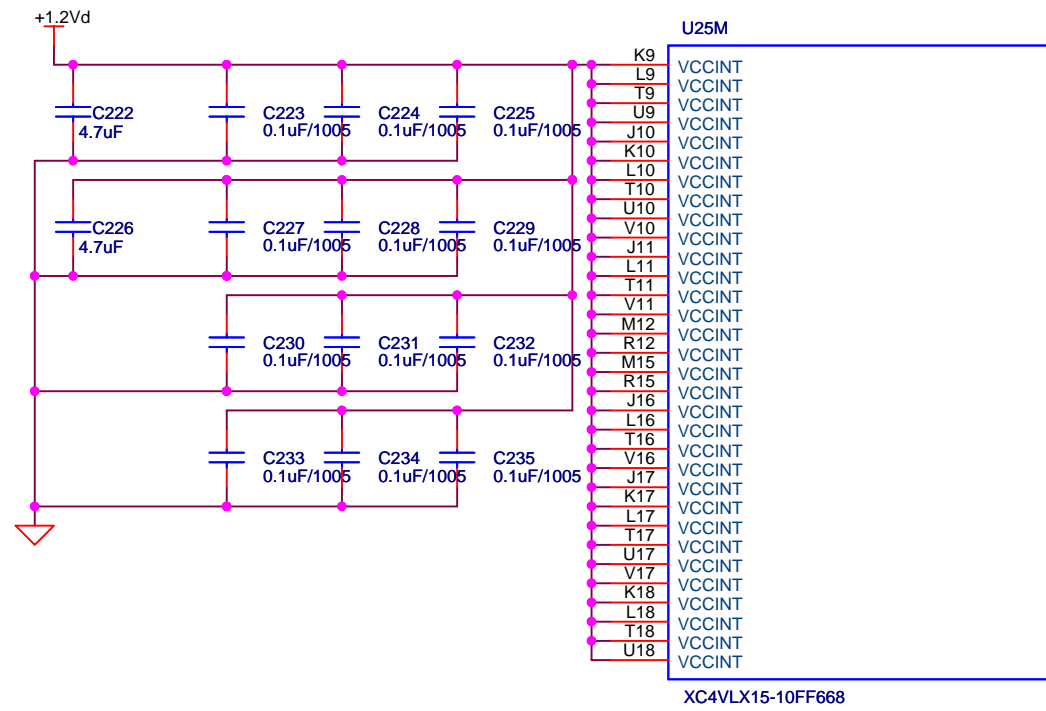
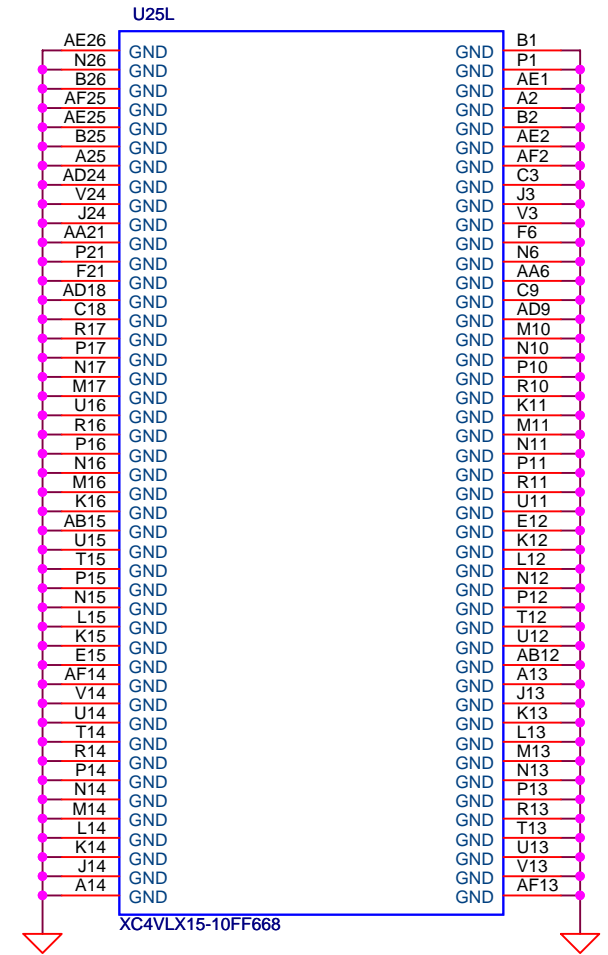
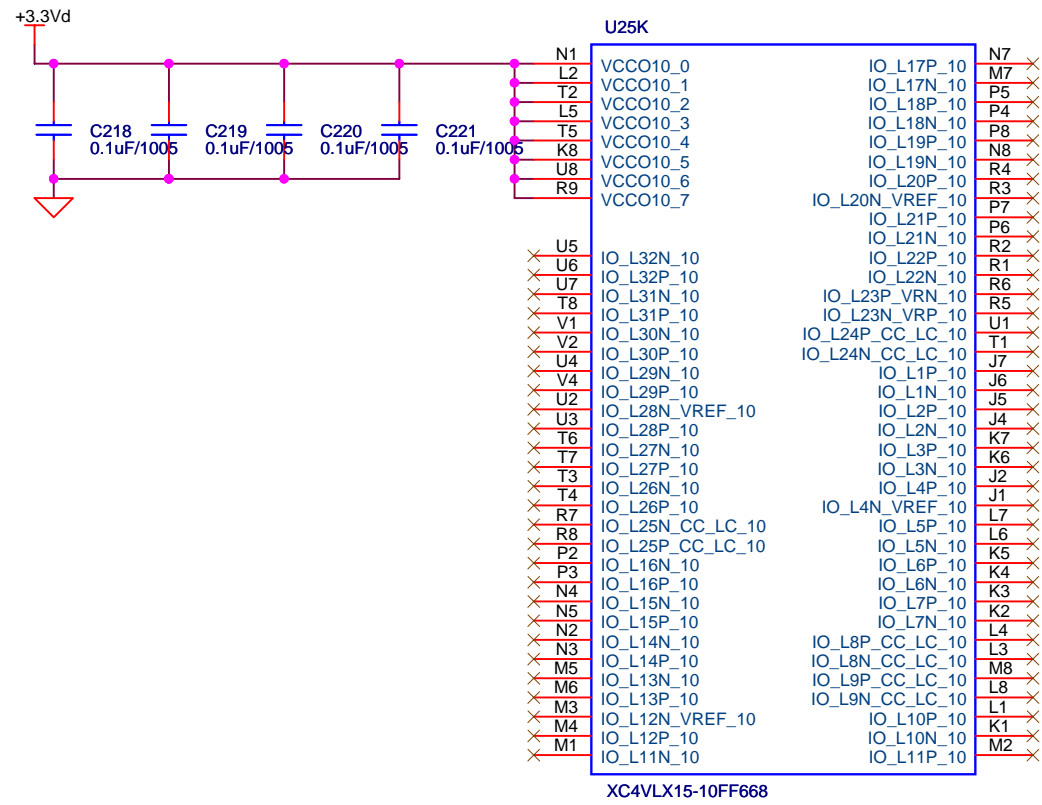
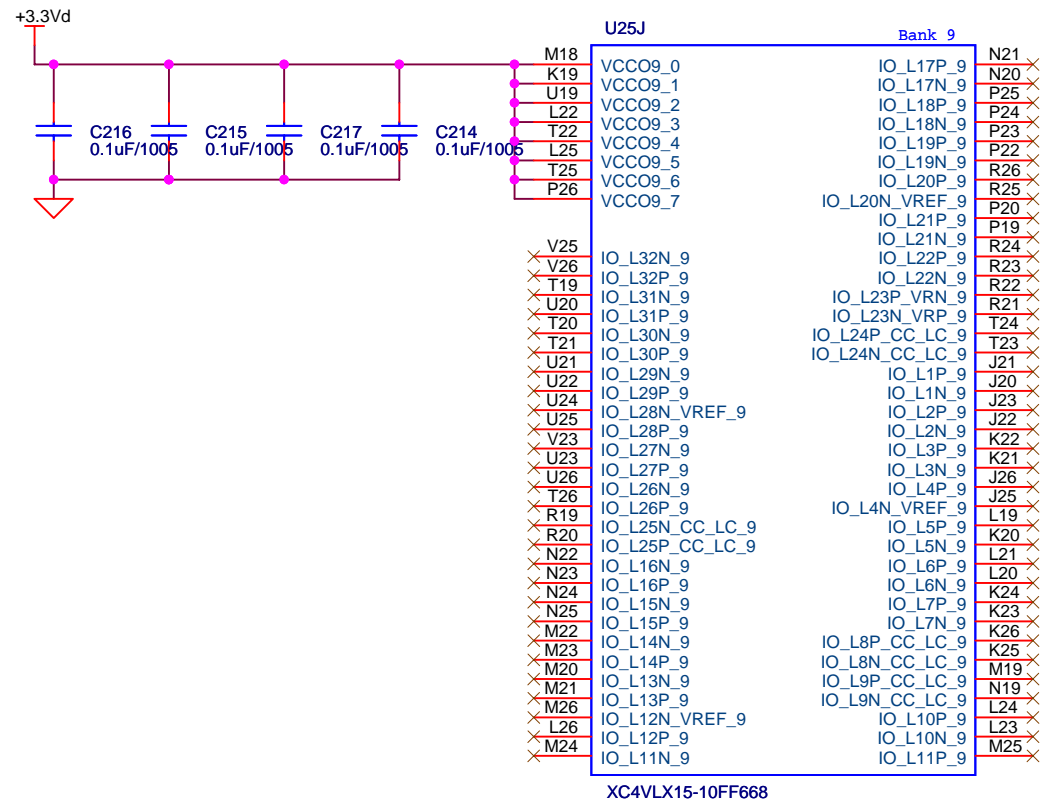


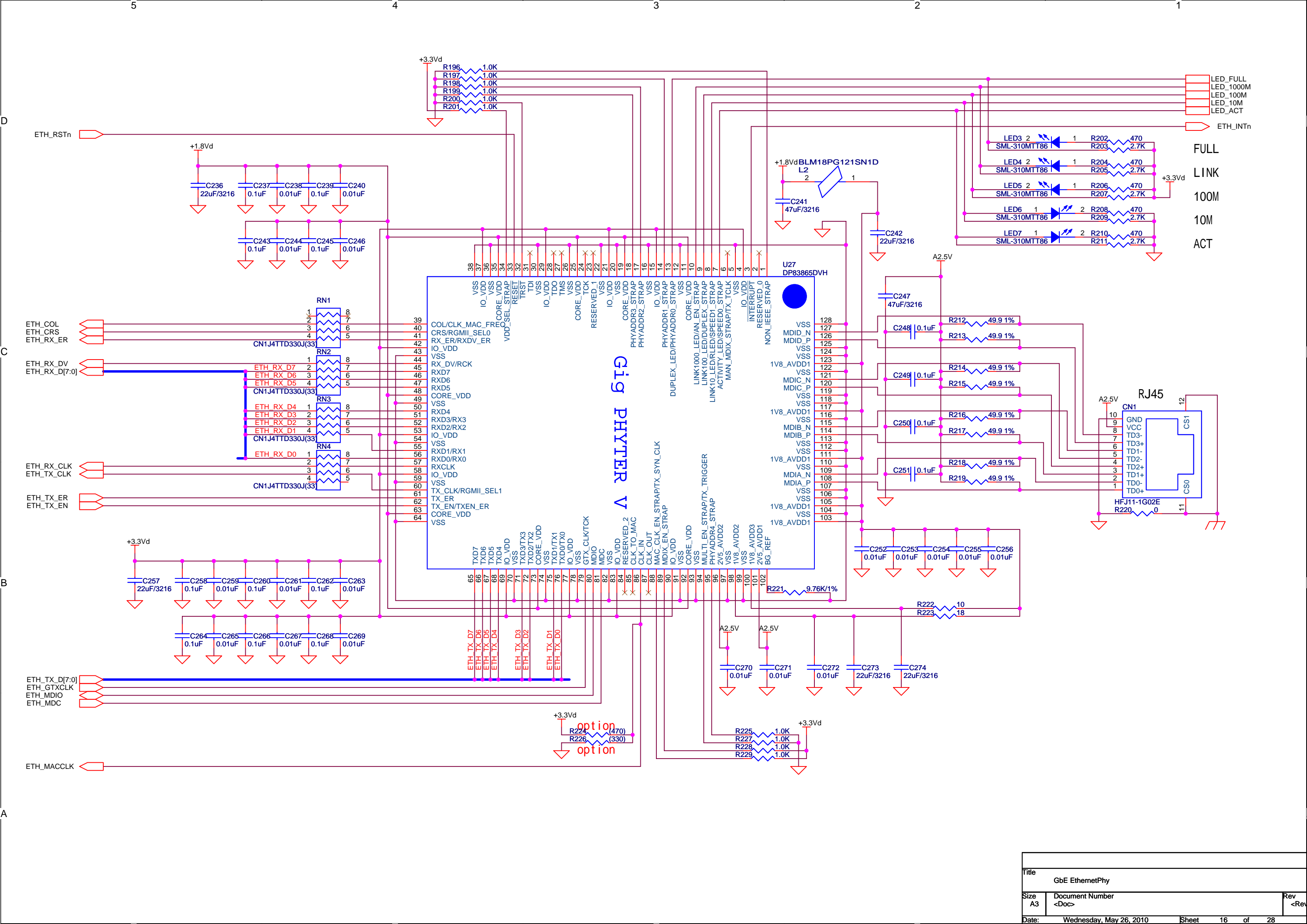
J7
Open: イニシャライズ時
Close: 通常動作

J8: 動作設定

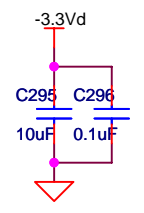
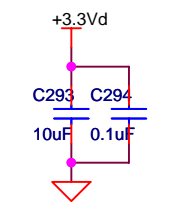
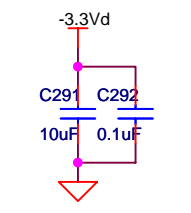
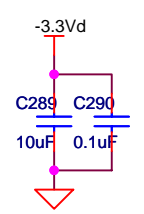
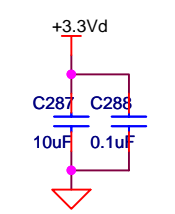
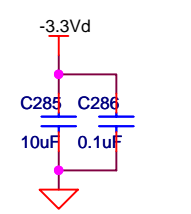
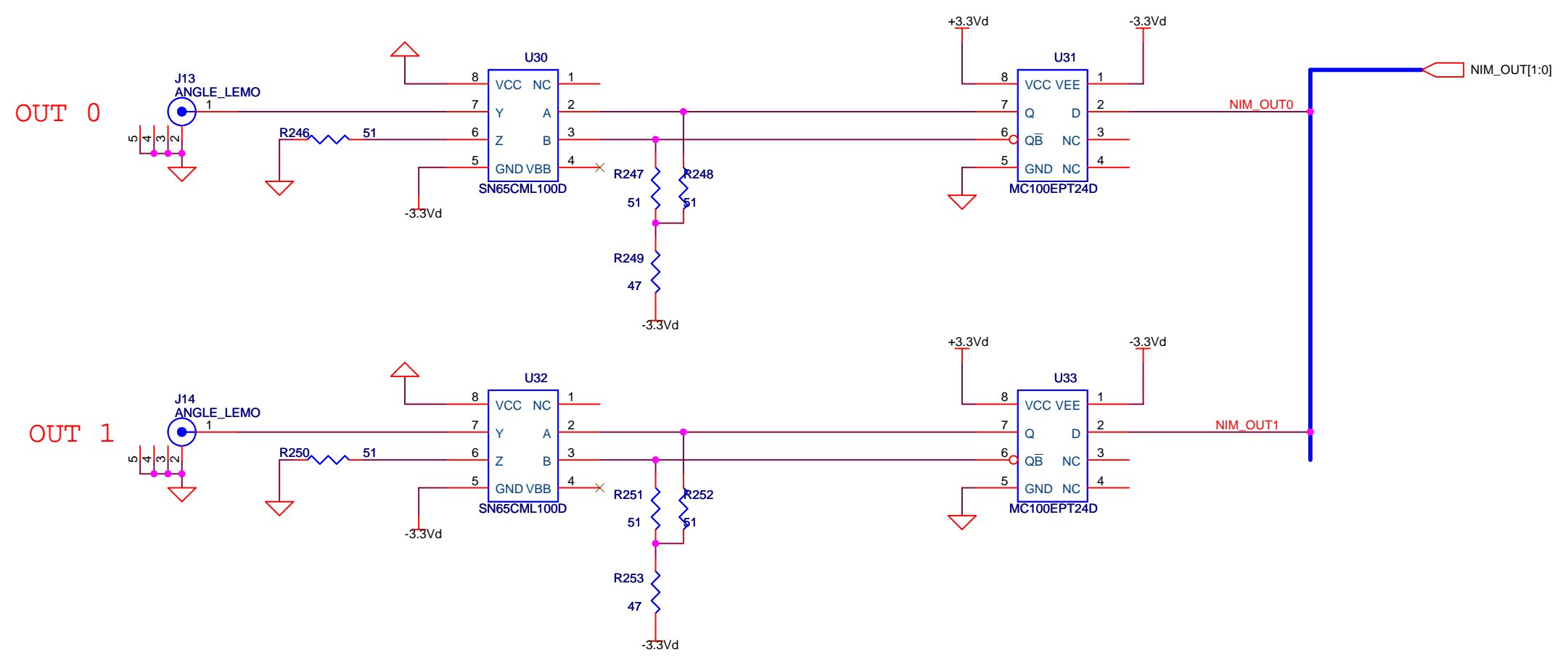
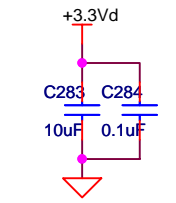
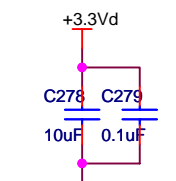
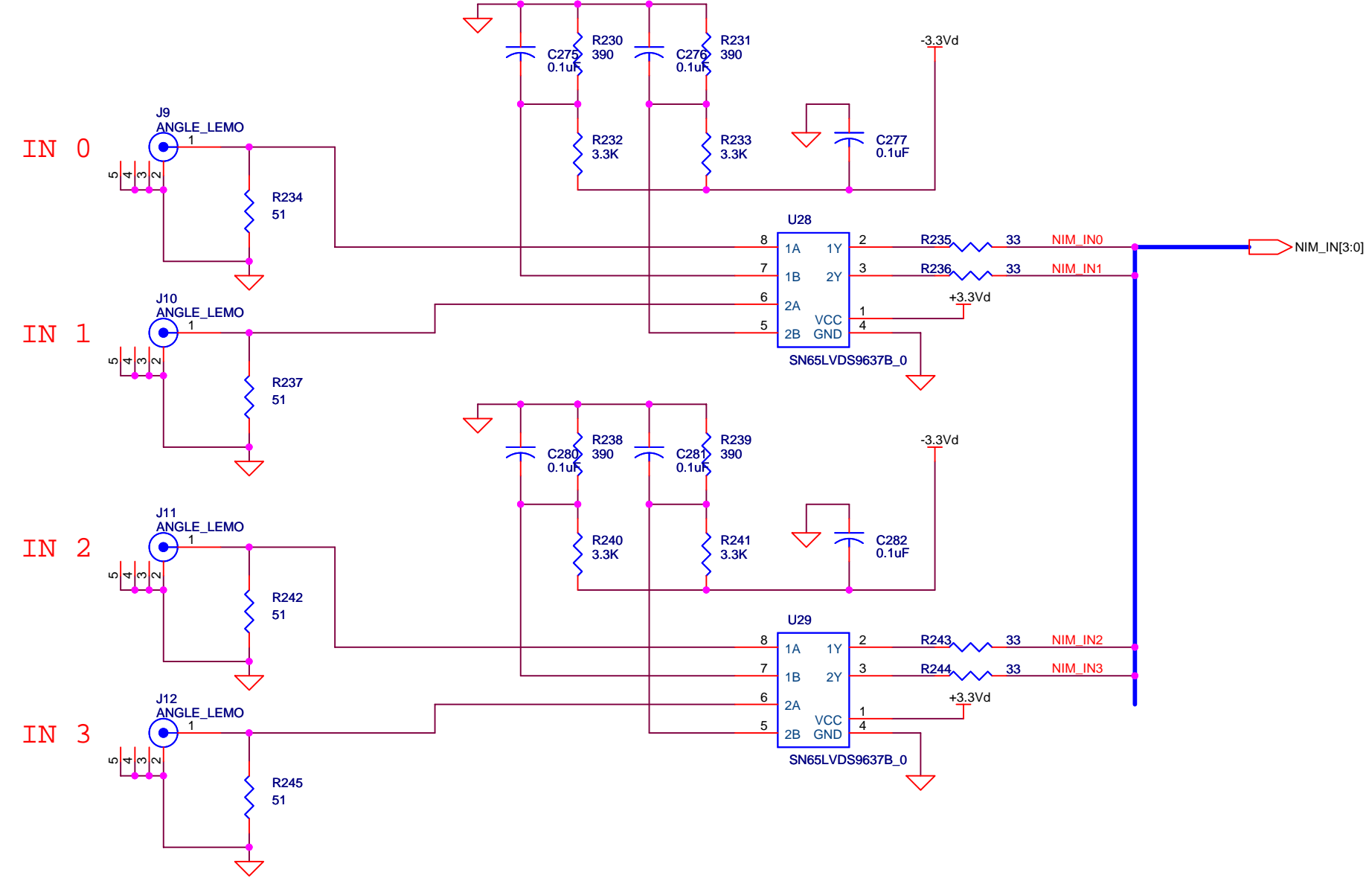




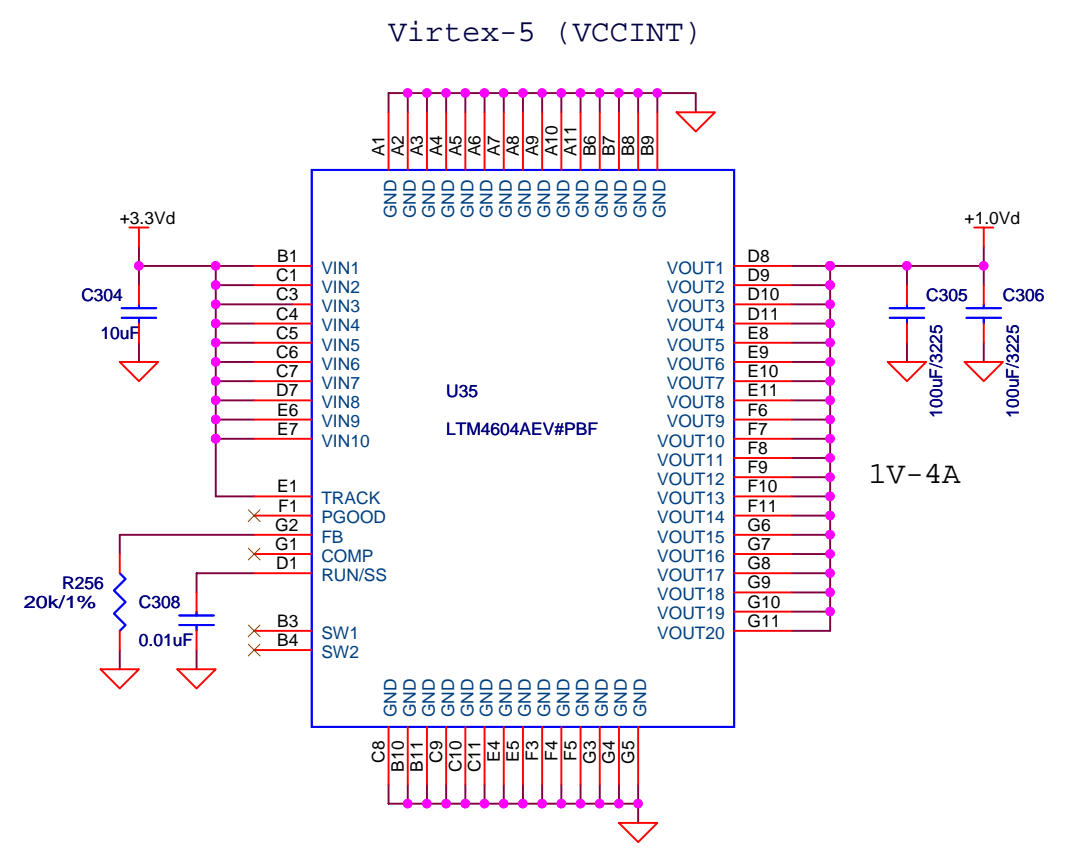
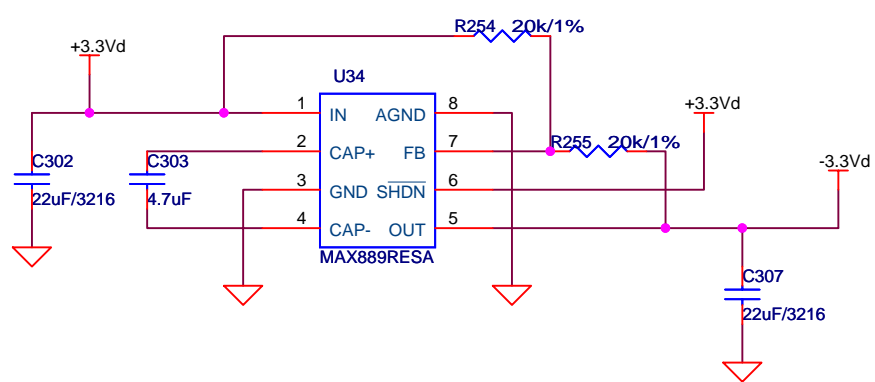
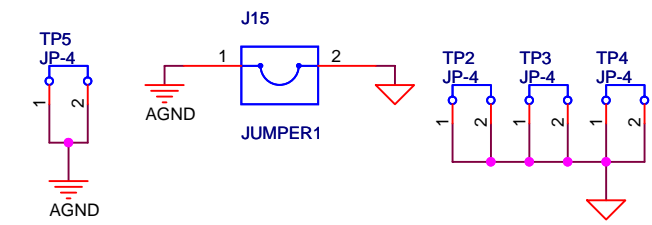
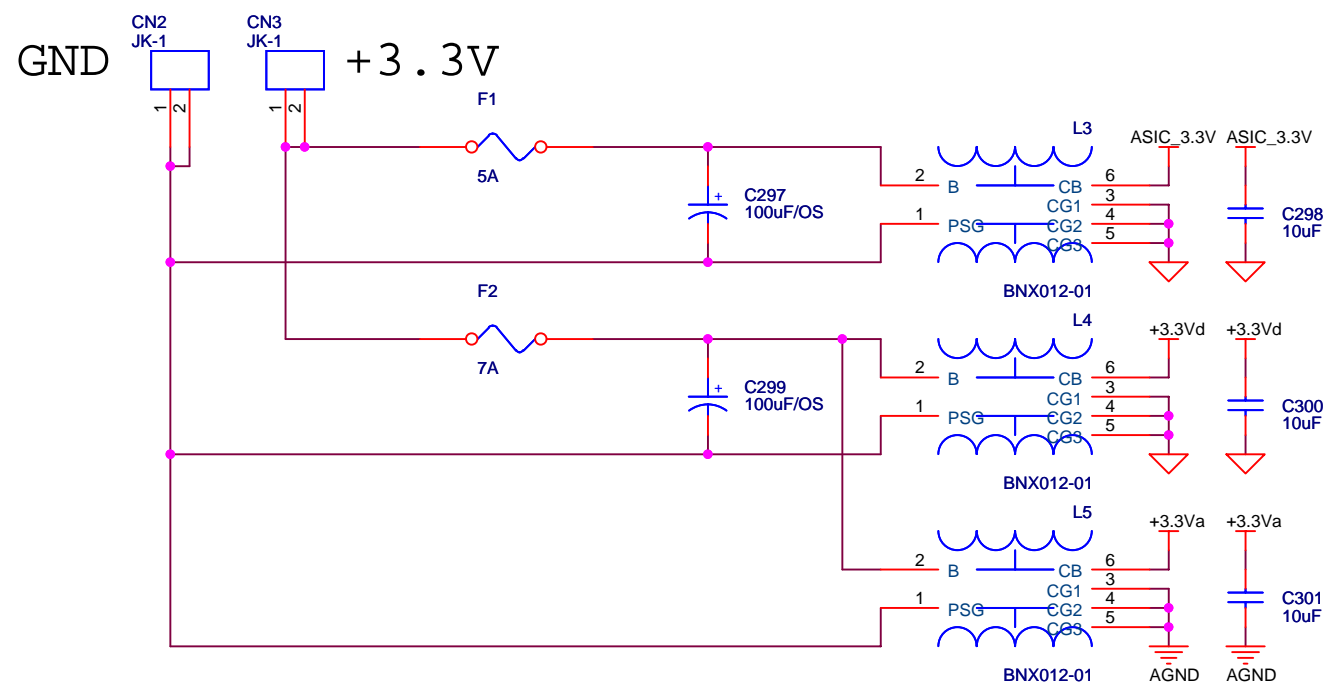




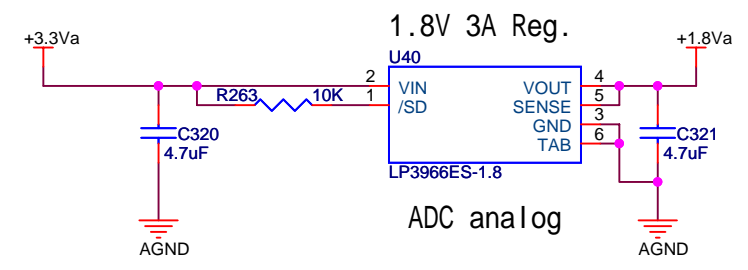
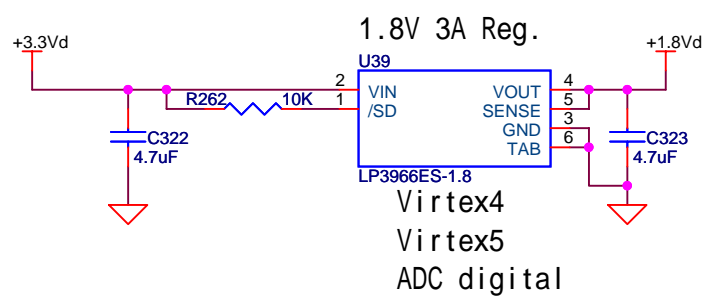
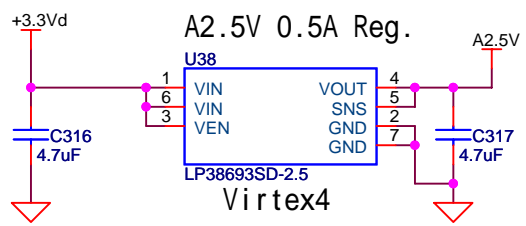
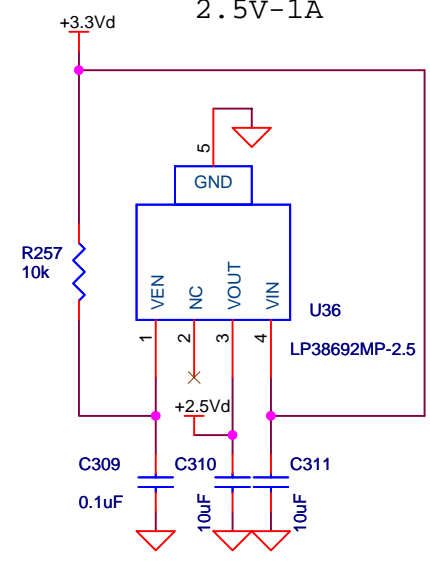
Title		
GbE EthernetPhy		
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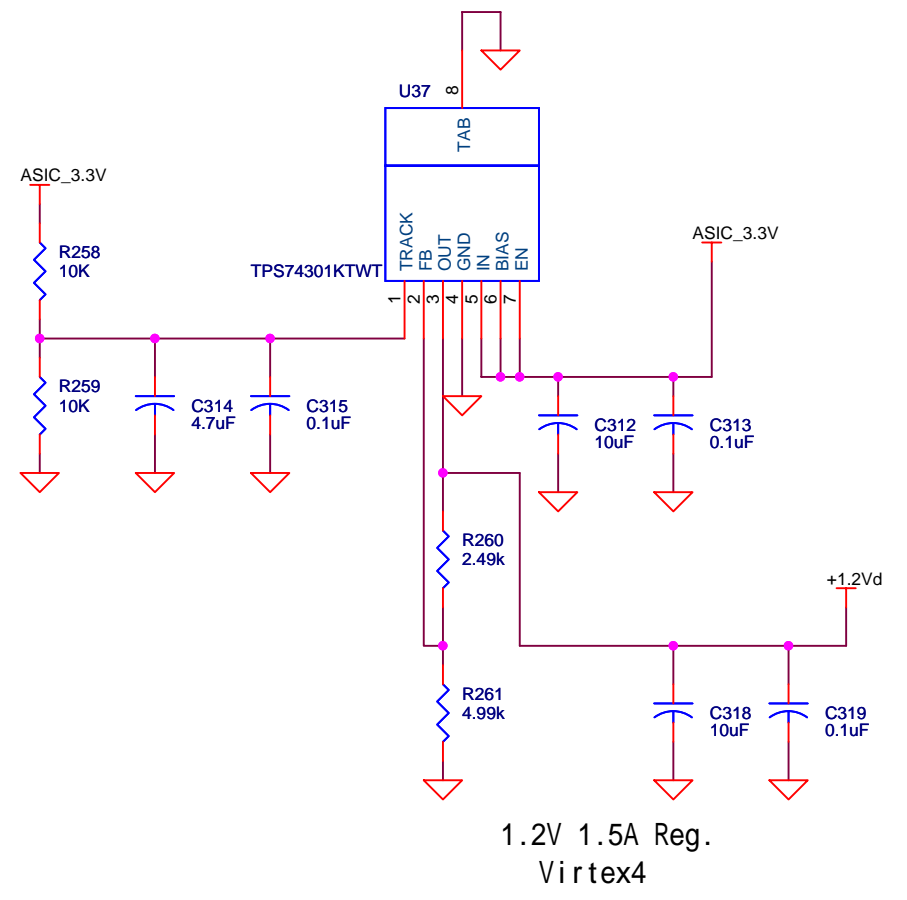
Title		
NIM_IO		
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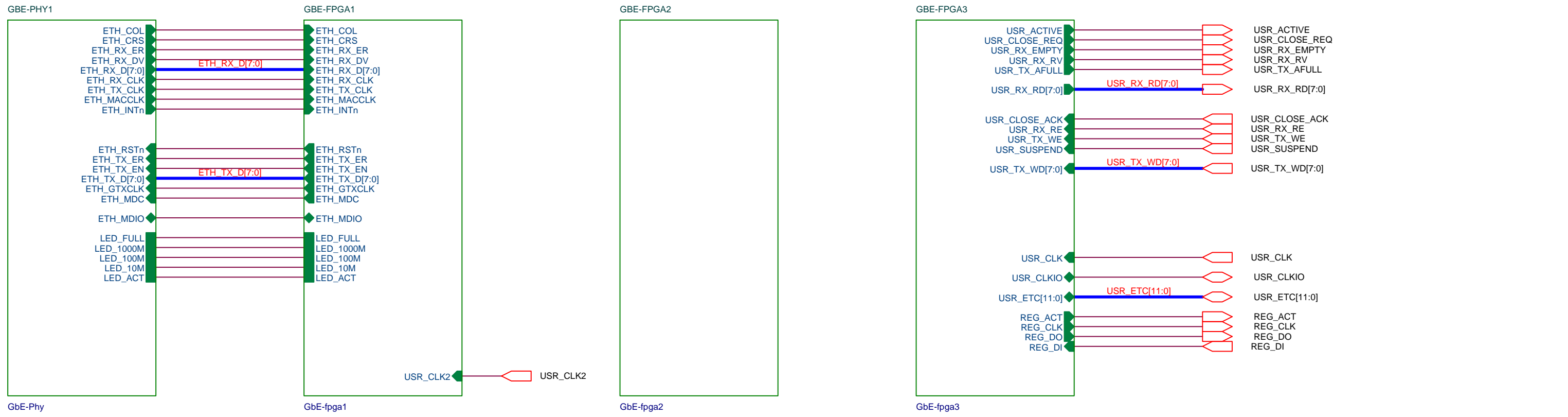


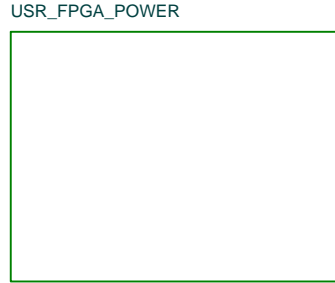
Virtex5
Virtex4
2.5V-1A



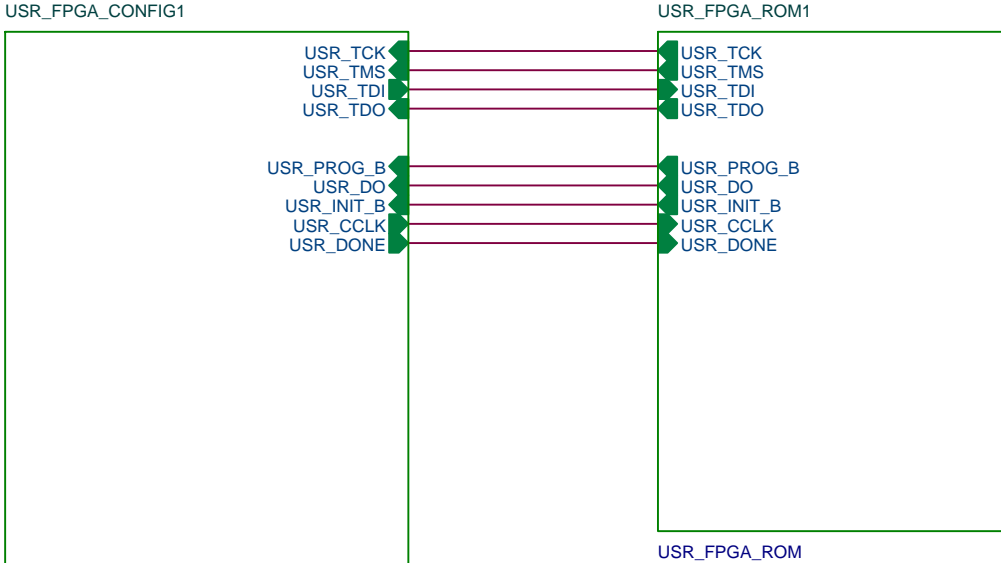
TABは放熱板です
必ず複数ビアで内層GNDへ落としてください。





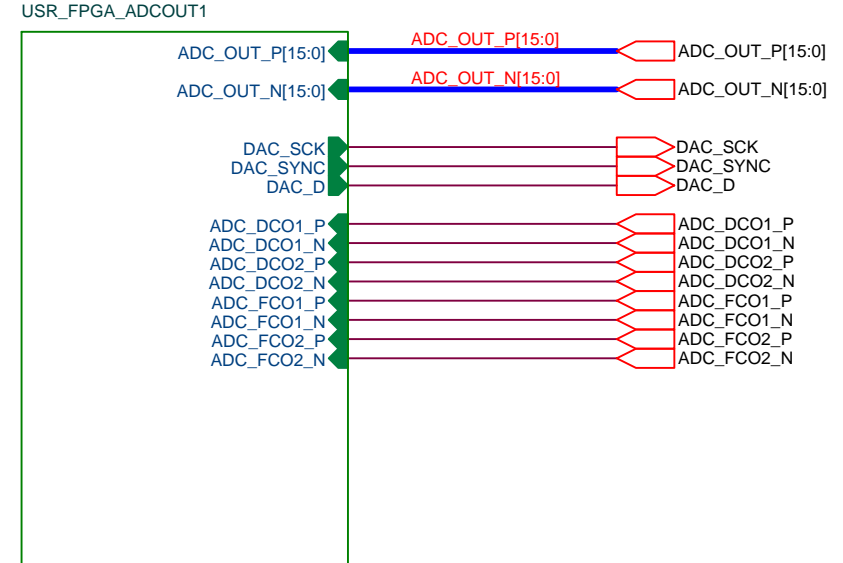


USR_FPGA_POWER

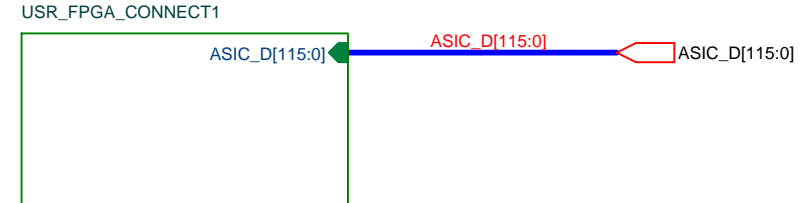


USR_FPGA_CONFIG1

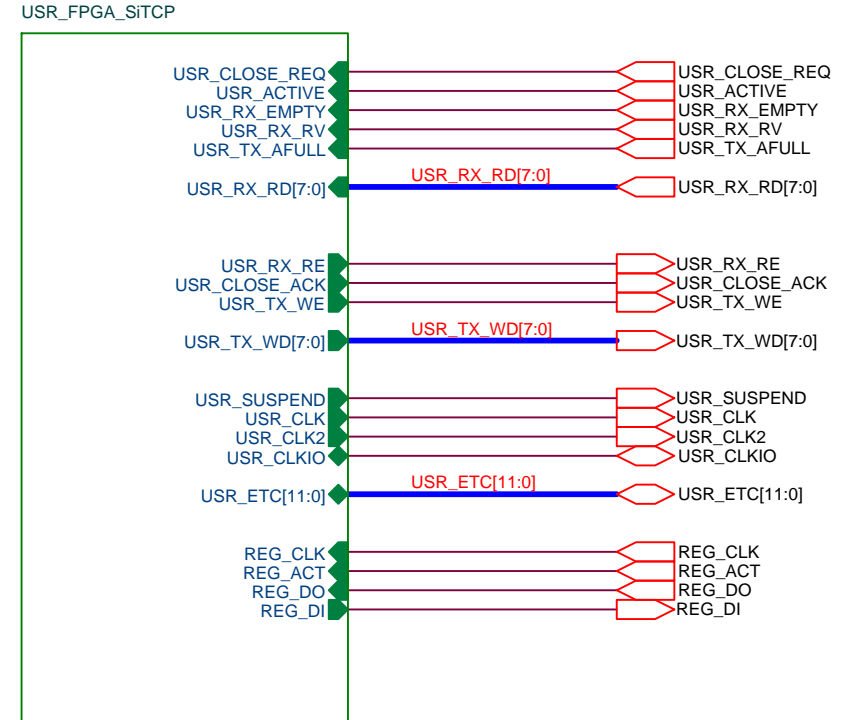
USR_FPGA_ROM



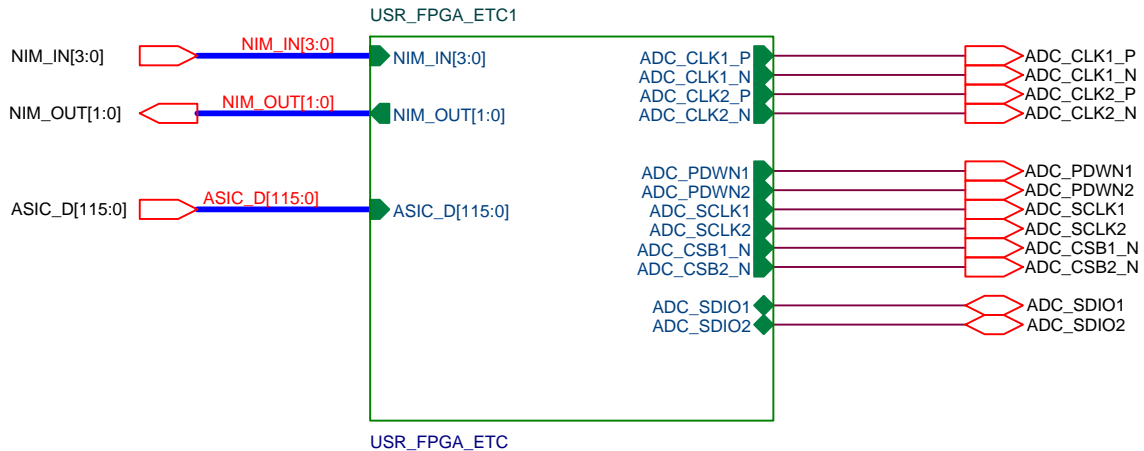
USR_FPGA_ADCOUT



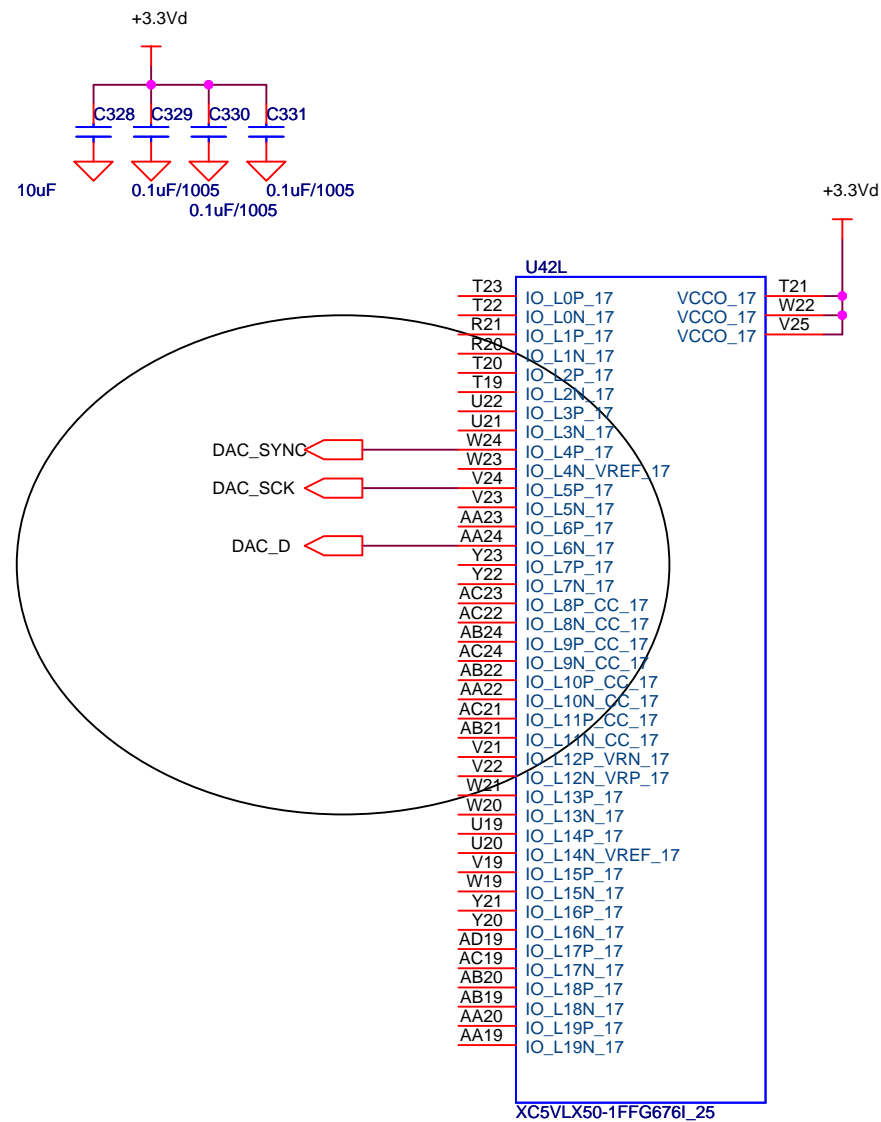
USR_FPGA_CONNECT



USR_FPGA_SITCP

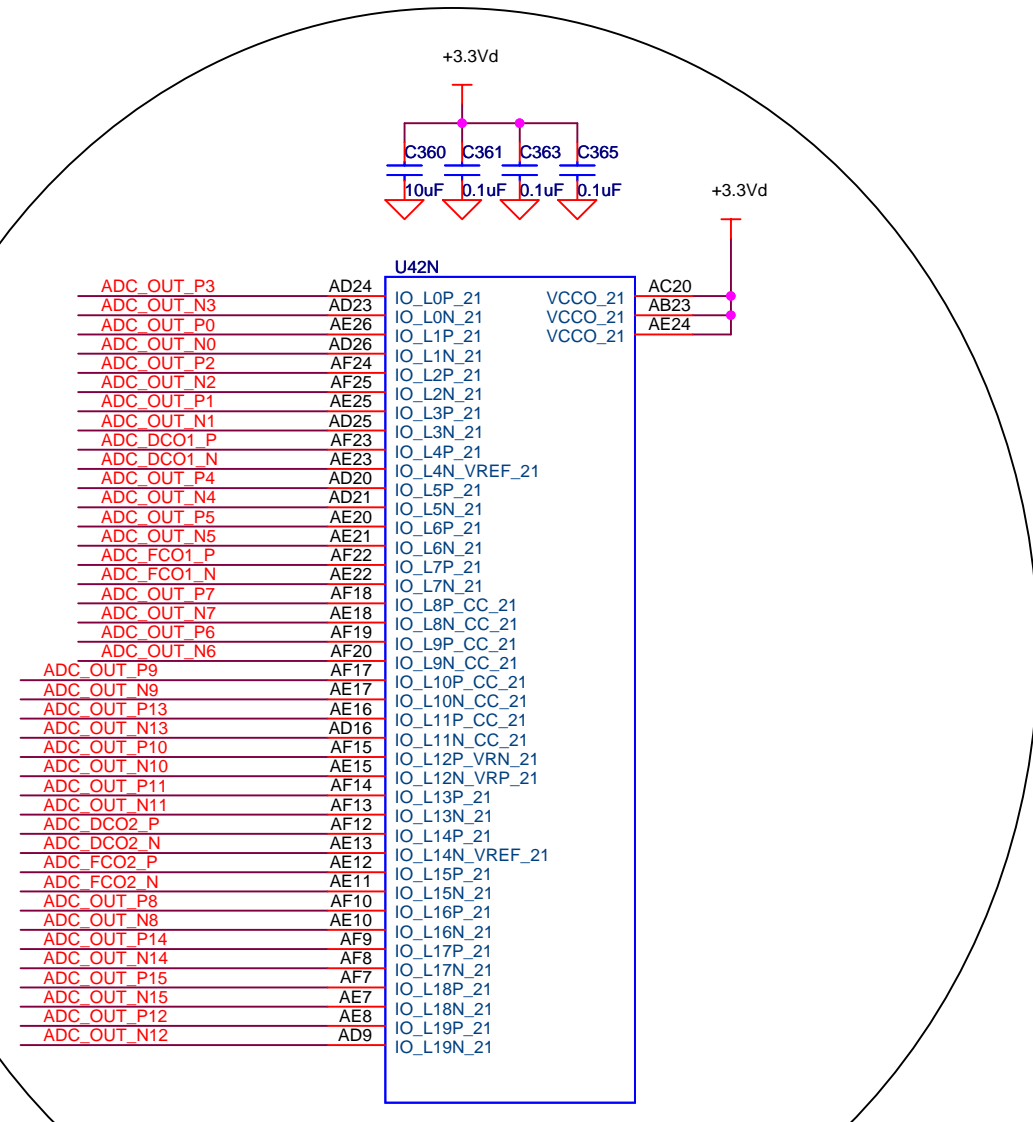
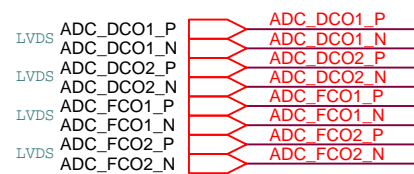


USR_FPGA_ETC



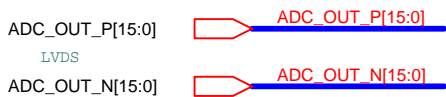
Pin	Signal	Pin	Signal	Pin	Signal
T23	IO_L0P_17	VCCO_17	T21		
T22	IO_L0N_17	VCCO_17	W22		
R21	IO_L1P_17	VCCO_17	V25		
R20	IO_L1N_17				
T20	IO_L2P_17				
T19	IO_L2N_17				
U22	IO_L3P_17				
U21	IO_L3N_17				
W24	IO_L4P_17				
W23	IO_L4N_VREF_17				
V24	IO_L5P_17				
V23	IO_L5N_17				
AA23	IO_L6P_17				
AA24	IO_L6N_17				
Y23	IO_L7P_17				
Y22	IO_L7N_17				
AC23	IO_L8P_CC_17				
AC22	IO_L8N_CC_17				
AB24	IO_L9P_CC_17				
AC24	IO_L9N_CC_17				
AB22	IO_L10P_CC_17				
AA22	IO_L10N_CC_17				
AC21	IO_L11P_CC_17				
AB21	IO_L11N_CC_17				
V21	IO_L12P_VRN_17				
V22	IO_L12N_VRP_17				
W21	IO_L13P_17				
W20	IO_L13N_17				
U19	IO_L14P_17				
U20	IO_L14N_VREF_17				
V19	IO_L15P_17				
W19	IO_L15N_17				
Y21	IO_L16P_17				
Y20	IO_L16N_17				
AD19	IO_L17P_17				
AC19	IO_L17N_17				
AB20	IO_L18P_17				
AB19	IO_L18N_17				
AA20	IO_L19P_17				
AA19	IO_L19N_17				

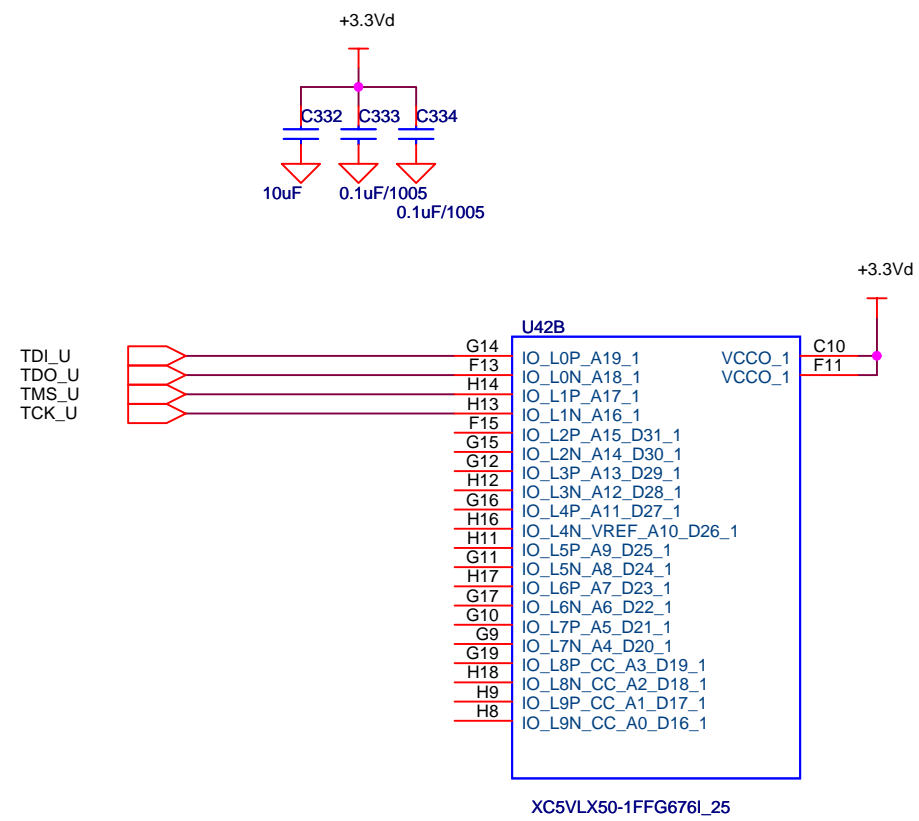
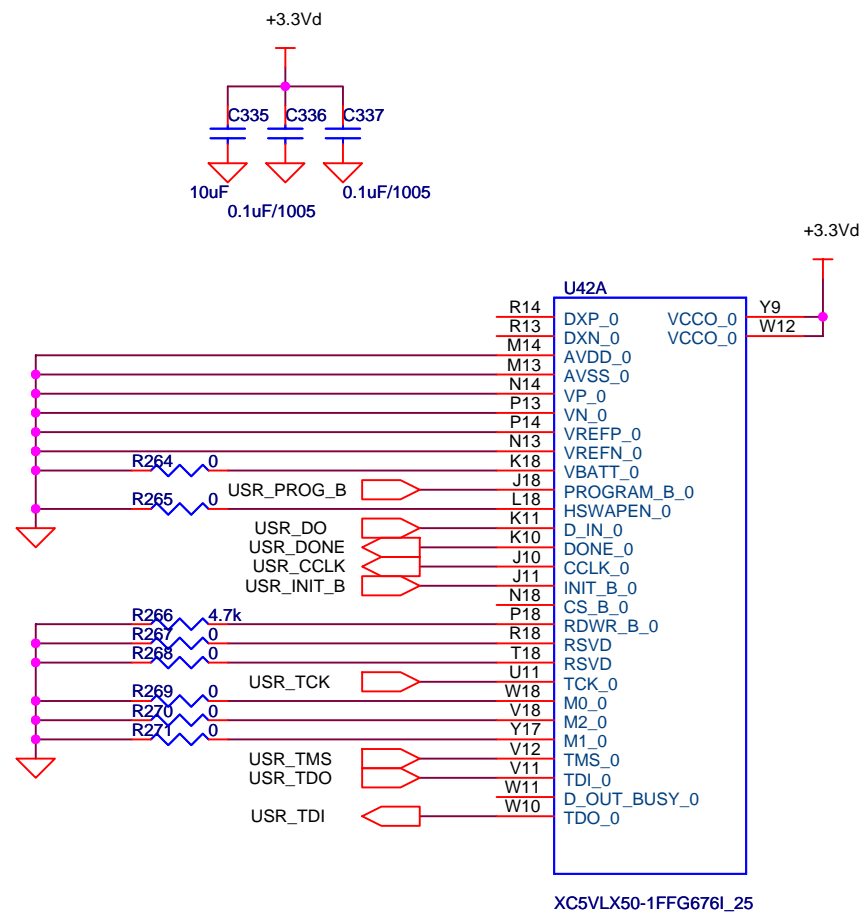
XC5VLX50-1FFG676I_25

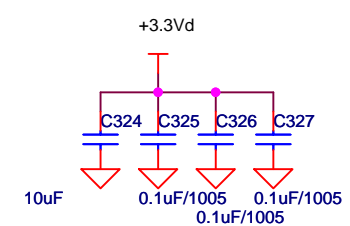
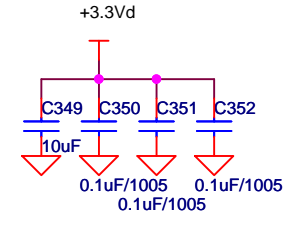
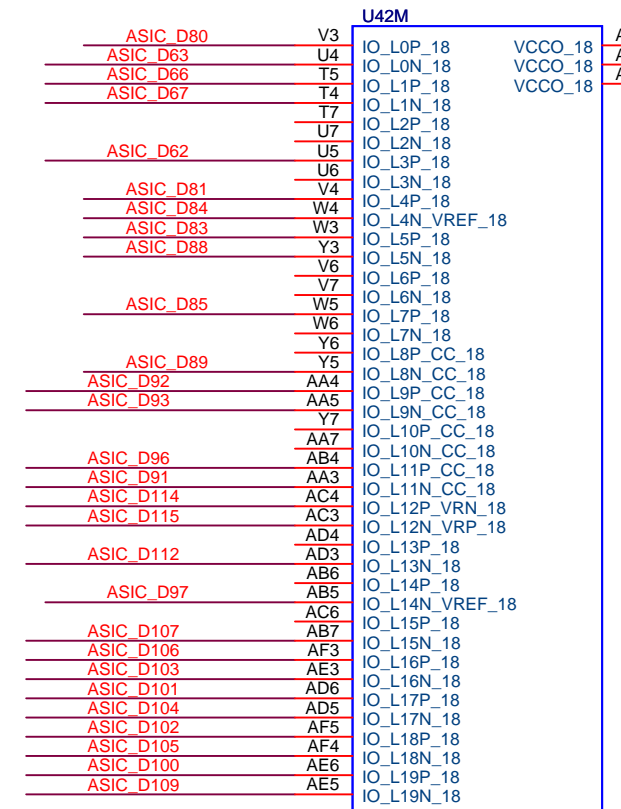
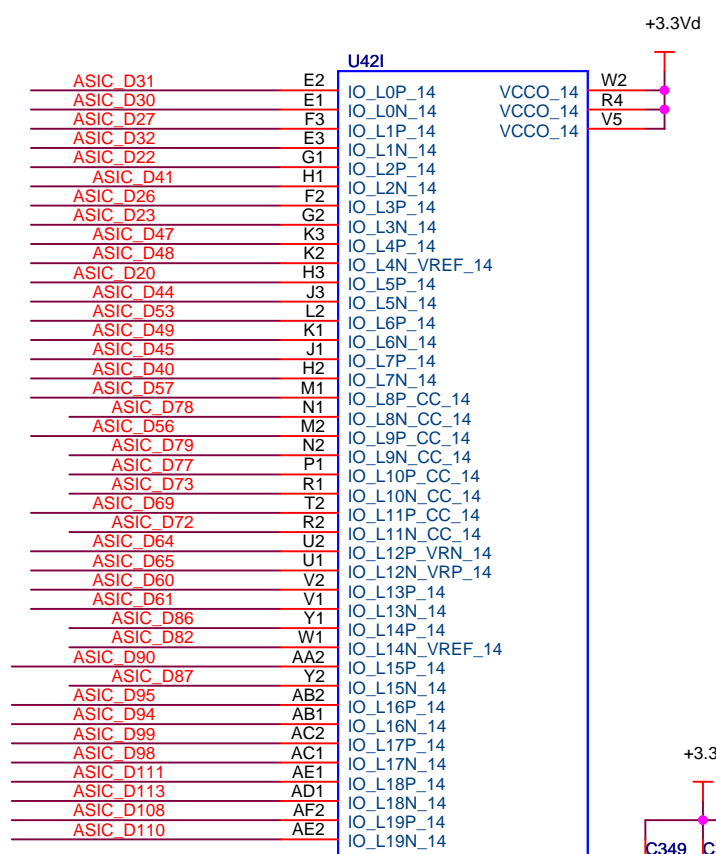
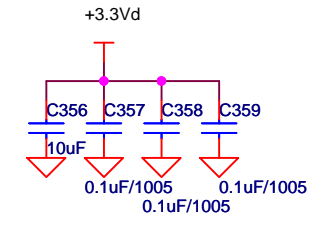
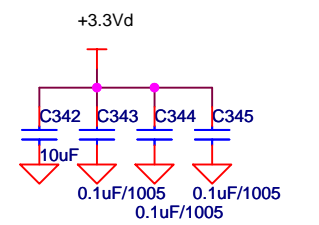
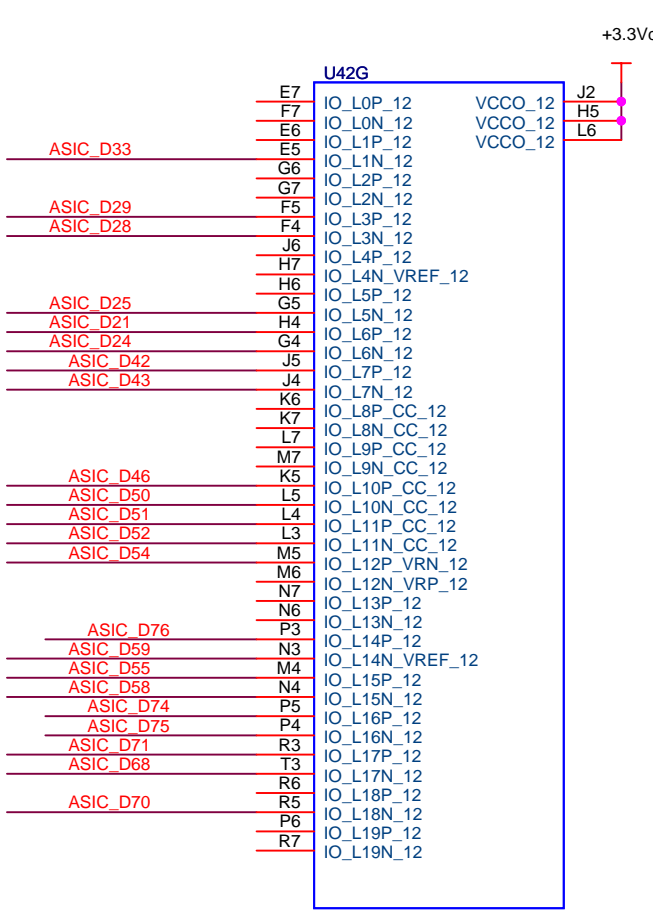
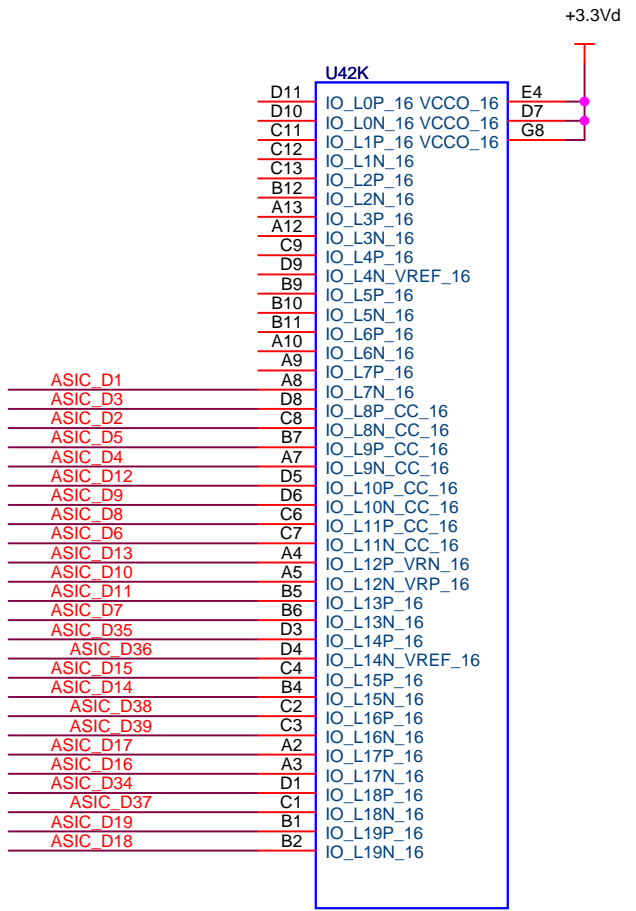


Pin	Signal	Pin	Signal	Pin	Signal
ADC_OUT_P3	AD24	IO_L0P_21	VCCO_21	AC20	
ADC_OUT_N3	AD23	IO_L0N_21	VCCO_21	AB23	
ADC_OUT_P0	AE26	IO_L1P_21	VCCO_21	AE24	
ADC_OUT_N0	AD26	IO_L1N_21			
ADC_OUT_P2	AF24	IO_L2P_21			
ADC_OUT_N2	AF25	IO_L2N_21			
ADC_OUT_P1	AE25	IO_L3P_21			
ADC_OUT_N1	AD25	IO_L3N_21			
ADC_DCO1_P	AF23	IO_L4P_21			
ADC_DCO1_N	AE23	IO_L4N_VREF_21			
ADC_OUT_P4	AD20	IO_L5P_21			
ADC_OUT_N4	AD21	IO_L5N_21			
ADC_OUT_P5	AE20	IO_L6P_21			
ADC_OUT_N5	AE21	IO_L6N_21			
ADC_FCO1_P	AF22	IO_L7P_21			
ADC_FCO1_N	AE22	IO_L7N_21			
ADC_OUT_P7	AF18	IO_L8P_CC_21			
ADC_OUT_N7	AE18	IO_L8N_CC_21			
ADC_OUT_P6	AF19	IO_L9P_CC_21			
ADC_OUT_N6	AF20	IO_L9N_CC_21			
ADC_OUT_P9	AF17	IO_L10P_CC_21			
ADC_OUT_N9	AE17	IO_L10N_CC_21			
ADC_OUT_P13	AE16	IO_L11P_CC_21			
ADC_OUT_N13	AD16	IO_L11N_CC_21			
ADC_OUT_P10	AF15	IO_L11N_CC_21			
ADC_OUT_N10	AE15	IO_L12P_VRN_21			
ADC_OUT_P11	AF14	IO_L12N_VRP_21			
ADC_OUT_N11	AF13	IO_L13P_21			
ADC_DCO2_P	AF12	IO_L13N_21			
ADC_DCO2_N	AE13	IO_L14P_21			
ADC_FCO2_P	AE12	IO_L14N_VREF_21			
ADC_FCO2_N	AE11	IO_L15P_21			
ADC_OUT_P8	AF10	IO_L15N_21			
ADC_OUT_N8	AE10	IO_L16P_21			
ADC_OUT_P14	AF9	IO_L16N_21			
ADC_OUT_N14	AF8	IO_L17P_21			
ADC_OUT_P15	AF7	IO_L17N_21			
ADC_OUT_N15	AE7	IO_L18P_21			
ADC_OUT_P12	AE8	IO_L18N_21			
ADC_OUT_N12	AD9	IO_L19P_21			
		IO_L19N_21			

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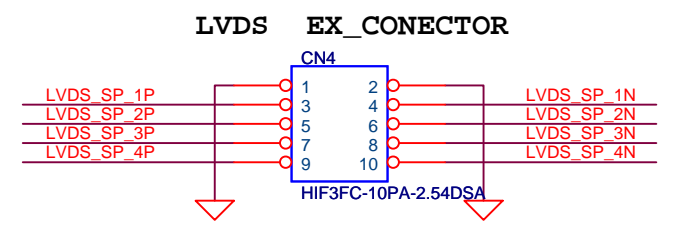
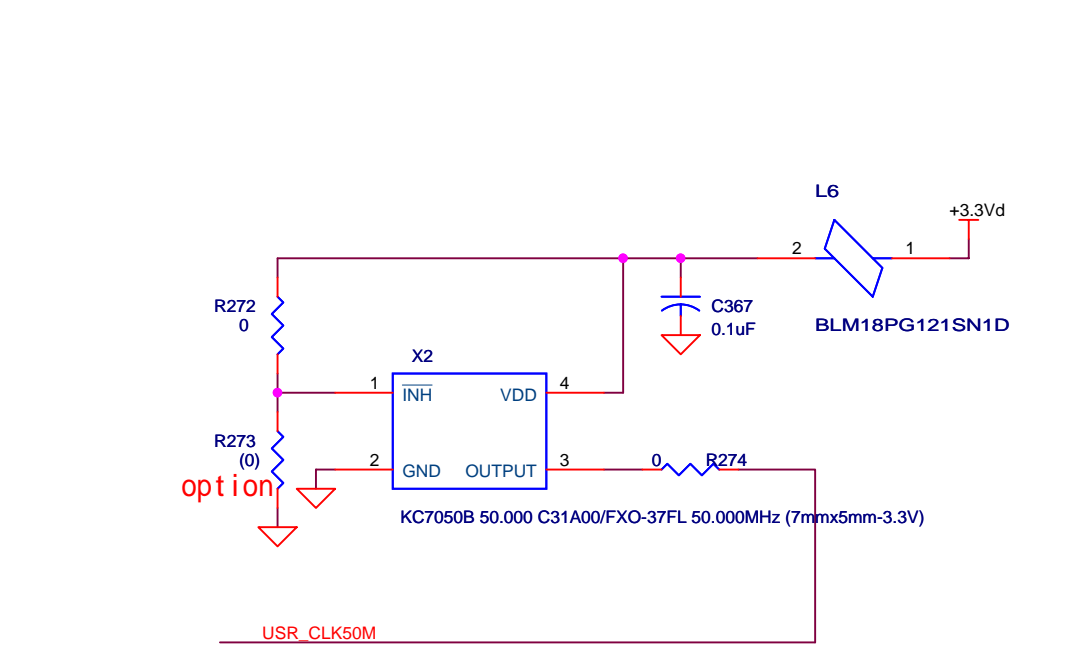
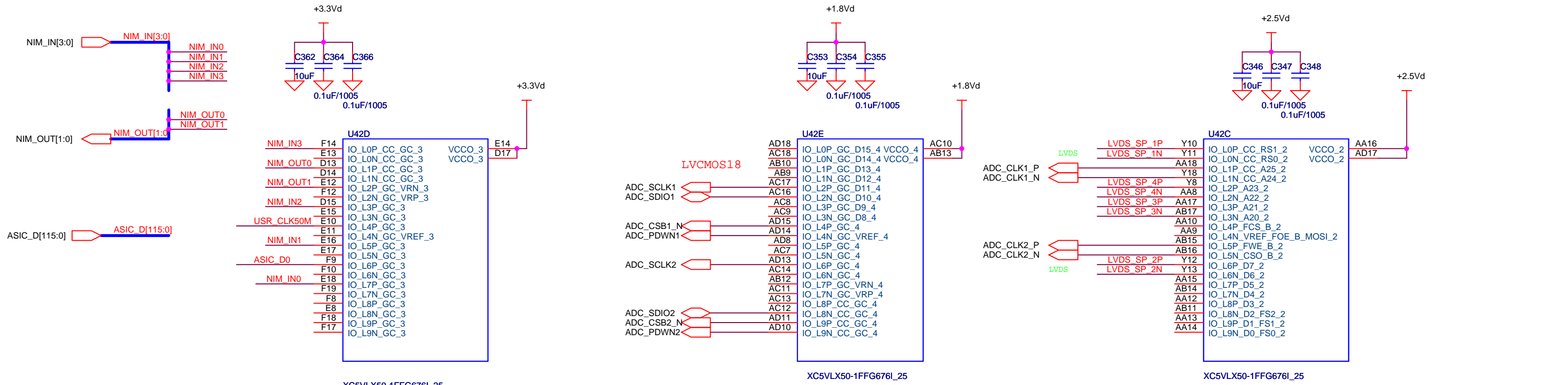


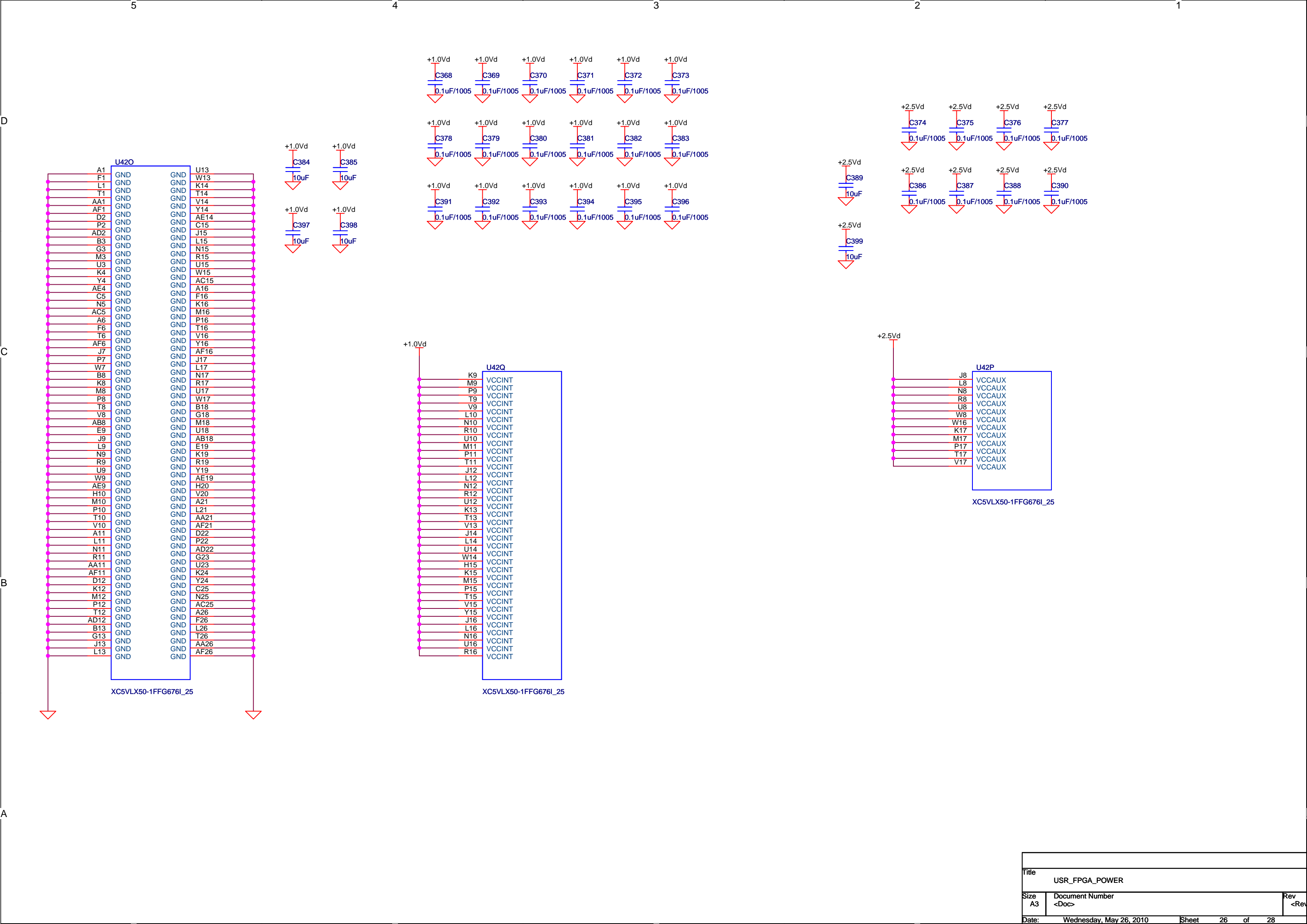




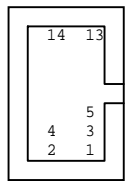
ASIC_D[115:0] ASIC_D[115:0]

Title		
USR_FPGA_CONNECT		
Size	Document Number	Rev
A3	<Doc>	<RevC>
Date:	Wednesday, May 26, 2010	Sheet 24 of 28

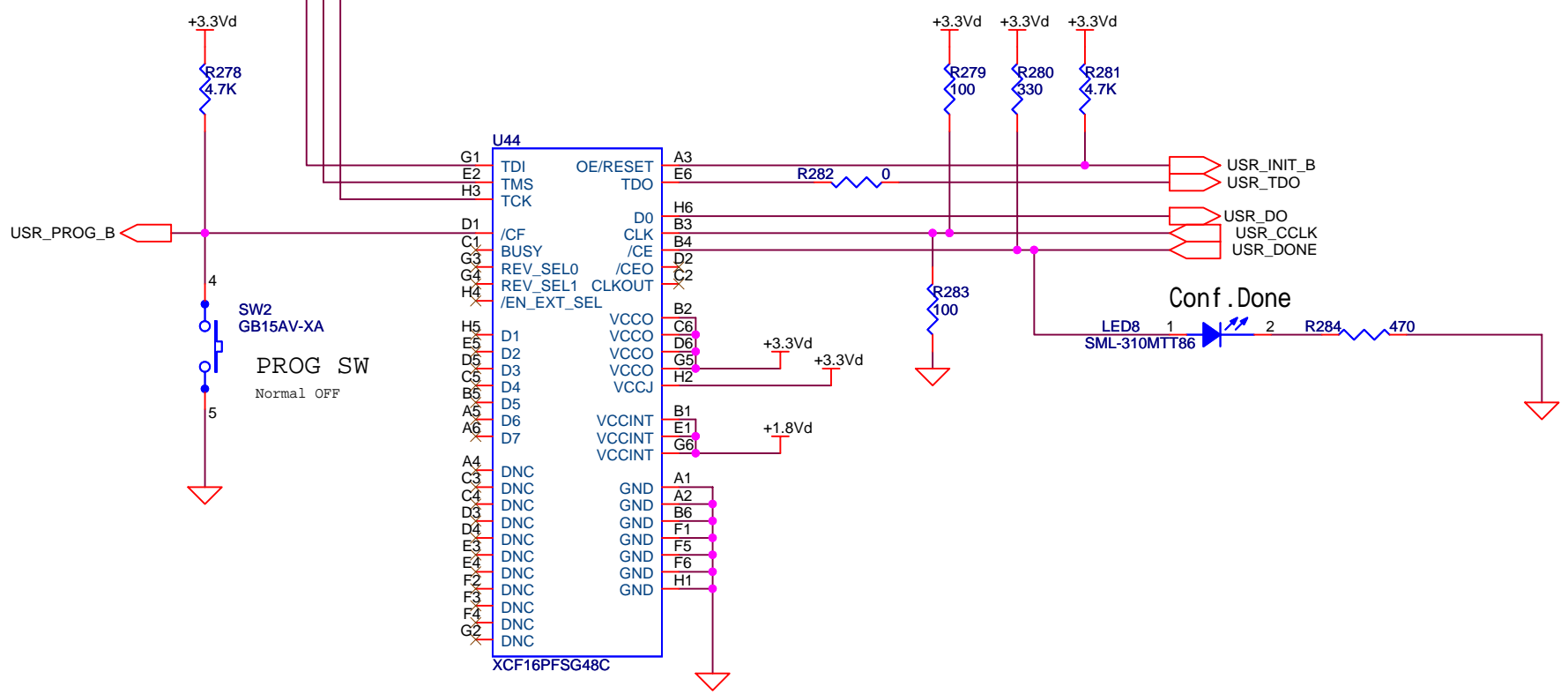
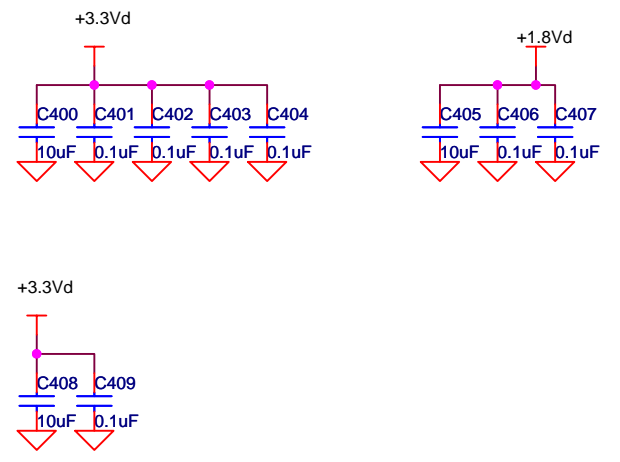
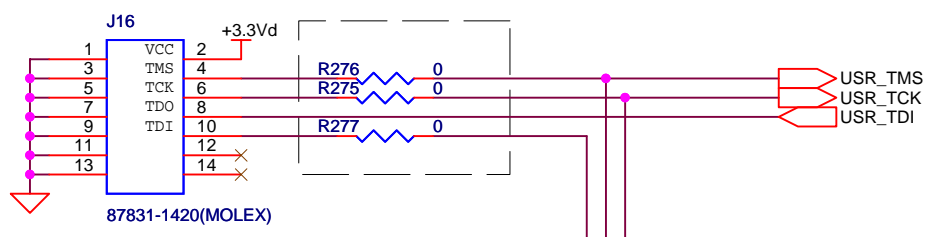




Top View

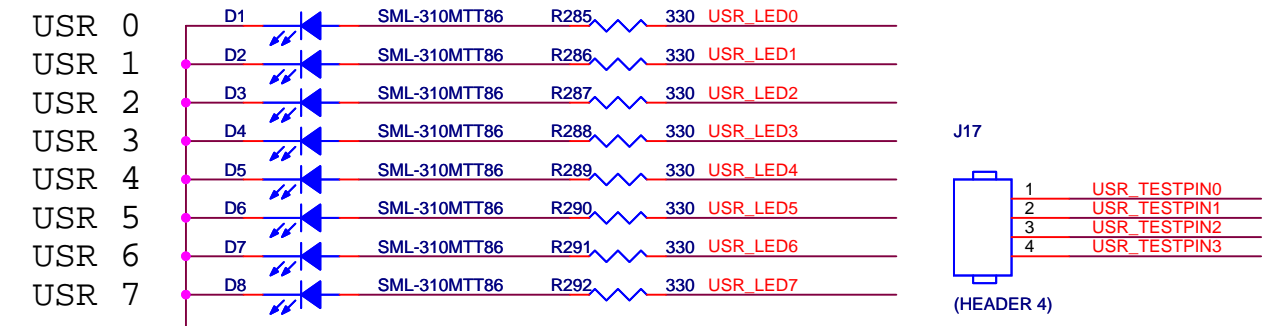


コネクタの近くに置く



Title		
USR_FPGA_ROM		
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表面実装LED



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穴だけ 基板の下の方に

