TMC

TMC1004 32-Channel CAMAC Multi-Hit TDC

Module Manual

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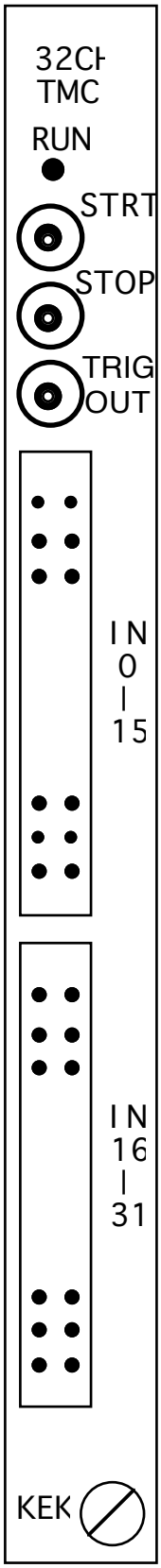
TMC1004 32-Channel Multi- Hit TDC Module



- 32 channels in single-w idth module
- 1ns / bit least count, σ= 0.52 ns time resoluti on
- 1024 bits / channel (or 2kbit / 2 ch, or 4kbit/ 4ch)
- Common stop or Common start operation
- No clear/dizitization t ime needed
- Rising edge detection a nd 6 bit encoded data output for each 32 ns data, or raw data dump for full d ata
- Very stable for tempera ture, voltage variation
- Q stop block transfer r eadout for encoded data
- ECL differential input for signal
- NIM level start / stop signal input
- NIM level trigger outpu t for test purpose

Specifications

Signal Inputs :	32 Channel. ECL-differential. Input Impedance 100 Ω. Two 40-pin Flat Cable Connector. Input signal is stretched to about 32 ns internally if the width is less than 32 ns.
START Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Start mode.
STOP Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Stop mode.
TRIGGER Output :	Lemo-type connector; NIM level. Generate synchronous output pulse with internal clock when started. Used for test purpose.
Least Time Count :	1 ns/bit
Time Range :	1.024 μs (4 ch), 2.048 μs (2 ch) or 4.096 μs (1 ch)
Double Hit Resolution :	32 ns
Timing Measurement Error :	σ = 0.52 ns (including digitization error)
Integral Linearity Error :	< 1.5 bit
Differential Linearity :	< 0.2 ns
Variation of Slope : (time-to-digital conversion factor)	< 0.1 % (2.6 - 3.4 V) < 0.1 % (15 - 55 ˚C) < 0.1 % (chip to chip)
Channel to Channel Discontinuity:	< 0.5 bit
Data Readout :	Fast readout is done through encoded data readout (6 bit/ch) by F(0). The row which is read out is pointed by the Read Pointer (CSR1). For debugging and other purpose which requires entire data, Serial I/O mode through CSR0 can be used. This mode read out entire data of the TMC chip, but takes much longer readout time.
Data :	The proper CAMAC address and F(1) gates the 4 channel data of a TMC chip onto the R(1) to R(24). A(0) through A(7) are used for chip number.

	R24	R18	R12	R6	R1
Chip 0 : A(0)	Ch 3	Ch 2	Ch 1	Ch 0	
Chip 1 : A(1)	Ch 7	Ch 6	Ch 5	Ch 4	
	:	:	:	:	
Chip 7 : A(7)	Ch 31	Ch 30	Ch 29	Ch 28	

CAMAC Commands :	Z or C : All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". X : An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.

CAMAC Function Code :	F(0) : Read Data; requires N and A. A(0) through A(7) are used for chip address. F(1) : Read CSR0 register; requires N and A. A(0) through A(7) are used for chip address. F(4) : Read CSR1 (Read Pointer) register; requires N and A. A(0) through A(7) are used for chip address. F(6) : Read CSR2 (Write Pointer) register; requires N and A. A(0) through A(7) are used for chip address. F(9) : Reset. Reset all CSR registers and internal circuit. F(17) : Write CSR0 register; requires N and A. A(0) through A(7) are used for chip address. F(20) : Write CSR1 (Read Pointer) register; requires N and A. A(0) through A(7) are used for chip address. F(22) : Write CSR2 (Write Pointer) register; requires N and A. A(0) through A(7) are used for chip address. F(25) : Start signal recording. Used in common start mode. Functions as same as the START input, but F(25) starts signal recording with synchronous to the internal clock.
Packaging :	CAMAC 1 width module.
Power Requirement :	+6 V at 1.2 A, -6V at 0.5 A.

Settings

There are several switches and jumpers in the module. User should set up these settings correctly. The meaning of each switches and jumpers are described below.

SW1, SW2, and SW3 : Common Stop / Common Start selection switches. These switches select Common Stop or Common Start mode in accordance with measurement style. All these switches must be same position as indicated in PC board, otherwise the circuit does not work correctly.

SW4 : Stop Counter value (default = 32). Used in common start mode; selectable between 0 to 255. In Common Start mode, input signal is written to TMC's after receiving "START" signal or F(25) command. The operation will stop after passing the period defined in this switch. The period is selected from a multiple of 32 ns. The bit where switch is off has value "1". If you set the period longer than the depth of the channel, first part of the data and the start mark will be lost naturally. Ex) If the position "1", "2", and "4" is off and others are on, the period will be 32 ns x 7 = 224 ns.

CONF0, CONF1 : Configuration select pin (default = 0). Each chip has these jumper pins, so there are 8 sets of jumpers. They select depth of a channel in each chip.

CONF	CONF0	CONF1	Depth	Channel/chip
0	close	close	1 k bit	4 channels
1	open	close	2 k bit	2 Channels. Ch0 and 1, Ch2 and 3 are connected together. Each channel needs same signal in inputs.
2	close	open	4 k bit	1 Channels. Ch0, 1, 2 and 3are connected together. Each channel needs same signal in input.

OVWRP : Always open.

Input Connector Pin Assignment

Upper Connector

Pin No.	Assignment	Pin No.	Assignment
1	no connection	2	no connection
3	Ch 0 +	4	Ch 0 -
5	Ch 1 +	6	Ch 1 -
7	Ch 2 +	8	Ch 2 -
9	Ch 3 +	10	Ch 3 -
11	Ch 4 +	12	Ch 4 -
13	Ch 5 +	14	Ch 5 -
15	Ch 6 +	16	Ch 6 -
17	Ch 7 +	18	Ch 7 -
19	Ch 8 +	20	Ch 8 -
21	Ch 9 +	22	Ch 9 -
23	Ch 10 +	24	Ch 10 -
25	Ch 11 +	26	Ch 11 -
27	Ch 12 +	28	Ch 12 -
29	Ch 13 +	30	Ch 13 -
31	Ch 14 +	32	Ch 14 -
33	Ch 15 +	34	Ch 15 -
35	no connection	36	no connection
37	no connection	38	no connection
39	no connection	40	no connection

Lower Connector

Pin No.	Assignment	Pin No.	Assignment
1	no connection	2	no connection
3	Ch 16 +	4	Ch 16 -
5	Ch 17 +	6	Ch 17 -
7	Ch 18 +	8	Ch 18 -
9	Ch 19 +	10	Ch 19 -
11	Ch 20 +	12	Ch 20 -
13	Ch 21 +	14	Ch 21 -
15	Ch 22 +	16	Ch 22 -
17	Ch 23 +	18	Ch 23 -
19	Ch 24 +	20	Ch 24 -
21	Ch 25 +	22	Ch 25 -
23	Ch 26 +	24	Ch 26 -
25	Ch 27 +	26	Ch 27 -
27	Ch 28 +	28	Ch 28 -
29	Ch 29 +	30	Ch 29 -
31	Ch 30 +	32	Ch 30 -
33	Ch 31 +	34	Ch 31 -
35	no connection	36	no connection
37	no connection	38	no connection
39	no connection	40	no connection

General Description

The TMC 32-Ch CAMAC module was designed to evaluate the newly developed TMC1004 chip which is a low-power and high-resolution Multi-hit Time-to-Digital Converter chip. The TMC chip is developed for readout of a drift chamber in high-rate experiment such as the SSC.

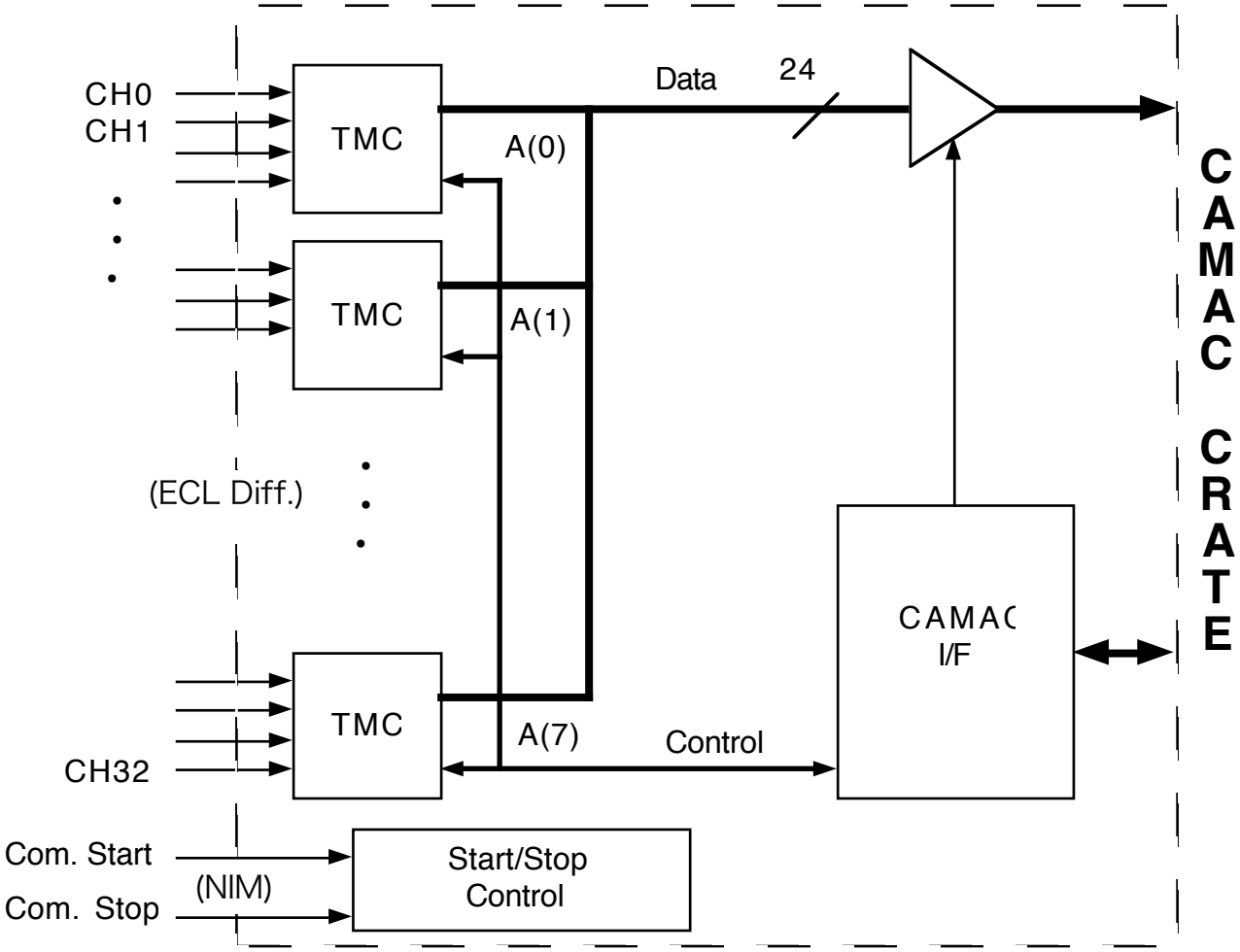
The chip has special kind of memories which record input pulses in 1 ns time resolution. TMC1004 chip has 4 channels of circuit and each channel has 1024 bits of memories. Thus each channel records signal of 1 μsec period. The chip also can be configured to 2 channels times 2 k bits or 1 channel times 4 k bits.

The TMC 32-Ch CAMAC module consists of 8 TMC1004 chips, so it has 32 input channel. Although the TMC1004 is designed for deadtime-less readout, this CAMAC module can not operate as deadtime-less because the CAMAC cycle is very slow comparing with the input data bandwidth. The module runs in "Common Stop" or "Common Start" mode which is selectable by internal switches.

Detailed explanation of the CAMAC circuit is also found in reference 1.

CAMAC Module Circuit Description

Figure 1 shows the block diagram of the TMC 32-channel CAMAC module. The module contains 8 TMC chips, thus the 4 channels are grouped and most of the operations are applied to one of eight chips. These eight chips are accesses by using subaddress A(0) through A(7). Four channel data are read out at once as the format shown in Fig. 1. Each chip has three CSR registers. The contents of the registers are shown in Table 1.



[Data Format]

23 18	17 12	11 6	5 0
CH3 data	CH2 data	CH1 data	CH0 data

F(0) • A(0-7) : Read Data
F(1) • A(0-7) : Read CSR0
F(4) • A(0-7) : Read CSR1
F(6) • A(0-7) : Read CSR2
F(17) • A(0-7) : Write CSR0
F(20) • A(0-7) : Write CSR1
F(22) • A(0-7) : Write CSR2
F(9) : Reset
F(25) : Start

Fig.1 Block Diagram of the TMC 32-Channel CAMAC module

Table 1 CSR Registers

bit	6	5	4	3	2	1	0
CSR0	-	MOD1	MOD0	SIO3	SIO2	SIO1	SIO0
CSR1	Read Pointer Value [RP]						
CSR2	Write Pointer Value [WP]						

* CSR0 (= 0 after reset [read/write])
  - SIO3 ~ 0 : Serial I/O bits. These bits are valid only in the serial i/o mode. One bit data for each channel is read/written through these bits from/to the address pointed by the read counter(row position) and the write counter(column position).
  - MOD0,1 : MODE = [MOD1,MOD0].

    * MODE = 0 (Stand alone Mode) : Usually this mode is used. Data are read out from the row pointed by the Read Pointer.
    (Caution: If the data recording is in progress, the Read Pointer will also be counted up with the Write Pointer.)

    * MODE = 1 (Slave Mode) : Not use.

    * MODE = 2 (Serial I/O Mode) : This mode is used mainly for testing each bit in the memory. Data are read/write from/to the address pointed by the CSR1(row address) and CSR2(column address) through bit 0 ~ 3 in the CSR0. Bit 0 corresponds to the data in the CH0 and bit 1 corresponds to CH1 and so on.

* CSR1 (= 2 after reset [read/write])
  - RP : Read Pointer Value. The contents of the read counter are set through this register. The value read back indicates present value of the read counter. The counter is incremented by the system clock (31.25 MHz) during data recording. This register also works as a row address register in the Serial I/O mode.

* CSR2 (= 0 after reset [read/write])
  - WP : Write Pointer Value. The contents of the write counter are set through this register. Present value of the write counter is read back. The counter is incremented by the system clock (31.25 MHz) during data recording. This register also works as a column address register in the Serial I/O mode.

Data Format and Conversion

Since the TMC1004 chip is designed for high-rate application, the time recording is continuous and does not have any timing reference point inherently. However, for usual application, we need a start time or a stop time information. In this CAMAC module, these timing are recorded in TMC in addition to the input signal timing. Start or Stop timing is recorded in the first or the last 2 columns as shown in Table 2. In common start mode, input multiplexer will change inputs from start signal to input signal at third row (N+2). In common stop mode, input multiplexer will change inputs from input signal to stop signal when reciving stop pulse (M-3), and record the stop pulse which is delayed internally in row M-2 and M-1. Start/Stop pulse has about 12 ns width, and can be discriminated from input signal which has more than 32 ns pulse width.

Table 2. Raw data map of the TMC chip for Common Start/Stop mode

[Common Start Mode]

Start pulse recording area	Row N
Start pulse recording area	Row N+1
... Input signal recording area	Row N+2
Input signal recording area	Row N+3
:	:
Input signal recording area	Row N+31

(N = Initial Value of the Write Pointer.)

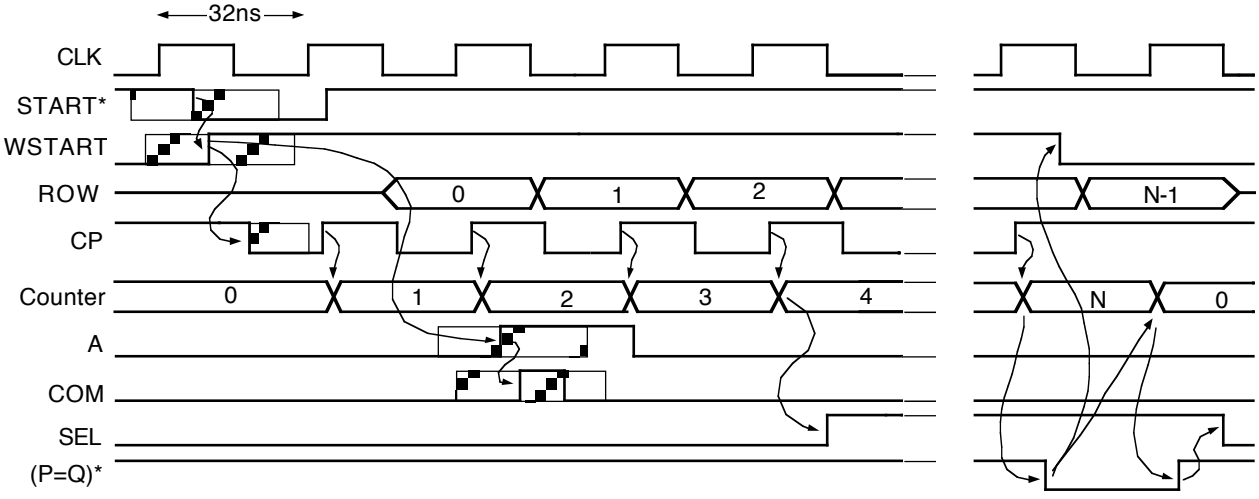
[Common Stop Mode]

Input signal recording area	Row M-32
Input signal recording area	Row M-31
:	:
Input signal recording area ...	Row M-3
Stop pulse recording area	Row M-2
Stop pulse recording area	Row M-1

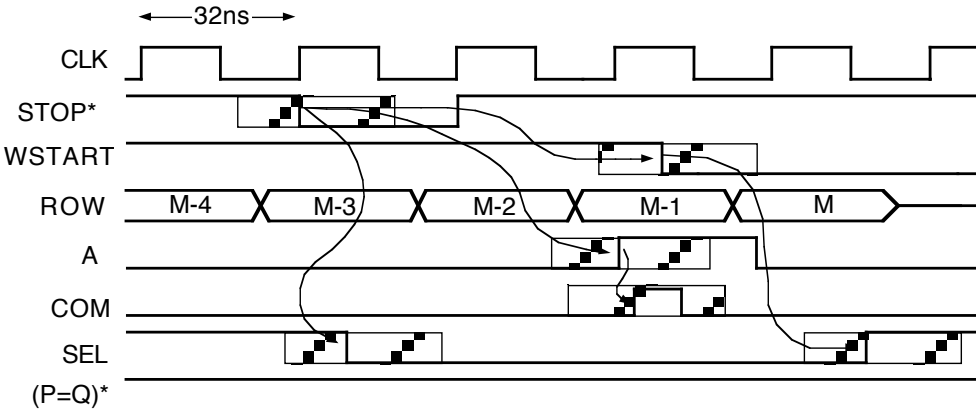
(M = Final Value of the Write Pointer.)

Fig. 2 Timing for (a) common start,, and (b) common stop mode.

(a) Common START Mode



(b) Common STOP Mode



Each Row data (32 bits) is encoded to 6 bit as shown in Table 3. The most significant bit shows the value of the first bit of a row, and the remaining 5 bits show the position of the "0" to first "1" transition.

Table 3 Data Encoding Schme

Bit Pattern of inside TMC	Encoded Data
<------- Time 3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	5* 4 3 2
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0	0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0	0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0	0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0 0 0	0 0 0 1
:	:
:	:
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0
(not appear)	1 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 1	1 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x 1	1 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x x 1	1 0 0 1
:	:
:	:
1 0 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1	1 1 1 1

(*) Bit 5 of the encoded data is used for distinguish the transition between row.

An example of data taking and conversion flow is shown below. The common stop mode and CONF=0 are assumed in the example.

TMC Chip Circuit Description

The idea of Time Memory Cell (TMC) was proposed by us and tested by making a TEG chip[2]. The cell utilizes low-power and high-density characteristics of a CMOS memory cell and gate delay time. Figure 2 shows the basic operation of the TMC. As the write signal (WL) timing in each TMC cell is delayed by 1 ns, timing information of the input lines (TIN and TIN*) is recorded to memory cells sequentially. To keep the delay time constant, the delay time of the delay element is controlled through the Vg line by a feedback circuit which refers to an external system clock period.

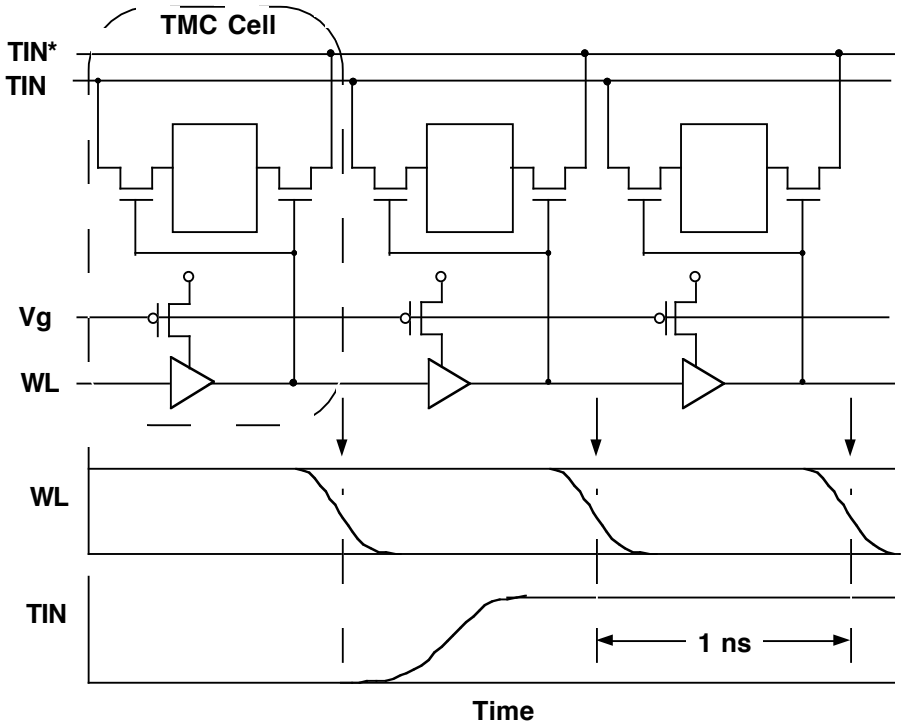


Fig.2 Input signal write operation in the TMC cells.

The TMC1004 has been developed using an 0.8 μm CMOS process. It contains 4 channels and each channel has 1024 TMC cells (32 rows and 32 columns). The chip achieves more than 10 times the density of a 1 GHz GaAs shift register while dissipating less than 1/100 of the power.

The schematic of the TMC cell is shown in Fig. 3. Each cell has one timing-information write port (TIN and TIN*) and one data-read/write port (BL and BL*). Two PMOS transistors (M1 and M2) are added to the previous design[1] to ease write operation by cutting the F/F paths in the cell. Transistor parameters of the delay element were selected to obtain a gate delay time close to 1 ns/bit. To get high precision and consistency between rows a feedback circuit adjust the total delay of the 32 cells in a row to be 32 ± 0.5 ns.

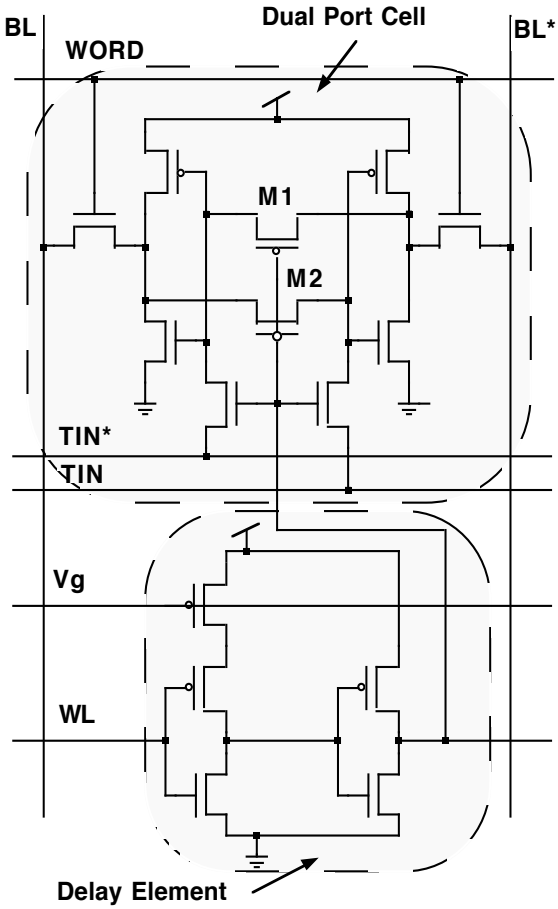


Fig.3. TMC cell circuit.

Figure 4 shows the schematic of the feedback circuit. When an external clock (ϕ_1) sets two flip-flops (F1 and F2) at the falling edge, capacitors C1 and C2 begin to charge. The charging of C1 is stopped by the falling edge of the pulse at the end of the delay line. The charging of C2 stops at the next falling edge of the clock pulse (ϕ_2). Hence, the voltage difference between C1 and C2 is proportional to the time difference between the delay line and clock period. If the delay time is less than the clock period, C3 charges during a store period increasing the delay of the delay line. If the delay time is longer than the one clock period, C3 discharges reducing the delay.

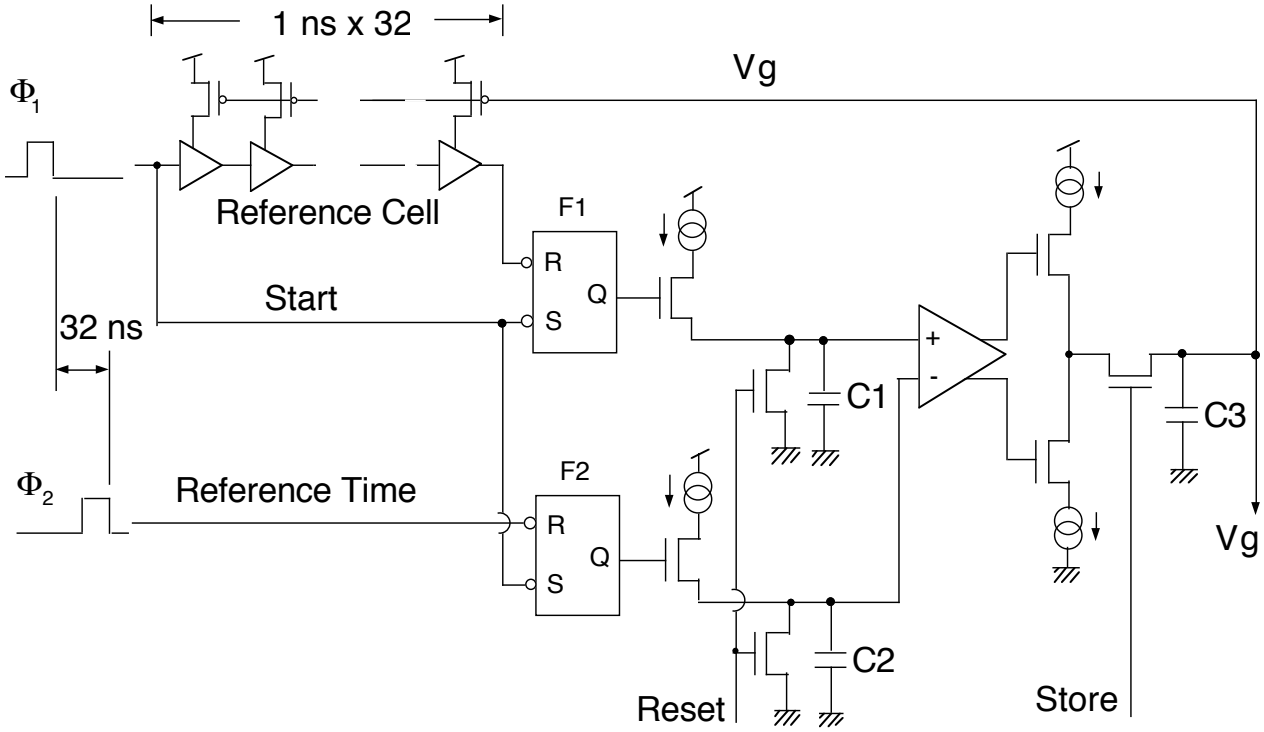


Fig.4. Feedback circuit.

The Block diagram of the TMC1004 is shown in Fig. 5. The chip has four TMC arrays, each with 32 rows by 32 columns of TMC cells. For accessing the four arrays, there are two pointers (Write and Read) each of which consists of 7 bit counter and decoder. The write pointer is incremented in each clock (CLK) cycle which initiates a pulse in the delay line of the designated row. The read pointer selects a row for readout and is incremented by the same clock (CLK). This scheme with two pointers and dual port cells enables read and write operations to proceed simultaneously. The four TMC arrays can be configured as 1, 2, or 4 channels by setting external pins. The 1, 2, and 4 channel modes utilize respectively the lower 5, 6 or 7 bits of the counters.

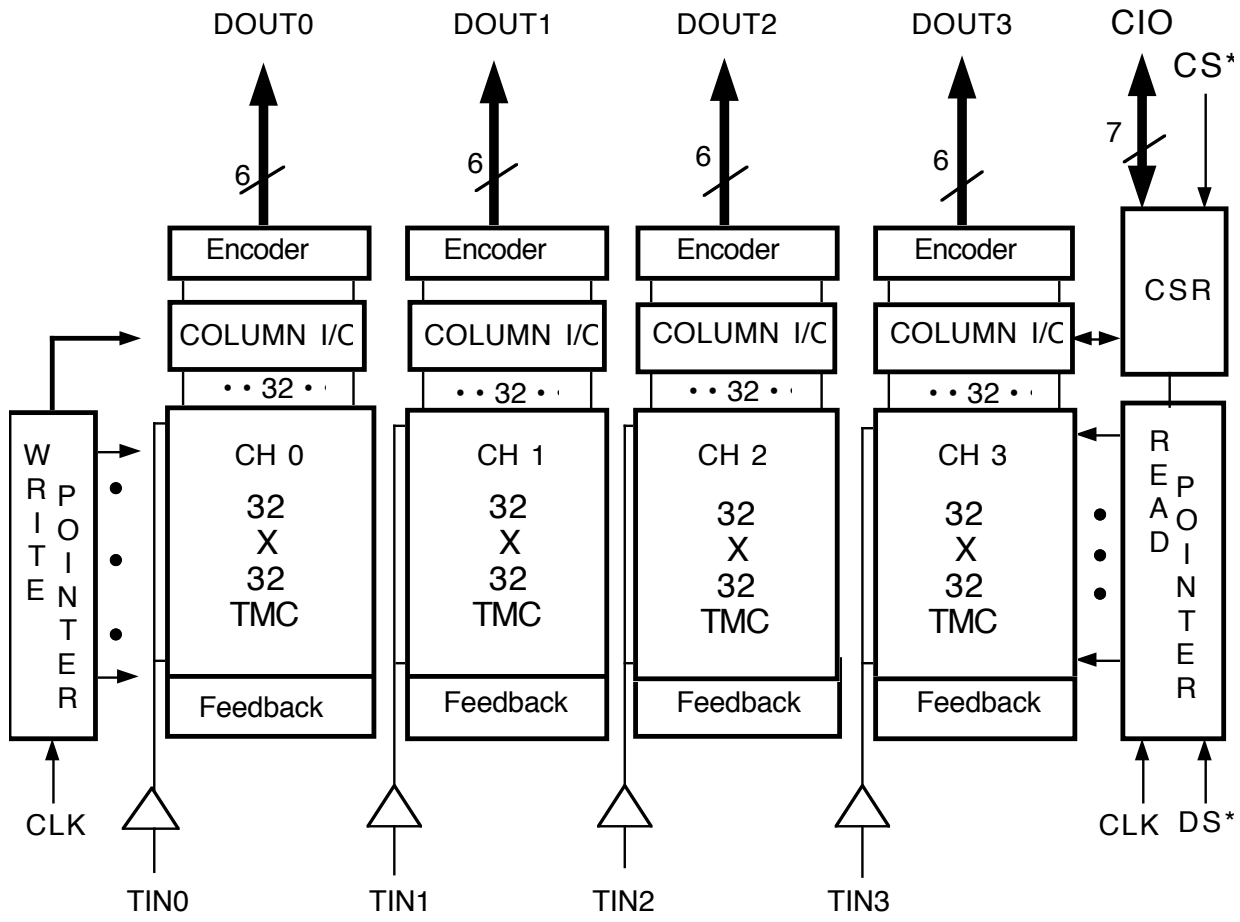


Fig. 5. Block diagram of the TMC1004.

The 32 bit row data is encoded to 6 bits. The most significant bit shows the value of the first bit of a row, and the remaining 5 bits show the position of the "0" to first "1" transition. Since the transition times will be spaced by at least 32 ns, the encoding reduces the output pin requirement and the amount of data without sacrificing information. The readout cycle is pipelined to 2 stage and the cycle continues while the trigger signal DS* is asserted. The data are read out through the DOUT lines.

There are 3 CSR registers which set/show the operating mode and the settings of the pointers. All TMC cells can also be read and written through the CSR register. This access path is used for testing each TMC cell. The CSR register is accessed through the CS* and the CIO lines.

Fig.6. Photograph of the TMC1004 chip.

References

[1]Y. Arai, T. Matsumura and K. Endo, IEEE Journal of Solid-State Circuits. Vol. 27, No. 3, 359(1992).

[2] Y. Arai and T. Baba, 1988 Symposium on VLSI Circuits, Tokyo, Aug.1988, IEEE CAT. No. 88 TH 0227-9 Page 121.

[Appendix A : Sample Program]

```
C...A part of Sample Readout Program for the TMC CAMAC module
C...        Common Start mode.
C
C...Start
                :
C...Stop
                :
C...Read out Final Row Position from CSR2 (Write Pointer)
            IADD=0
            CALL CAM16(CHAN,CRATE,ISLOT,IADD, 6,MM,ERRSTAT)
            MM = MM - 32
            IF (MM.lt.0) MM=MM + 32          ! MM points first Row of data recording

C...Find Start Time
            STIME=0
C...Set Start Row to CSR1 (Read Pointer)
            DO RR=MM,MM+1
            CALL CAM16(CHAN,CRATE,ISLOT,IADD,20,RR,ERRSTAT)
C...Read out strt time
            CALL CAM24(CHAN,CRATE,ISLOT,IADD,0,IDATA_4,ERRSTAT)
            DD=IAND(IDATA_4,'3F'x)
            ZQ=IAND(DD,'20'x)
            TT=IAND(DD,'1F'x)
            IF(ZQ.EQ.0) GO TO 556
            STIME=RR*32
            GO TO 555
  556       CONTINUE
            IF(TT.EQ.0) GO TO 71
            STIME=RR*32+TT
            GO TO 555
   71       CONTINUE
            ENDDO
            TYPE *,'Error! No Start Time Data'
C...
   555      CONTINUE

C...Find Stop Time
            DO 70 IADD = 0,7
            DO RR=MM+2,MM+31
C...Write Start Row to CSR1
                CALL CAM16(CHAN,CRATE,ISLOT,IADD,20,RR,ERRSTAT)
C...Read out one chip data
                CALL CAM24(CHAN,CRATE,ISLOT,IADD,0,IDATA_4,ERRSTAT)
                IDATA_S(RR)=IDATA_4
            ENDDO
C...Extract one channel data
            DO 70 JL=0,3
            ICHAN=4*IADD+JL+1
            IT1=6*JL
            ZZ = 0
            DO 70 RR=MM+2,MM+31
            IDATA_4=IDATA_S(RR)
            DD=ISHFT(IDATA_4,-IT1)
            DD=IAND(DD,'77'O)
            TT=0
            IF(ZZ.NE.0) GO TO 511
            ZQ=IAND(DD,'40'O)
            IF(ZQ.NE.0) GO TO 515
  514       CONTINUE
            TT=IAND(DD,'37'O)
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```
      IF(TT.EQ.0) GO TO 70
515   CONTINUE
      M(1,ICNT) = ICHAN                    ! Channel No. of ICNT data
      M(2,ICNT) = RR*32 + TT - STIME       ! Timing data of ICNT data
      ICNT = ICNT + 1
      ZZ=1
      GO TO 70
511   CONTINUE
      ZQ=IAND(DD,'40'O)
      IF(ZQ.NE.0) GO TO 70
      ZZ=0
      GO TO 514
70    CONTINUE
```