TMC304(TMC-TEG3) Trouble Report

April 22, 1996 Yasuo Arai (KEK)

I. Trap of PLL oscillation at unstable state.

[Symptom]

Recently, we have built 20 TMC-VME boards, each of which implements 8 TMC304 (TMC-TEG3) chips. Thus we have tested 160 TMC chips. Then we observed unstable PLL oscillation in about 10% of channels.

Fig. 1-(a) shows normal wave form of the PLL oscillation, and Fig. 1-(b) shows abnormal one. Fig. 2-(a) shows a histogram of oscillation period for normal channel, and Fig. 2-(b) shows abnormal one. From these measurement, we can see there are 3 different oscillation periods, and it still follows external clock frequency of 40MHz in average.

This abnormal oscillation will not occur every time. In some channels, it occurs very often, and in other channel it occurs scarcely. It looks like depend on crate, so depend on characteristic of power supply.

Fig. 3 shows trace of the PLL control voltage (VGN0..3). In normal channel, it goes up to 2.4 V and gradually come to stable point of around 1.8V. On the other hand, in abnormal channel, the voltage is trapped at around 1V.

[Measuring Method]

By connecting 'TSTROSC' pin to VDD, PLL oscillation clock will appear in the 'ROSC' pin. The channel of the PLL is selected by 'DCH0' and 'DCH1' pins.

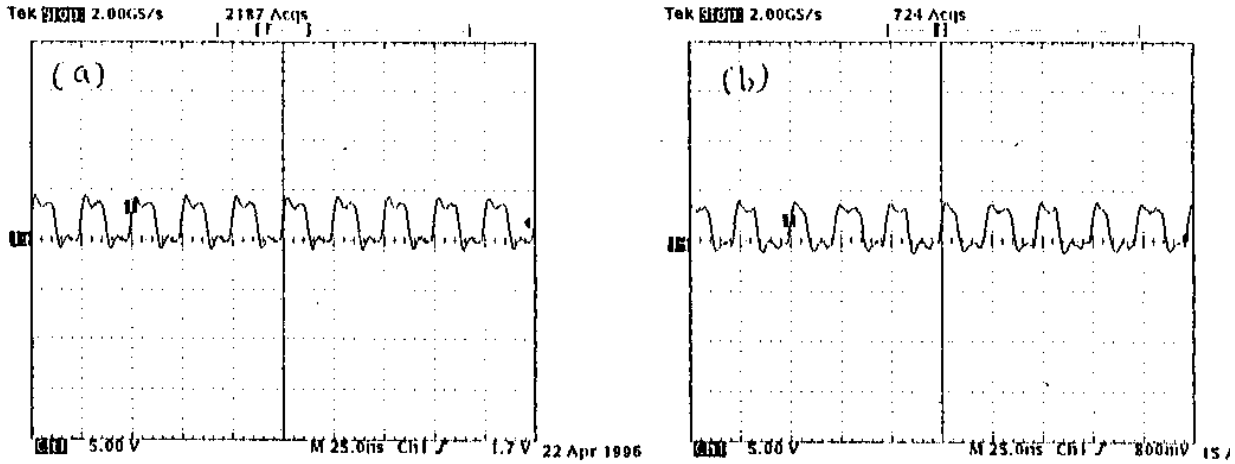


Fig. 1 PLL clock wave form. (a) normal, (b) abnormal.

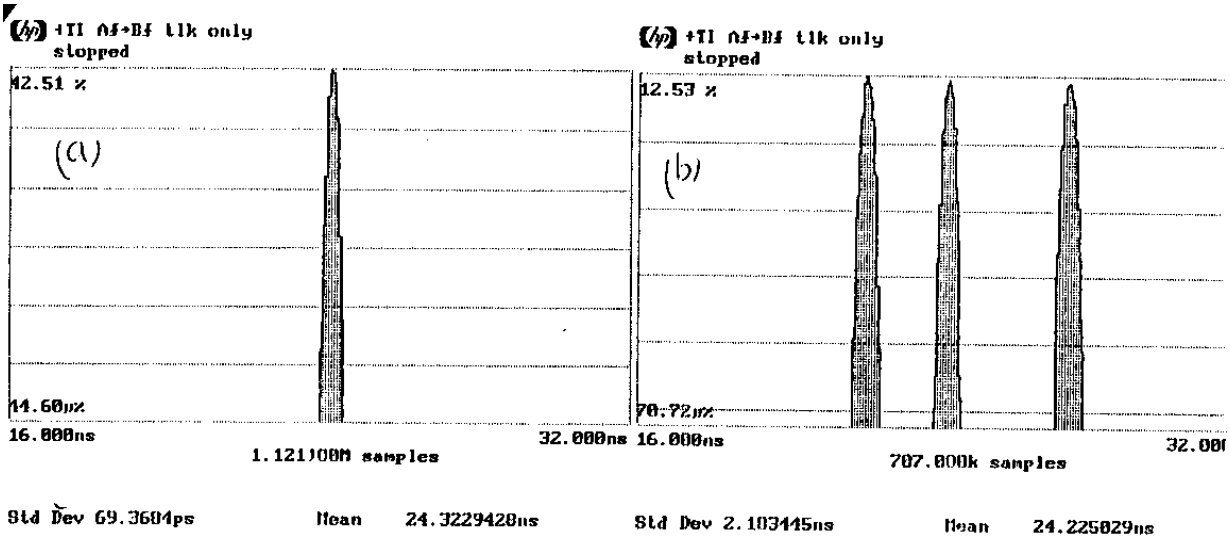


Fig.2 Clock period distribution (log scale). (a) normal, (b) abnormal.

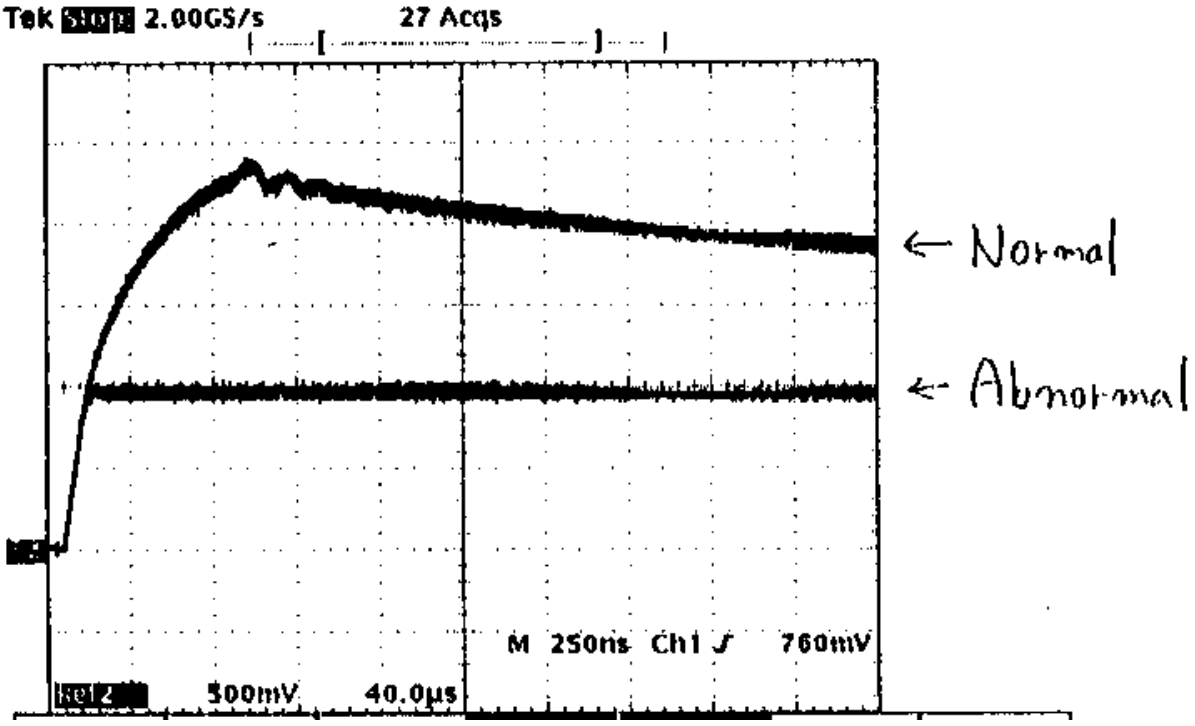


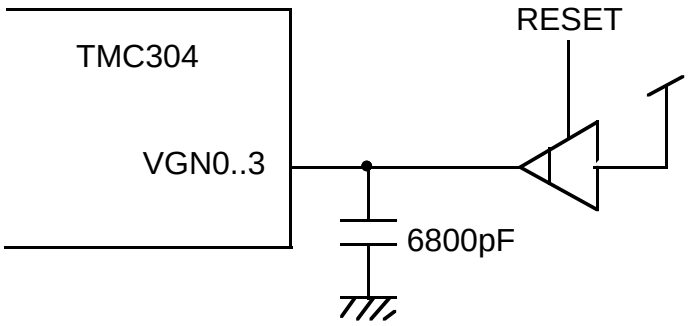
Fig. 3 Trace of the control voltage VGN.

[Fixing method]

For the moment, we can avoid above phenomena with following fixing.

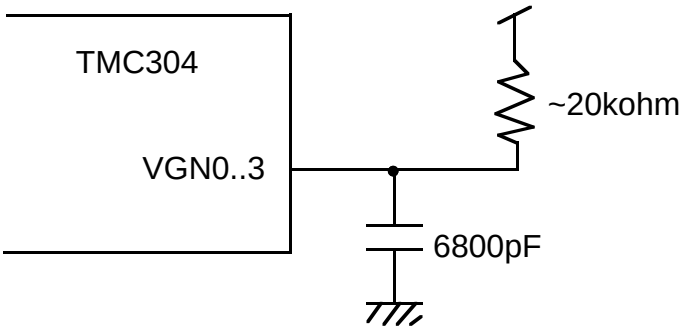
A. Connect to Vdd at Reset cycle.

Since the trap occurs when the control voltage goes up from ground level, if you can connect the control voltage to Vdd at power on or reset‘, you can avoid this trap.



B. Pull up with resister

More easy method is connect a pull up resistor to the control voltage. This pull up register will help to skip the unstable point. Since the internal pull-down transistor for the control voltage can sink up to 4 mA, pull up resistor of around 20 kohm can be used safely.



II.TMC Internal Memory Error

[Symptom]

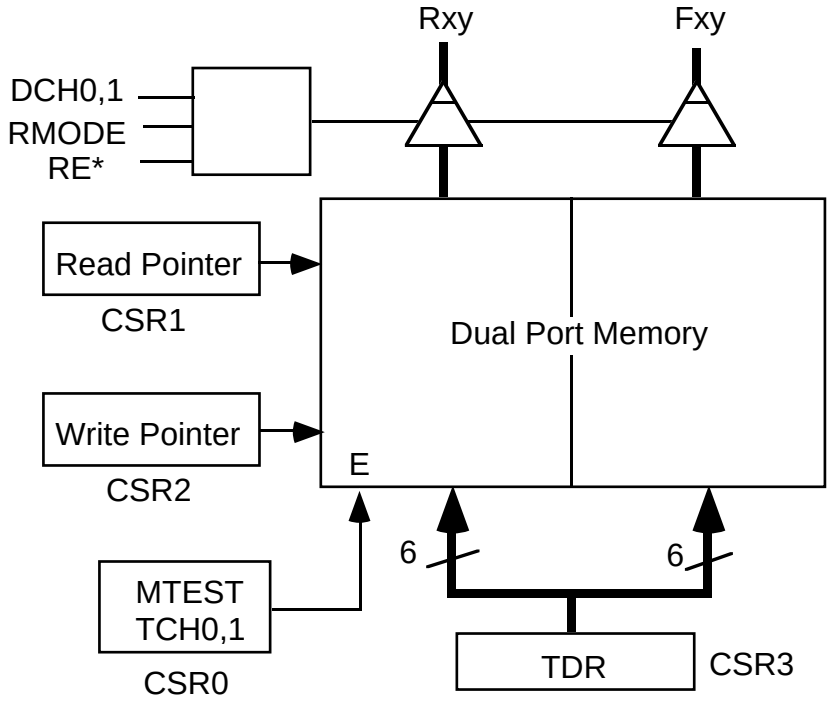
We found memory bit error in about 5% of chips. In a time difference measurement, it is usually very difficult to find the least significant bit error. However, if there is an error in upper bit, you can observe large (2bit, 4bit, .. 16bit) deviation of data occasionally. If there is an error in hit bit, you can miss the hit.

[Measuring Method]

You need rather tedious sequence to check the internal memory.

i) Set MTEST bit (bit 6) and select test channel with TCH0(bit 1) and TCH0(bit2) in the CSR0.
ii) Set write address in the Write Pointer Register of the CSR2.
iii) Write test data in the Test Data Register (bit 0 - 5) of the CSR3. This data is written to the both rising edge and falling edge memory selected with TCH0, 1 and addressed with CSR2
iv) Set read address in the Read Pointer Register of the CSR1.
v) Read data from the data line of the selected channel (Rxy and Fxy; x=channel number, y=0..5)

Repeat (ii) .. (v) with combination of data and address for every memory bit.



[Fixing method]

No fixing method.

Origin of the abnormal oscillation in the TMC304(TMC-TEG3)

May 31, 1996 Y. Arai (KEK)
(revised Nov. 13, 1996)

I have reported on the abnormal oscillation in the previous report titled "TMC304(TMC-TEG3) Trouble Report (April 22, 1996)". Since then, I could specify the origin of the abnormal oscillation, so I explain it here. In this report, I also mention about a new fixing method which is not shown in the previous report.

In the "abnormal oscillation" state, the control voltage of Vgn is trapped at around 1.0V, while in the normal oscillation it is around 1.8V. There are 3 different periods of pulses in the abnormal oscillation as shown in Fig. 1.

Fig. 2 shows the relation between the control voltage Vgn and the delay time of a set of delay elements. The delay at Vgn=1.0 V is about three times larger than the delay at Vgn=1.8 V. Then I thought of possibility of 3rd harmonics of oscillation (although this is not exactly 3rd harmonics of oscillation).

I have done simulations for the circuit shown in Fig. 3, in which Vgn is set to 1.0V. Fig. 4-(a) and (b) are simulation result starting from different initial conditions. In Fig. 4-(a), there is only one wave front (edge) in the ring oscillator, while there are three wave fronts in the Fig. 4-(b). The oscillation period in Fig. 4-(a) is about 75ns, and an average period in Fig. 4-(b) is 25ns. Thus the oscillation in Fig. 4-(b) can be locked to external clock of 40MHz.

Since there is no initialization circuit in the ring oscillator, the initial condition is not determined. Usually, there appear only one edge, but it is also possible to have 3 edges.

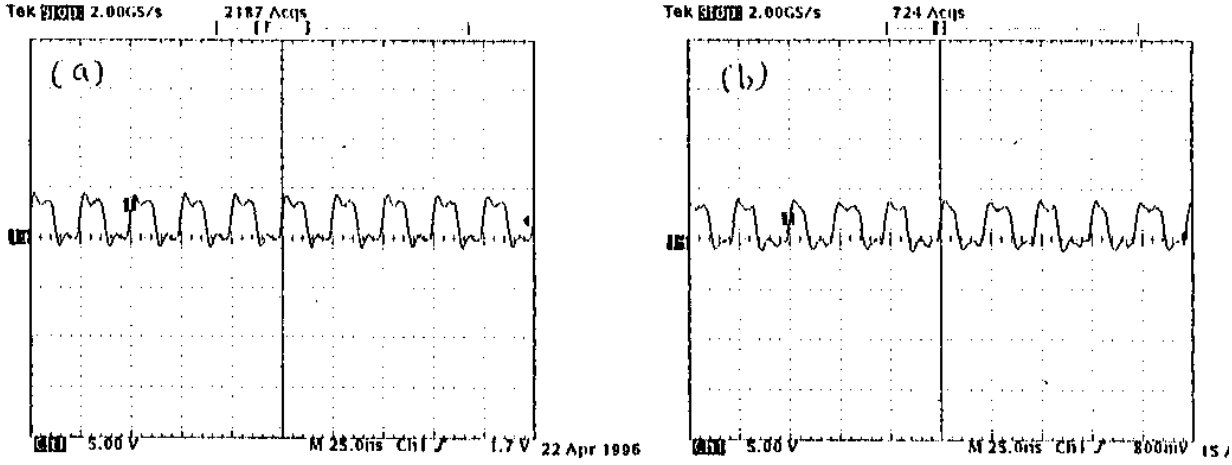


Fig. 1 PLL clock wave form. (a) normal, (b) abnormal.

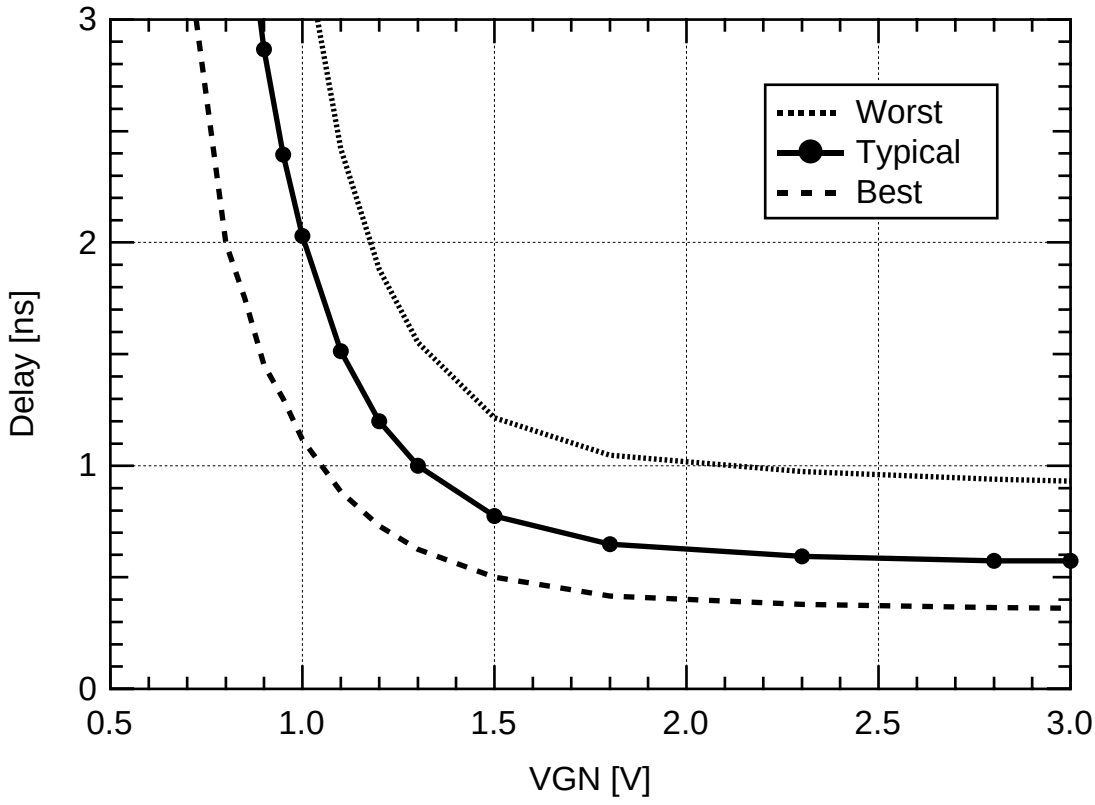


Fig. 2 Simulation of the propagation delay characteristic of the delay stage (two delay elements) for the control voltage VGN under best, typical and worst conditions.

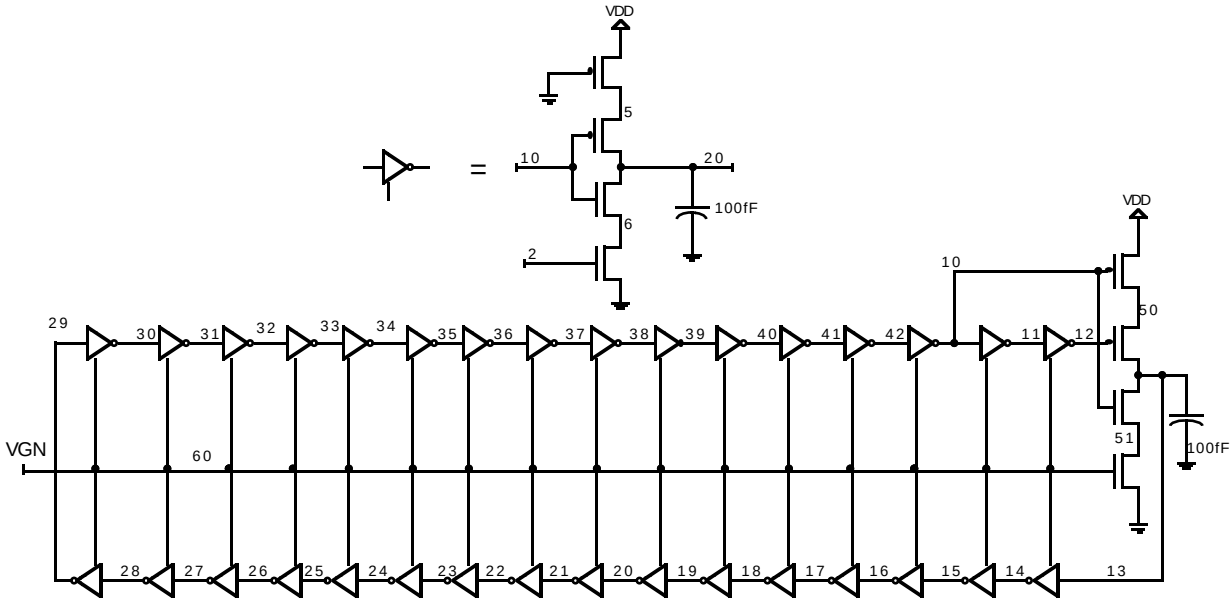


Fig. 3 Circuit diagram of the ring oscillator used in the simulation.

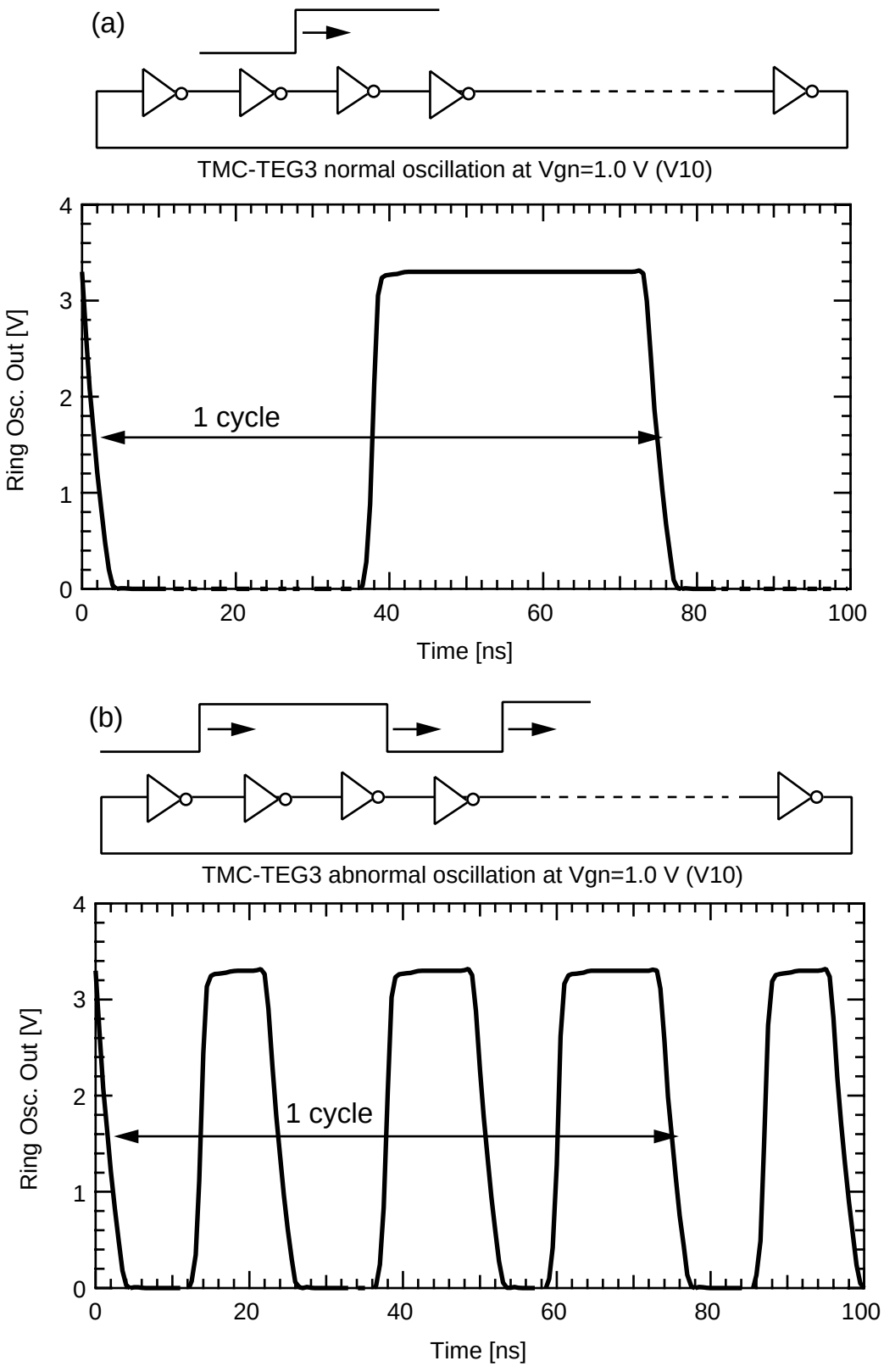


Fig. 4 Simulated wave form with different initial condition. (a) one wave front, (b) three wave front.

Fortuitously, there is a stop gate in TMC-TEG5, so this abnormal oscillation will not occur in the TMC-TEG5. This phenomena occurs only in TMC304(TMC-TEG3) and TMC-TEG4. So far, we have seen this abnormal oscillation at 40MHz clock only. We have not yet observed it at 26 MHz although the observed sample is not so large.

[New fixing method]

I have shown two fixing methods for this phenomena in the previous report;

(A) connect Vgn to Vdd during RESET.
(B) pull up Vgn with a 20kΩ resistor.

Now we knows the origin of the abnormal oscillation, thus I can propose to you new fixing method.

[DIV4 = 1]

If you are using "multiply by 4 mode" (DIV4 = 1), then you just need to keep RESET period for more than 1 μsec. Since the divide by 4 circuit in the chip is stopped during RESET, the Vgn signal come close to Vdd during the RESET period. After releasing the RESET, the PLL frequency come to stable point from high frequency.

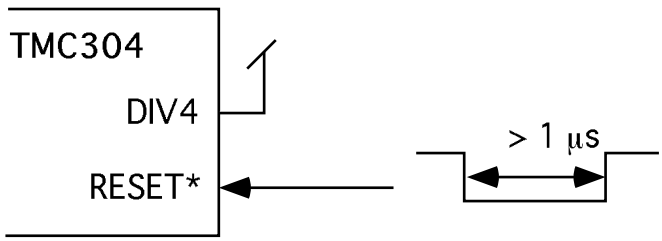


Fig. 5-(b) Fixing method for DIV4=1 mode.

[DIV4 = 0]

If you are not using "multiply by 4 mode" (DIV4 = 0), then connect DIV4 signal to RESET signal and keep RESET period for more than 1 μsec. This emulate above situation.

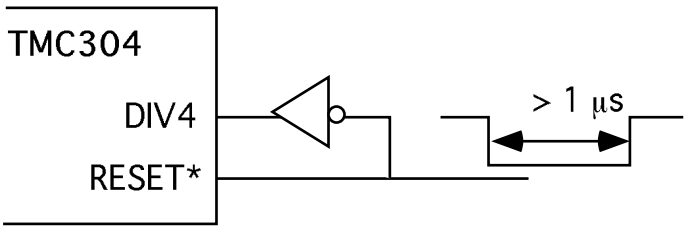


Fig. 5-(b) Fixing method for DIV4=0 mode.