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A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution

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Abstract - A pipelined time digitizer CMOS gate-array has been developed using 0.5 μm Sea-of-Gate technology. Precise timing signals which are used to sample input signals are generated from 32 taps of an asymmetric ring oscillator. The frequency of the oscillator is controlled by a PLL circuit which runs in the 10 - 50 MHz frequency range. A test chip has been developed and tested; a time resolution of 250 ps rms at 40 MHz clock was measured. The chip has 4 channels and encoding circuits for both the rising and the falling edges of the input signals. The chip has 128-word dual-port memories, allowing the histories of the input signals to be stored and causing no deadtime for the conversion.

I. Introduction

Recent high-energy physics experiments are demanding a pipeline (deadtime-less) time-to-digital converter (TDC) with a time resolution of better than 500 ps and a double-pulse resolution of less than 30 ns. The TDC must keep all of the timing history until a trigger signal arrives about 3 μsec later. In large experiments, since the number of channels used is more than 100 k, the device must have a low power dissipation, a high circuit density and a low cost .

There is an analog approach to this kind of TDC which uses a time-to-charge converter with analog-memory units (TCCAMU, [1]). We took a digital approach and developed a pipeline TDC LSI called a time memory cell (TMC) [2,3] in 1990 by using 0.8 μm CMOS technology with a full-custom layout. The chip has a 1 μsec synchronous buffer and attained a 520 ps rms time resolution. Voltage-controlled delay elements are used to obtain 1 ns timing; they are controlled by a pseudo-PLL circuit (DLL : Delay Locked Loop). After the success of the chip, several groups also developed TDC's by using the same kinds of techniques, but implemented asynchronous buffers [4,5,6] instead of synchronous buffers. In these chips, the buffer depth is optimized for a specific application and has a smaller gate count per channel. However, the rather complicated control logic used to handle the buffer and trigger signal is required due to the event-driven architecture. Furthermore, the required buffer depth will increase as the input rate increases. Thus, for high-rate applications, the synchronous buffer system is more adequate in both simplicity and the gate count.

We also found that TMC-like devices have applications in many fields; not only scientific fields but also in such industries as the mass spectroscopy of recoiled ions (MSRI) [7], distance measurements of auto mobiles[8], and video signal processing [9]. Although the first TMC chip (TMC1004) fulfills most of our basic requirements, the development cost was relatively high, and it was not so easy to modify the circuits for each application due to the full-custom layout. Each application requires a different performance in the encoding circuit (rising edge and/or falling edge), double-pulse resolution, time resolution, and the buffer depth. To ease the modification and to reduce the cost, we began to develop a gate-array version of the TMC. In addition, the gate-array structure is more adequate for a radiation-hardened process, which is required in some experiments, due to the uniform physical structure of transistors.

The direct conversion of the TMC circuit to a gate-array is not suitable due to the difference in the technologies; we thus newly developed a time digitizing circuit with a phase locked loop (PLL) circuit. To obtain an even number of equally spaced timing signals, we developed an asymmetric ring oscillator and implemented 32 stages of the oscillator in the gate-array chip. The time-critical parts are simulated in an analog simulator and manually arranged; however all other parts were designed with a conventional gate-array design methodology. Besides a reduction in the cost and the turn-around time, the time resolution and stability have also been improved in the new chip.

In this paper we report on the circuit and test results of a test chip named TMC-TEG3. The technology used is Toshiba's 0.5 μm CMOS Sea-of-Gate gate-array (TC180G series, 3.3V operating voltage). In section II, we present a general scheme of the chip. The new features of the circuit are described in detail in section III and experimental results are presented in section IV. A discussion of the timing accuracy of the circuit is presented in section V.

II. General Scheme

In our application, two accelerator beams collide at every tens of ns, and the collision generates many secondary particles. Sophisticated electronic detectors catch these particles and record their signals. Since not all of these collisions is interesting from the physics point of view, a trigger signal is generated to identify an interesting event. It will take a few μsec to make a trigger decision, so all the data must be kept in local electronics until the trigger signal comes.

In the TMC, there is a dual port memory to store the temporary data. Two address pointers of the memory, write and read pointers, are incremented synchronous to the system clock and the memory acts as a ring buffer. All the input signal is recorded into the dual port memory of which address is provided by the write pointer. If a trigger signal comes, corresponding part of data are read out from the memory of which address is provided by the read pointer. New data can be recorded even when the trigerd data is read out . In this way, all the timing information of the input signal can be derived without causing any deadtime.

While the TMC stores 32 bits of time sliced data in each clock cycle, there is at most one transition in the cycle due to the detector response time. Thus it is better to reduce data size by implementing an encoding circuit. The encoder searches transition point and encode its address. Thus the 32 bits data are reduced to 5 bits. In addition, there needs a hit tag bit which represent the existence of the transition.

III. CIRCUIT DESCRIPTION

Fig. 1 shows a block diagram of the TMC-TEG3 chip. There are 4 input channels in the chip. Each channel has a 32 bit TMC circuit, a PLL circuit, rising- and falling-edge encoders, a 128 word dual-port memory, and output timing logic. A 24-bit wide dual-port memory is shared by 2 channels as 12 bits each. There are 4 control and status registers (CSR's) to set write and read pointers, and various conditions.

Input receivers for the clock and measuring signals are also custom designed and operate as either single-ended or differential input receivers. Table 1 summarizes the main features of the TMC-TEG3 chip.

Table 1. Main features of the TMC-TEG3 chip

Technology	0.5 μm CMOS Sea-of-Gates (TC180G).
System clock	50 ~ 10 MHz (12.5 ~ 2.5 MHz : x4 mode). Single ended : CMOS level, or differential : $\Delta V > 50$ mV (Vcenter = 2 ± 0.6 V).
Digitization Step	0.6 ~ 3.1 ns/bit (= clock period / 32).
Time Resolution	250 ps rms @40 MHz.
Differential Nonlinearity	< 0.08 LSB @40 MHz
Integral Nonlinearity	< 0.1 LSB @40MHz
Time Range	2.56 μs ~ 12.8 μs (clock period x 128).
Input Channels	4 ch (single ended or differential).
Master Gate Size	66k Master (6.4 x 6.4 mm die), 32k gates used.
Phase Locked Loop	Response time : ~ 4 μsec.
Encoding Scheme	Dual edge encode : (hit tag + 5 bit) x 2 (rise and fall) x 4 ch.
Double Pulse Resolution	≤ Clock Period (≤ 25 ns @40 MHz).
Power Supply Voltage	3.3 V.
Power Consumption	< 200 mW @40 MHz clock, 1 MHz input, 100 kHz readout.
Package	0.5 mm pitch, 144 pins plastic QFP.

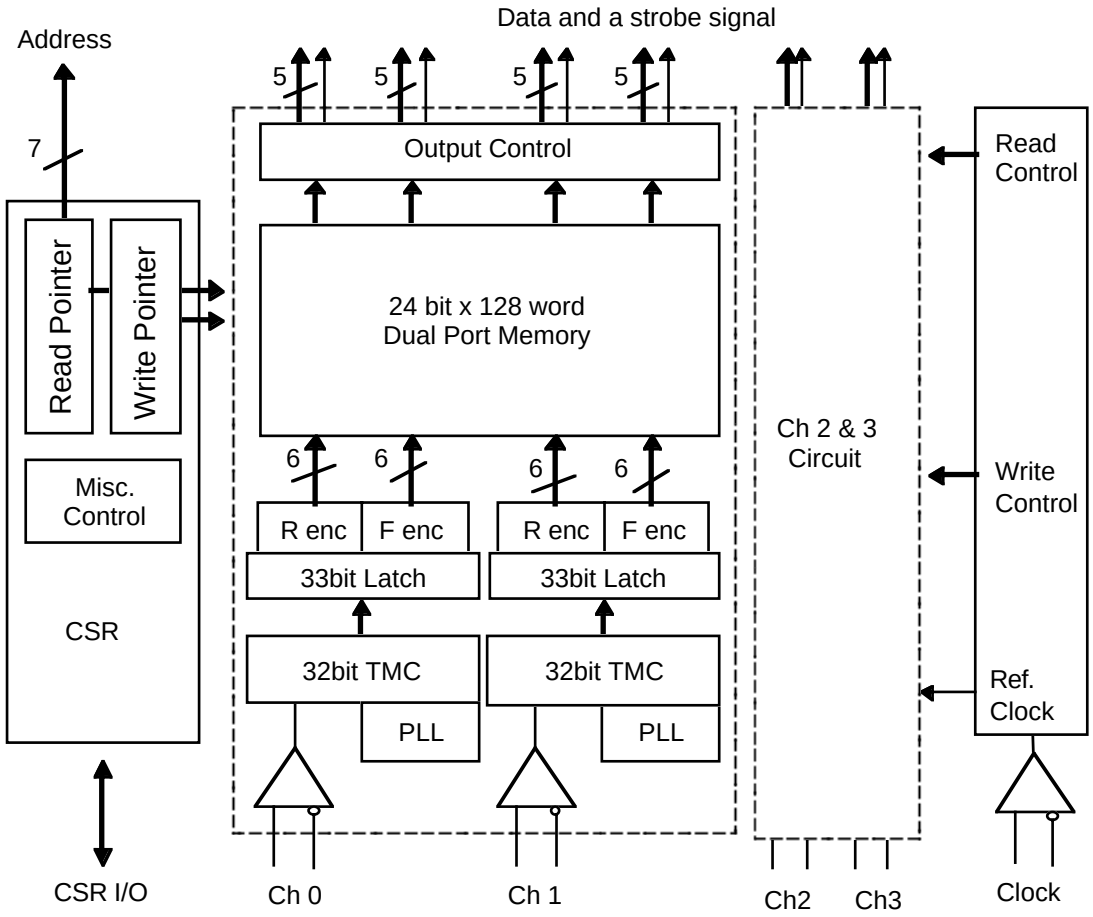

Fig. 1. Block diagram of the TMC-TEG3 chip.

A. TMC & Asymmetric Ring Oscillator

The heart of the time-to-digital conversion part is called a time memory cell (TMC), which comprises a voltage-controlled delay element and a memory. In the TMC1004, voltage-controlled delay lines and a DLL circuit were used to obtain precise timing, as shown in Fig. 2-(a). TMC cells are arranged as an array. Since the sampled data are kept locally and do not move until readout, the power consumption can be kept very low (< 10 mW/ch). The accuracy of the delay-line structure is mainly limited by an accumulation of the timing jitter in the delay line and non-uniformity of the delay elements. In addition, the circuit requires good matching of delays between the clock path and the delay path, since the difference in these delays causes a differential non-linearity error.

The new scheme used in the TEG3 chip is shown in Fig. 2-(b). In this scheme, standard dual-port memories are used for the data buffer, and only 33 delay elements and 32 memories are used in a time-critical part. Since the time-critical parts are packed in very small area, the effect of non-uniformity in the delay elements can be minimized. Time-digitized data are transferred to the dual-port memory through a synchronization stage and encoders. The frequency of the asymmetric ring oscillator is controlled by a PLL circuit. Since the clock path difference just shifts the phase relation between the sampling time and the input signal, it does not affect the time-interval measurements if it is

stable. Thus, a fine adjustment of the clock path, which is rather hard to realize in a gate array design, can be avoided.

A ring oscillator normally comprises an odd number of inverter stages; an odd number of timing signals can be obtained. However, an even number of timing signals (especially 2's power) is desirable for our application. To obtain these signals we developed an asymmetric ring oscillator which generates an equally spaced even number of timing signals.

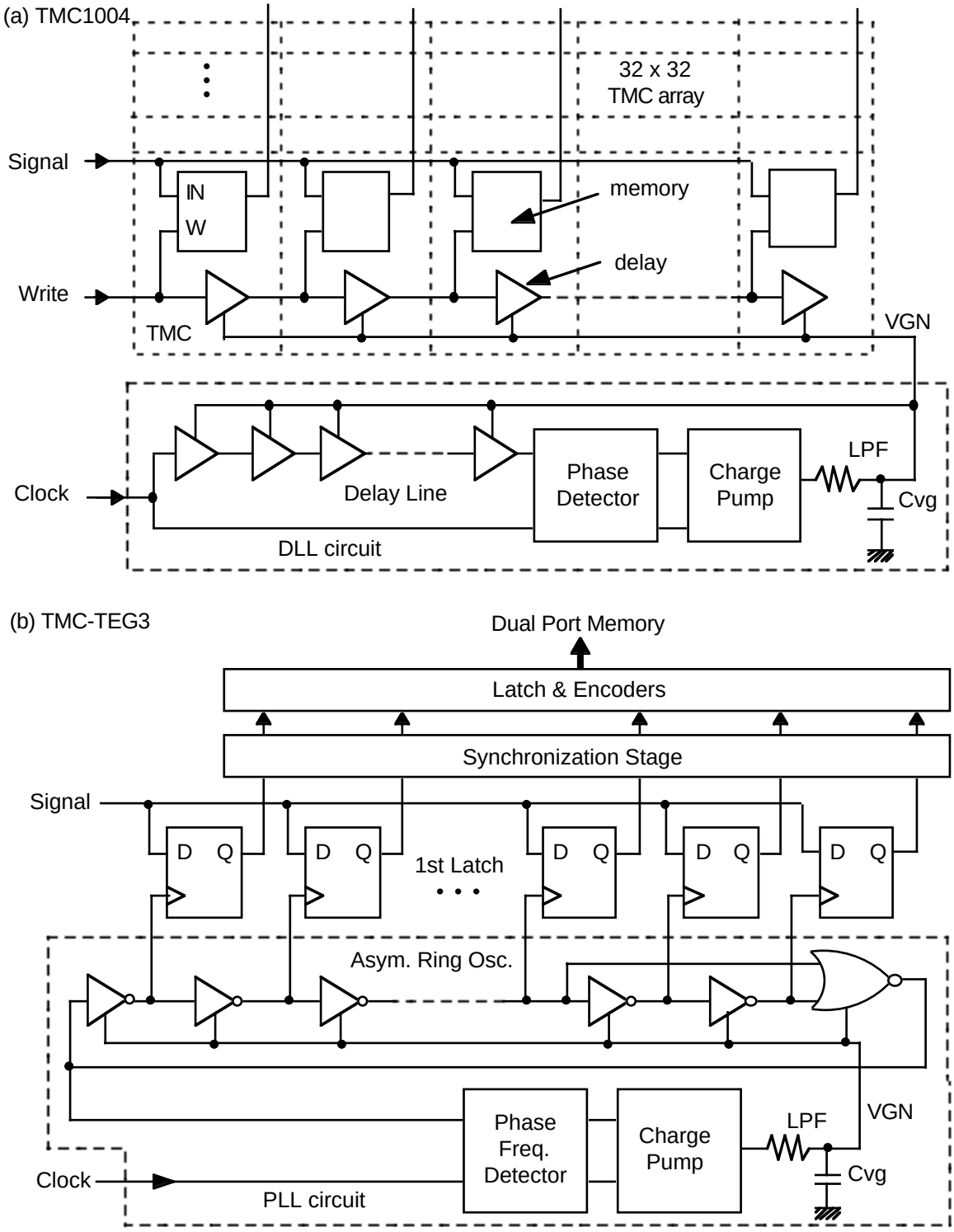

Fig. 2. Configuration of the time digitizing circuit in the (a) TMC1004 and (b) TMC-TEG3.

A simplified schematic of an asymmetric ring oscillator comprising 8 stages and their timing diagram are shown in Figs. 3-(a) and (b), respectively. The present TMC chip implements 32 stages. Timing signals are extracted from node A through H. Voltage-controlled delay elements (U1-U8 and US) are made of two PMOS transistors and two NMOS transistors, and fit in gate-array structure very well. The fall delay time (Tf) is controlled by transistor M4 through a control-voltage VGN, while the rise delay time (Tr) is not controlled. Since the output signal is inverted at each stage and input sampling occurs at the falling edge only, complementary control at the PMOS side is not necessary. Transistor M1 has been added to have the same structure as the US and its gate is connected to ground. The element US operates like a NOR gate. When node F goes high between time t2 and t3, the output node S becomes low. On the other hand, when node F goes low at time t6, node H is still high, so the node S remains at a low level. After node H goes low at time t7, the output node S goes to a high level.

At node A, a low-level signal passes through 7 inverter stages to return to node A, while a high-level signal passes through 9 inverter stages. Since the number of stages is odd for each half cycle, this chain of inverters oscillates. The total cycle time (T) will be (4Tr + 3Tf) + (4Tr+5Tf) = 8 x (Tr + Tf), and we can obtain an equally spaced timing of T/8 (= Tr + Tf) from this oscillator.

The layout was carefully arranged to have the same load capacitance at nodes A through H and S by adding some dummy transistors and having an equal path length. The layout image of a 32-bit TMC/synchronizing stage is shown in Fig. 4; its circuit schematic for one bit is shown in Fig. 5. The size of the layout for a channel is about 220 μm by 650 μm. The WIN and WOUT are connected circularly and an asymmetric ring oscillator is composed. The TIN is an input signal the timing of which is being measured. The gates of all unused transistors are connected to the VGN line as a part of a filter capacitor.

To encode digitized data, a synchronizing stage is provided after the TMC. A timing diagram of the synchronizing stage is shown in Fig. 6. First latch (see Fig. 5) stores the TIN signal at the falling-edge timing of the WOUT. The latched data is soon available at the PASS output. At half cycle later, the latched data is transferred to the BIT output. The BIT outputs are used for lower bits (B0-B15), and the PASS outputs are used for upper bits (B16-B31) and next cycle bit 0 (NB0). The NB0 is necessary for the data encoding described below. Since these 33-bit data are stable at the Tsync timing as shown in Fig. 6, all of the data can be stored safely into a 33-bit latch.

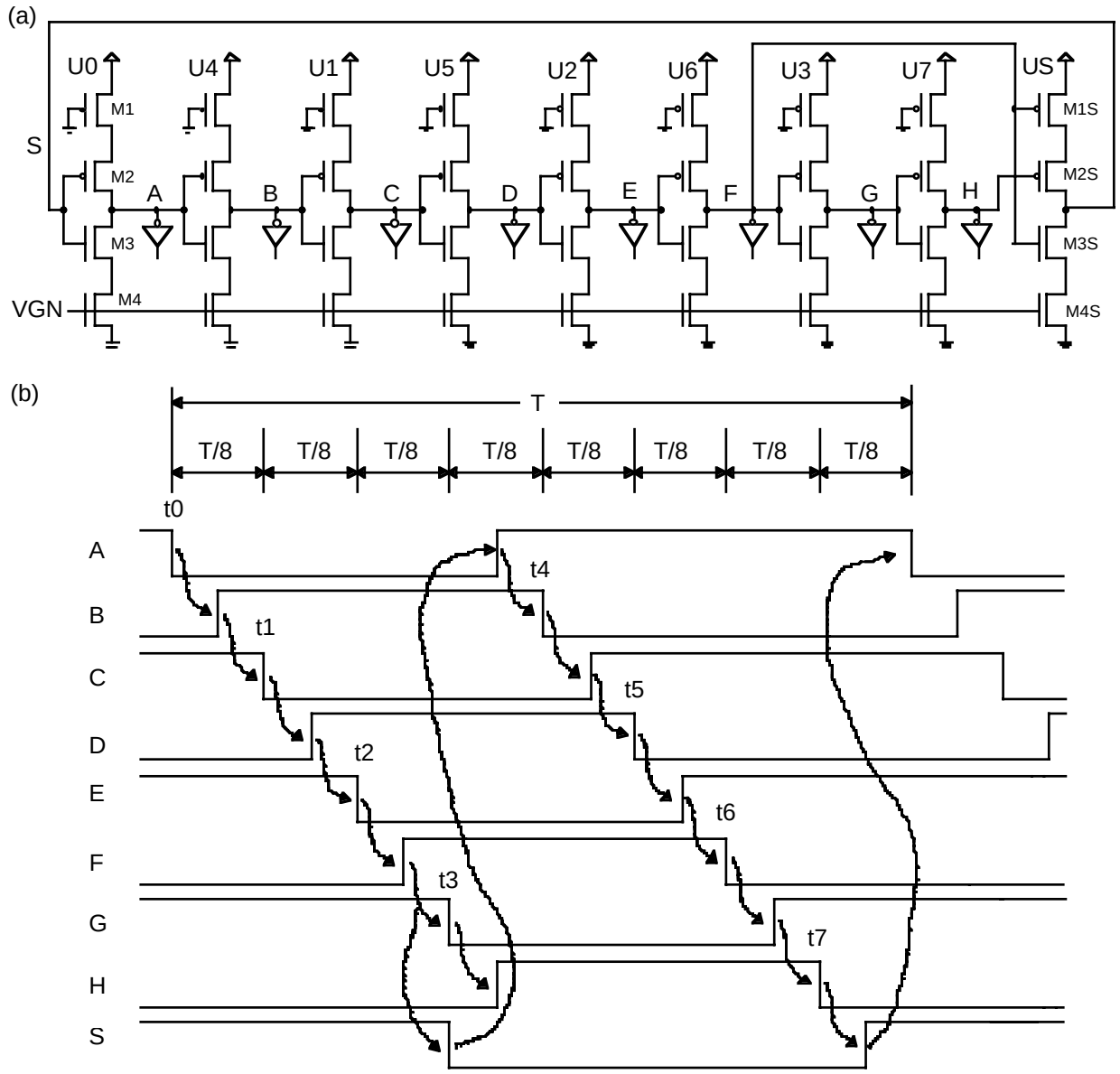

Fig. 3. An 8-bit example of the asymmetric ring oscillator; (a) a circuit schematic, (b) timing diagram.

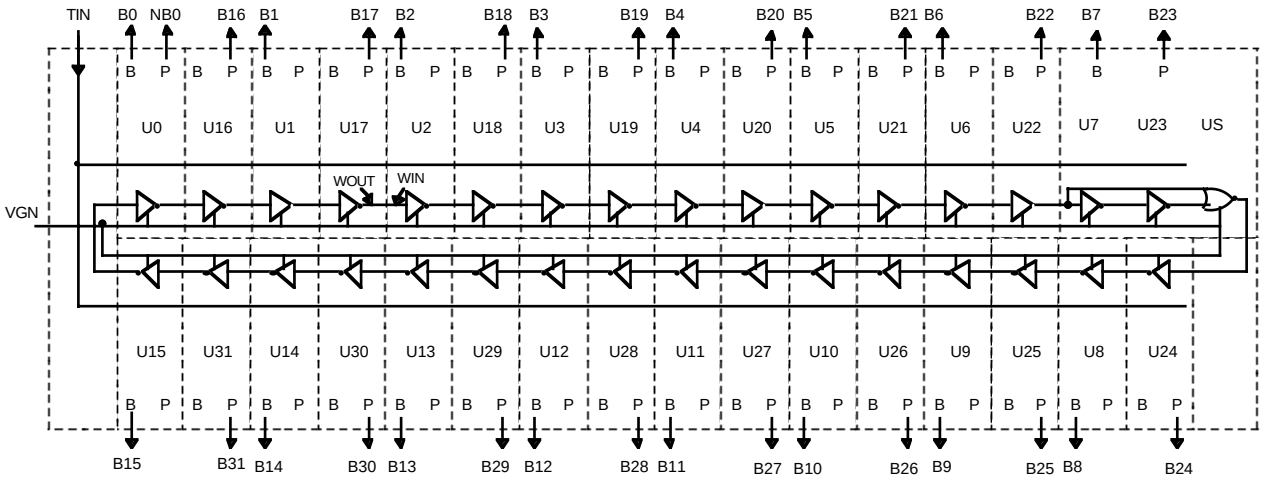

Fig. 4. Layout image of a 32-bit TMC/synchronizing stage. Only the delay elements and some global lines are shown. The circuit schematic of the U0 through U31 is presented in Fig. 5.

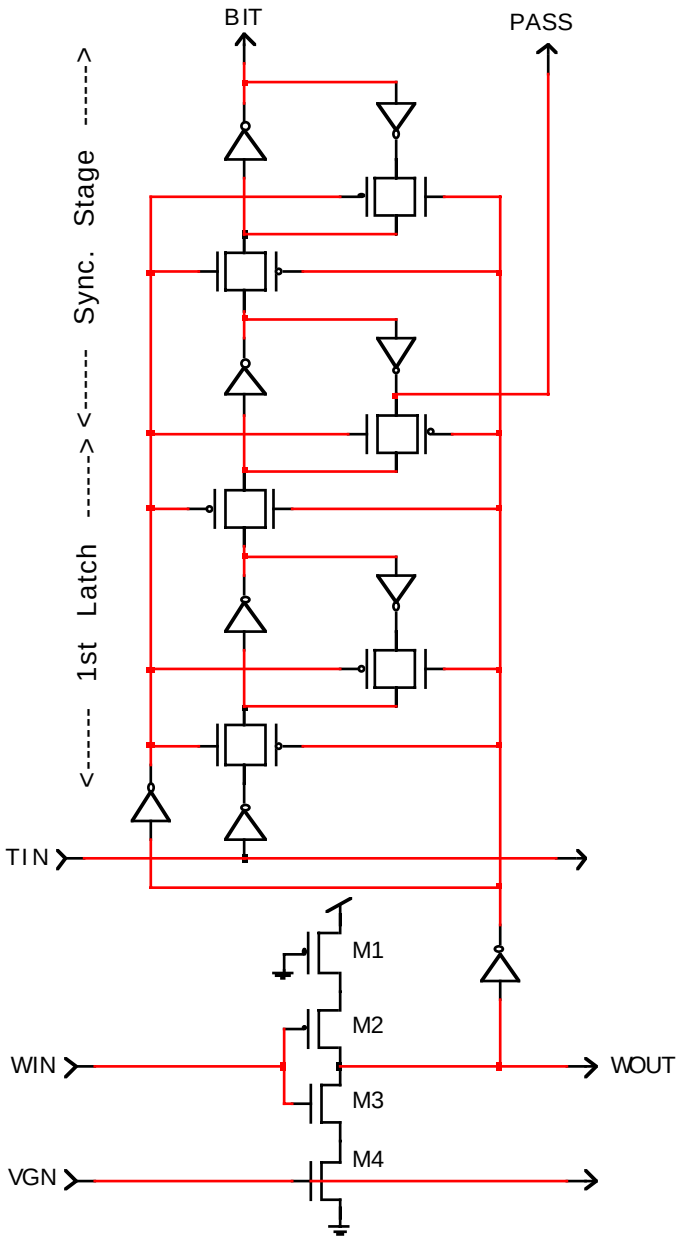

Fig. 5. A circuit schematic for one bit of the TMC circuit. The WIN and the WOUT signals are connected circularly as shown in Fig. 4. The BIT and/or The PASS outputs are connected to the 33-bit latch at next stage.

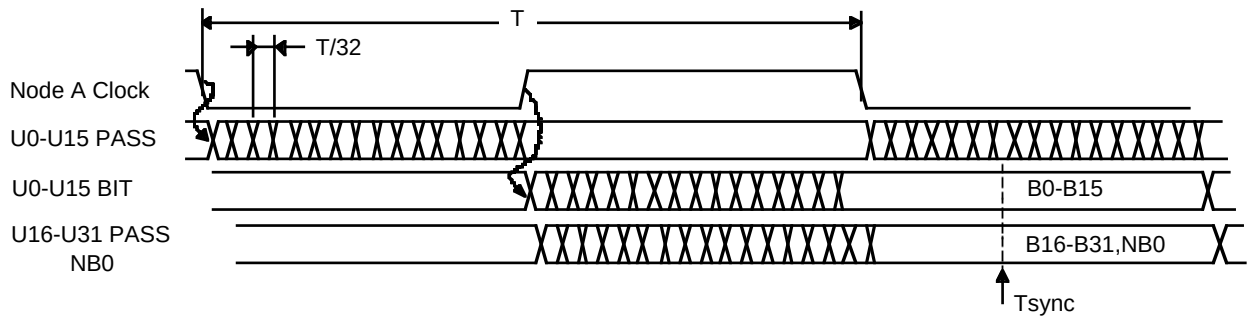

Fig. 6. Timing diagram of the synchronization stage. All the 33-bit data are stored in the 33-bit latch at the Tsync timing.

B. Rising and Falling Edge Encoders

The outputs of the 33-bit latch are transferred to rising- and falling-edge encoders. The rising-edge (falling-edge) encoder find the first rising (falling) edge and encodes it to 5-bit data and a hit tag bit. Other transitions after the first edge are ignored. To detect signal transition between the cycle, the NB0 signal, which is equivalent to bit 0 at the next cycle, is provided to the encoder . Furthermore, "all 0" and "all 1" conditions are represented by using a spare code with a hit tag bit of 0. The encoding scheme is summarized in Table 2. The encoded data are written to the dual-port memory half a cycle later.

Table 2 - Encoding Scheme (a) Rising edge encoder, (b) Falling edge encoder.

(a) TMC bit								next cycle	Hit Tag	Encoded Data
0	1	2	•	•	•	30	31	0	(1bit)	(5bit)
0	0	0	•	•	•	0	0	0	0	0
1	•	•	no rising edge			•	•	•	0	1
0	1	x	•	•	•	x	x	x	1	0
:	:	:	:			:	:	:	:	:
•	•	•	rising edge at N:N+1			•	•	•	1	N
:	:	:	:			:	:	:	:	:
•	•	•	no rising edge			•	0	1	1	31

(b) TMC bit								next cycle	Hit Tag	Encoded Data
0	1	2	•	•	•	30	31	0	(1bit)	(5bit)
1	1	1	•	•	•	1	1	1	0	0
0	•	•	no falling edge			•	•	•	0	1
1	0	x	•	•	•	x	x	x	1	0
:	:	:	:			:	:	:	:	:
•	•	•	fall. edge at N:N+1			•	•	•	1	N
:	:	:	:			:	:	:	:	:
•	•	•	no falling edge			•	1	0	1	31

(x : Don't Care)

C. PLL circuit

The PLL circuit comprises a phase frequency detector (PFD), a charge pump, a loop filter (LPF), and a voltage-controlled oscillator (VCO, that is the asymmetric ring oscillator). An external capacitor (Cvg) is used in the loop filter. A conventional sequential-logic PFD is used for phase/frequency detection[10]. Optionally a "divide by 4" counter can be inserted after the VCO, thus the frequency of the VCO can be either the same or the “multiplied by 4” of the input frequency.

The propagation delay of the delay elements that determine the oscillation frequency of the VCO is controlled through a control voltage (VGN). The delay characteristic of a delay stage (two delay elements) is simulated under best, typical and worst conditions and shown in Fig. 7. These conditions include supply voltage (Vdd = 3.0 - 3.6V), temperature (0 to 70˚C), and processing variations. In the typical condition, the shortest delay becomes about 600 ps.

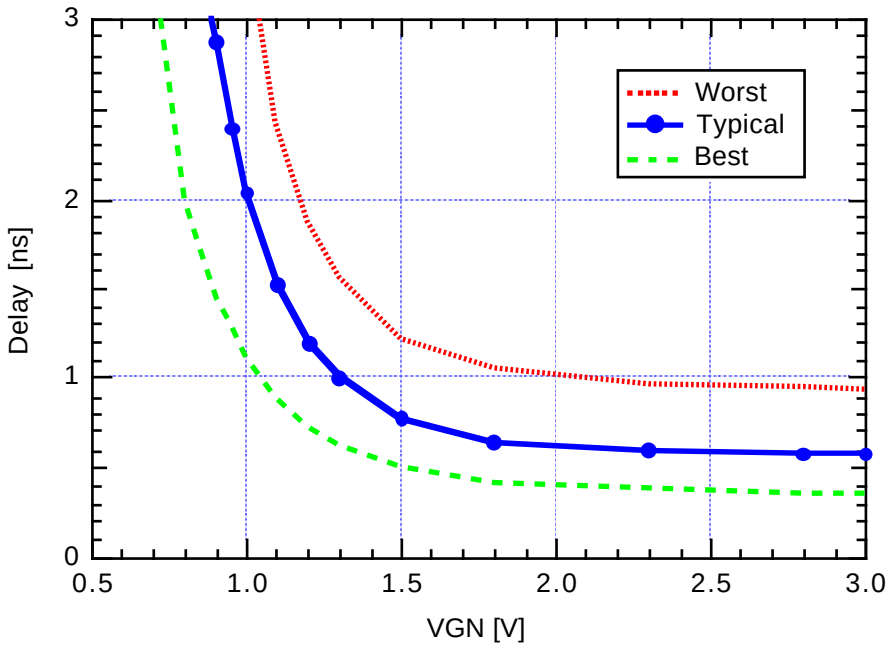

Fig. 7. Simulation of the propagation delay characteristic of the delay stage (two delay elements) for the control voltage VGN under best, typical and worst conditions. Typical condition is Vdd=3.3V and temperature of 27˚C. The best and the worst conditions include supply voltage (Vdd=3.0-3.6V), temperature (0 to 70˚C) and processing variations.

D. Readout mode

The readout circuit is accommodated to many kinds of readout circuits. The read pointer provides the address of the readout data and can be incremented synchronous to the clock or an external signal. For high-rate experiments, all 4-channel data will be read out synchronously with the system clock. In a zero-suppression mode, output strobe signals are generated from the hit-tag bit to send out only non-zero data. For slow readout applications, 4 output channels can be read out through a 12-bit bus after stopping the write operation.

IV. Test Results

A photograph of the TMC-TEG3 is shown in Fig. 8. The chip is 6.4 mm by 6.4 mm size and has a 66 k-gate master gate and about 32 k gates are used. Tests were performed at an operating voltage of 3.3V and most of the test were done at the clock frequency of 40 MHz.

A. Time Resolution

A time-resolution measurement was performed using a CAMAC system, which is a popular measurement system in nuclear and high-energy experiments. We used a TMC1004-CAMAC board [11] as a mother board and attached a new TMC chip to a TMC1004 socket through a daughter board. The TDC tester developed at our laboratory is used as a timing source, with a timing jitter of 20 ps rms. The clock signal is generated from a 80 MHz crystal oscillator and divided by 2 to obtain a symmetric 40 MHz clock. A start signal is supplied to both the TMC and the TDC tester after being

synchronized with the clock. After a preset time, the TDC tester generates a signal the timing of which is measured.

Fig. 9 shows a part of the linearity curve at the clock frequency of 40 MHz. The TMC circuit digitize an input signal at an interval of 32 stages and a slight gap were seen at 32 bit boundary in the TMC1004. However, there is no apparent gap seen in the TMC-TEG3 due to the uniform structure of the asymmetric ring oscillator.

Fig. 8. Photograph of the TMC-TEG3 chip.

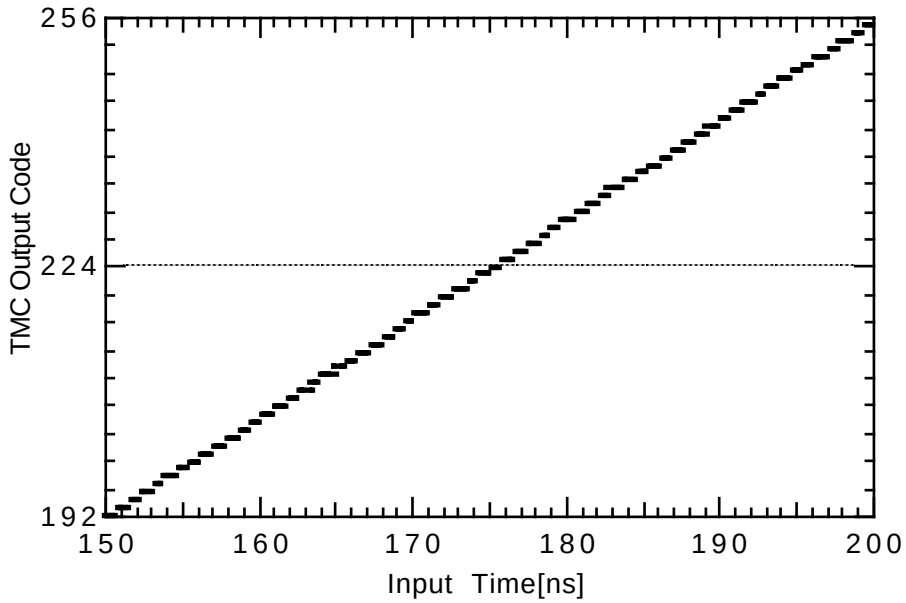

Fig. 9. Linearity curve of the TMC-TEG3. Data for 3 measurements are plotted. Only a part of time range is shown. There is no gap at output code of 224 which is a 32 bit boundary.

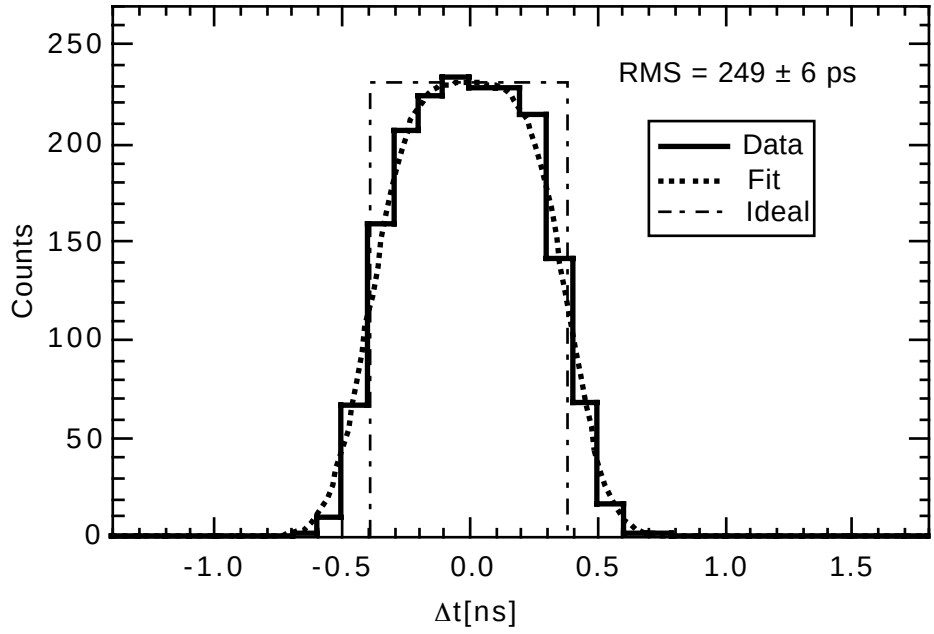

Fig. 10. Time-resolution measurement of the TMC-TEG3. The ideal distribution and a fitted curve by the function $F(x,\sigma)$ are also shown.

Fig. 10 shows a histogram of the deviation from the linear fit of the data. The rms value of the data is 249 ± 6 ps. Since one LSB is 781 ps, the quantization error is calculated to be 226 ps rms (=781ps / $\sqrt{12}$). The same measurement was performed for the "divide by 4" mode, where an input clock of 10 MHz is applied, and almost the same resolution is derived. A discussion of the source of the timing error is presented in the next section.

B. Differential and Integral nonlinearity

Fig. 11 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the TMC-TEG3 chip. Measurements were performed using a code density test, generating uniformly distributed time interval signals and taking a histogram of individual code occurrence. The histogram is accumulated for 5 LSB codes which correspond to 32-bit stages. Since the upper code is counted by the system clock, they can be neglected for DNL and INL measurements. The maximum errors of the DNL and INL are 0.08 LSB and 0.1 LSB respectively, and the rms errors of the DNL and INL are 24ps and 36ps, respectively. Points of large DNL errors (bit 8, 15, 22 and 23) correspond to the layout corner of the asymmetric ring oscillator (see Fig. 4). These errors can be reduced by making small modification of the layout in the next version.

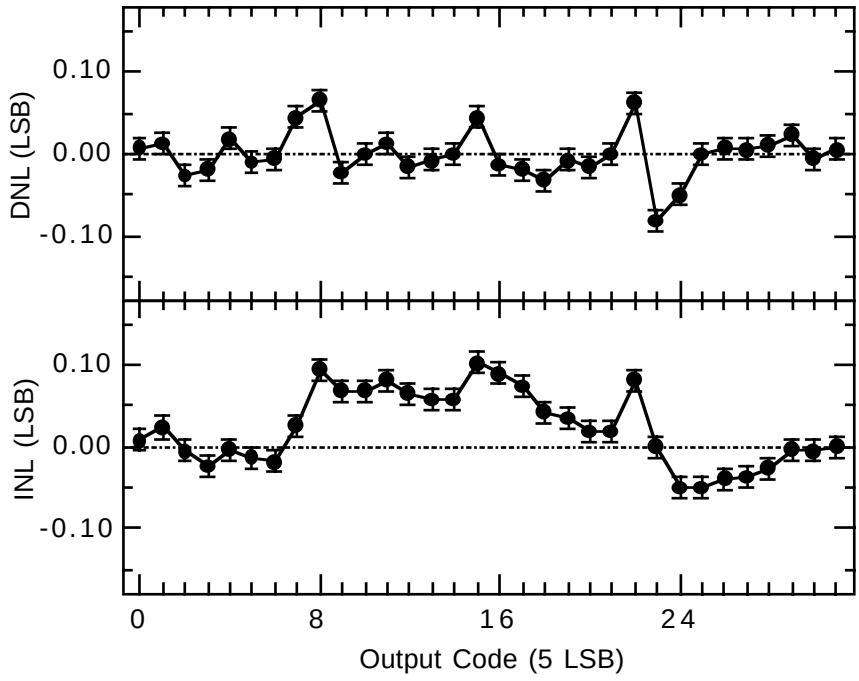

Fig. 11. Differential nonlinearity (DNL) and integral nonlinearity (INL) measurements at clock frequency of 40 MHz (1 LSB = 781ps).

C. PLL Tracking Range and stability

The PLL tracking range was measured. A reference clock is generated by a synthesized signal generator. The frequency and time interval were measured using a modulation domain analyzer.

For various input clock frequencies, oscillation cycle time of the VCO is measured and histogrammed with the modulation domain analyzer. The VCO frequency divided by the input clock frequency are plotted in Fig. 12. The error bar indicated in the figure is the standard deviation of the histogram data; it comprises a measurement error and a spread of frequencies. The measurement error of the time interval is about 70 ps. Thus, the error at the high-frequency side mainly comes from the measurement error, and the error at the low-frequency side mainly comes from the spread of the frequency.

From the figure, the PLL circuit tracks for the frequency range between 10 MHz to 50 MHz at supply voltage of 3.3 V. At a frequency of less than 5 MHz, although the center value of the frequency of the VCO circuit is still tracking the input clock frequency, the distribution of the time interval becomes spread. In the extreme case two time intervals appear (short and long interval), since the delay characteristic is not stable at this speed (Fig. 7).

We can also see from the figure that the PLL is stable for a voltage variation of 3.0 to 3.6 V from 10 MHz to 50 MHz.

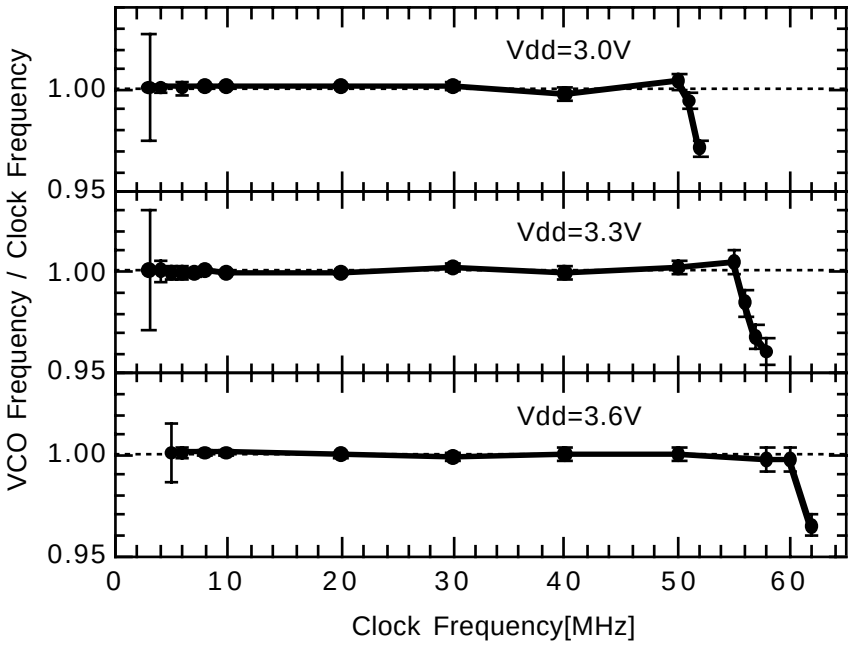

Fig. 12. PLL tracking range measurements for Vdd = 3.0, 3.3 and 3.6 V. The error at the high-frequency side comes from a measurement error, while the error at the low-frequency side comes from the spread of the time interval.

D. PLL Step Response

The step response of the PLL circuit is measured using a 4 GHz timing logic analyzer. The output of the VCO is recorded after resetting the PLL circuit. The measured wave form is converted into frequency and is plotted in Fig. 13 for 100 pF and 1000 pF capacitors in the loop filter. The frequency becomes stable in 4 μsec for both cases. The PLL is unstable for a capacitance of less than 20 pF.

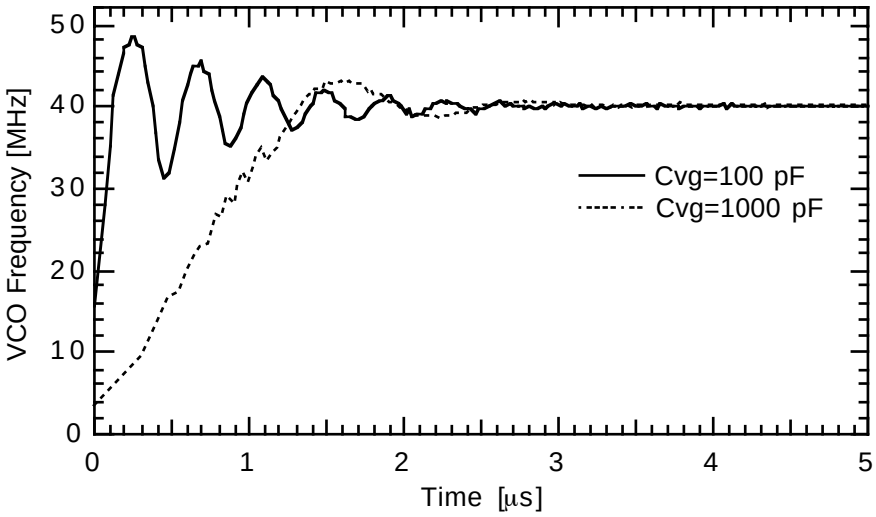

Fig. 13. PLL response-time measurement for external capacitances (Cvg) of 100 pF and 1000 pF.

E. Power consumption

The power consumption depends on the conditions of the clock frequency, input signal rate, and readout rate. At 40 MHz, the power consumption is about 21 mW/channel when data recording to the memory is not done while the ring oscillator is running. When the chip starts recording, the power consumption increases to about 29 mW. If an input signal of 1 MHz is applied, the power consumption increases by an additional 16 mW.

For our most severe condition (continuous recording, input rate of 1 MHz, and trigger rate of 100 kHz) the total power consumption becomes about 200 mW/chip. Since our detector system is very complicated, it is relatively hard to implement elaborated cooling system for the electronics. The power consumption of the TMC-TEG3 is low enough and can be cooled by air. Although the power consumption increased from the previous TMC1004, it is sufficiently low compared with using high-speed shift registers.

V. TIMING ACCURACY

Fig. 10 also shows a plot of an ideal time distribution; the distribution function, $P(x)$, can be expressed as

$$P(x) = \begin{cases} 1/L & |x| \le L/2 \\ 0 & |x| > L/2 \end{cases} ,$$

where L is the bit width and the function is normalized to have a unit area. Assuming a Gausssian distribution, $G(x,\mu,\sigma)$, for the various components of the timing error, such as jitter and non-uniformity of the delay elements, the actual distribution function, $F(x,\sigma)$, is expressed as a smeared plot of $P(x)$ with $G(x,\mu,\sigma)$

$$\begin{aligned} F(x,\sigma) &= \int_{-\infty}^{\infty} G(x,\mu,\sigma)\cdot P(\mu)\cdot d\mu \\ &= \frac{1}{L\cdot\sigma\cdot\sqrt{2\pi}}\int_{-L/2}^{L/2}\exp\left(-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2\right)d\mu \\ &= -\frac{1}{2L}\left(erf\left(\frac{x-L/2}{\sigma\sqrt{2}}\right)-erf\left(\frac{x+L/2}{\sigma\sqrt{2}}\right)\right) , \end{aligned}$$

where x is the deviation from the ideal line, μ and σ are the central value and the standard deviation of the Gaussian distribution, and erf(z) is an error function

$$erf(z) = \frac{2}{\pi}\int_0^z e^{-t^2}dt .$$

We fit the data shown in Fig. 10 with the $F(x,\sigma)$ multiplying a normalization factor. The fitted curve is also shown in Fig. 10; we obtained a σ of 104 ps as the timing error.

To estimate the source of the error, we also measured the jitter of the input clock and VCO output with a oscilloscope which can make a histogram of time jitter and analyze it statistically. We measured a jitter of 30 ps and 13 ps for the input clock and VCO output, respectively. As shown in previous

section, the differential and integral nonlinearity errors contribute 24ps and 36ps to the timing error, respectively. The time-to-digital conversion stages also contribute to the error; noise on the WOUT and TIN line causes an error in the time measurement. We estimate that this error could be around 40 ps. A further analysis of the error is required to obtain a better timing resolution.

VI. SUMMARY

A pipeline time-to-digital converter chip (TMC-TEG3), has been successfully designed and fabricated by using a 0.5 μm CMOS gate-array. To implement a high-resolution TDC in a commercial gate-array, an asymmetric ring oscillator controlled by a PLL has been developed. The oscillator generates 32 equally spaced precise timing signals. The digitized data are pipelined to an encoder and a dual-port memory. A time resolution of 250 ps rms is measured at 40 MHz clock. The chip contains 4 channels and consumes less than 200 mW under high-rate conditions.

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