TMC-VME

32Ch TMC-VME Module

User Manual

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Y. Arai and M. Ikeno

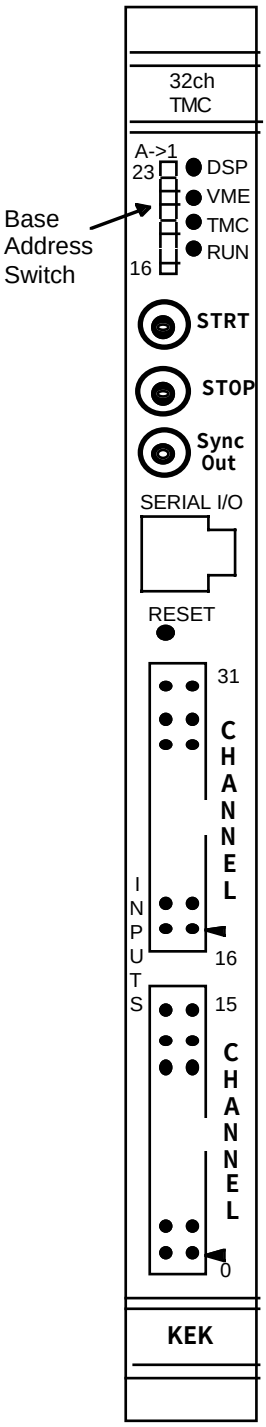
KEK, National High Energy Accelerator Research Organization
Institute of Particle and Nuclear Studies
1-1 Oho, Tsukuba, Ibaraki 305, Japan
Tel : 81-298-64-5366
Fax : 81-298-64-2580
yasuo.arai@kek.jp

and

H. Shirasu and T. Emura

Tokyo University of Agriculture and Technology
1-24-16 Nakamachi, Koganei, Tokyo 184, Japan
Tel : 81-423-81-4221
Fax : 81-423-85-6255

(see also http://atlas.kek.jp/~araiy/)



32-ch 6U TMC-VME Module

- 32 channels in Double-height, Single-width VME module
- 0.7ns / bit least count, sigma = 250 ps time resolution
- > 3 usec Full Scale
- Common stop/start operation
- on-board DSP56002
- Serial I/F to DSP
- Rising/Falling edge detection and 6 bit encoded data
- Stable operation for temperature, voltage variation
- VME Slave module (Dual Port Memory & Host I/F)
- ECL differential input for signal
- NIM level start / stop signal input
- NIM level trigger output

(This front-panel drawing is not scaled.)

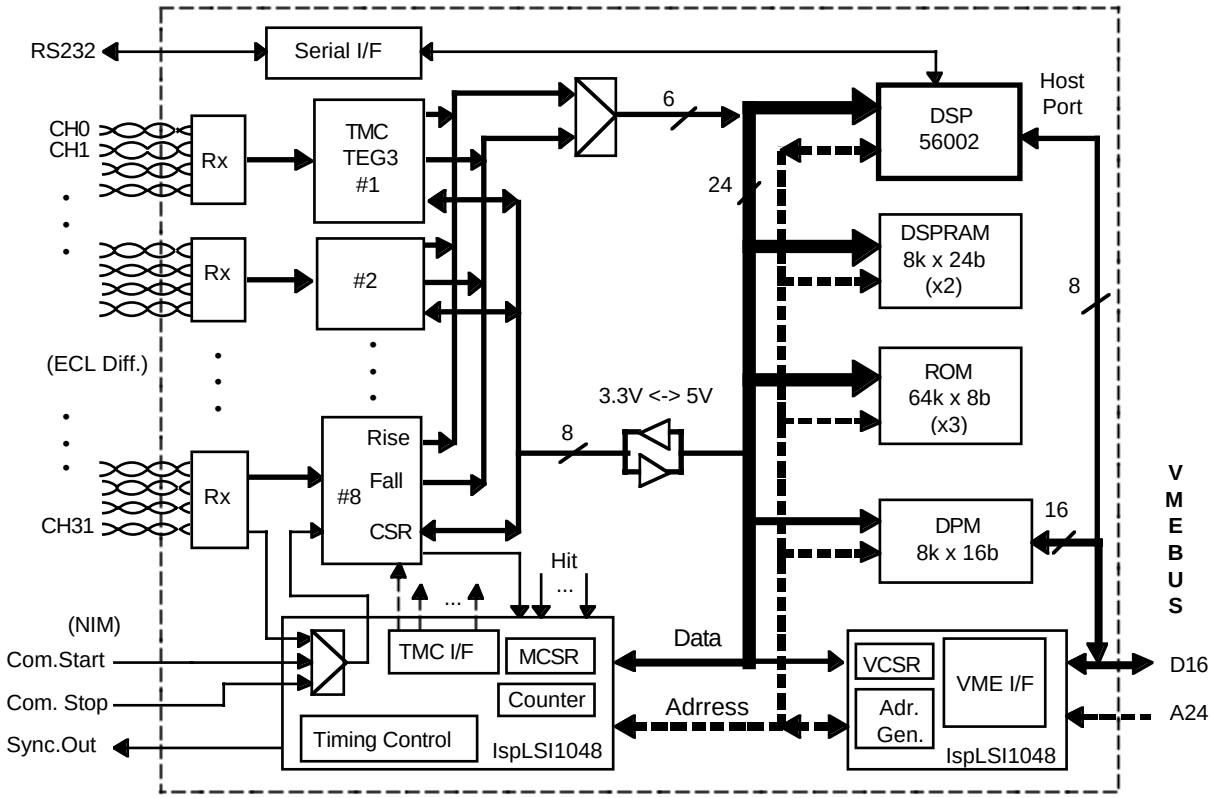


Fig. 1 Block diagram of the 32ch TMC-VME module.

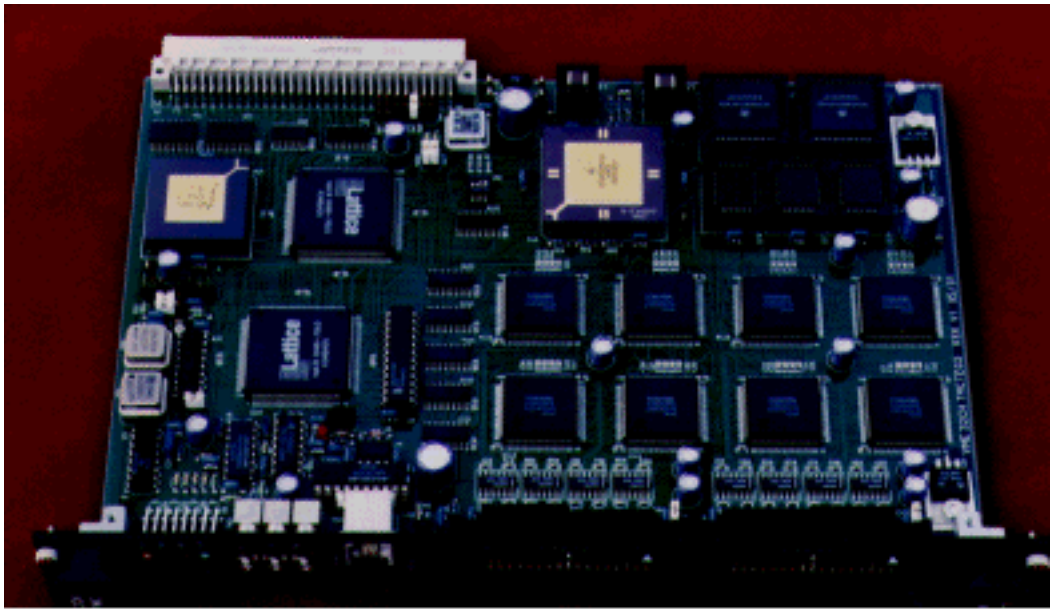


Fig. 2 Photograph of the module.

Specifications

Signal Inputs :	32 Channel. ECL-differential (or differential signal of amplitude > Δ100mV, common voltage range of ±3V). Input Impedance 100 Ω. Two 34-pin Flat Cable Connectors.
START Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Start mode.
STOP Input :	One, common to all channels, 50 Ω impedance; Lemo-type connector; NIM level. Used in common Stop mode.
SYNC Output :	Lemo-type connector; NIM level. Generate synchronous output pulse with internal clock at start/stop time. Used for test purpose.
Least Time Count :	0.63 - 3.1ns/bit (@ 50 - 10 MHz) nominal 0.78 ns (@ 40 MHz)
Time Range :	2.56 - 12.8 μsec (@ 50 - 10 MHz) nominal 3.2 μsec (@ 40 MHz)
Double Hit Resolution :	25 ns (@ 40 MHz)
Time Resolution :	Single Hit : σ = 262 ps (@ 40 MHz) Time difference: σ = 370 ps (@ 40 MHz)
Integral Linearity Error :	< 0.1 LSB
Differential Linearity :	< 0.1 LSB
Serai Interface :	RS-232C (Front panel). RJ-11 connector.
Host Interface :	8-bit DSP Host Interface through VME bus.
VME I/F :	P1 connector. A24/D16 (BLK). Base address (A23..A16). Single word transfer(AM=$29,$2D,$39..$3F), and Block Transffer(AM=$3B,$3F) are supported. Interrupt from(to) the DSP to(from) a VME master.
DSP :	24 bit DSP (DSP56002) (@ 40 MHz) 16k x 24b RAM, 64kB x 3 ROM, 8k x 16bit Dual Port Memory
Packaging :	Double height (6U), Single width VME module.
Power Requirement :	+5 V x 1.4 A, -12 V x 0.16 A, < 8 W

Front Panel LED's

There are 4 LED's in the front panel.

DSP : This LED is connected to DSP PS signal. Thus this LED become On when the DSP access to program space address.

VME : This LED is connected to VME module select signal. When the VME address [A23..A16] coincide to the module base address with proper address modifier, this LED becomes ON. The circuit contains 74LS123 one-shot multi vibrator so that user can recognize the access.

TMC : This LED become ON when the TMC is running. Normally TMC need running before real measurement.

RUN : This LED indicate the module is measuring signal.

In common start mode, when the module is ready for measurement and waiting start signal, the TMC lED is ON and the RUN lED is OFF. When the start signal come, the RUN LED flash very shortly (maybe you can not recognize) until preset count is over.

In common stop mode, when the module is ready for measurement and waiting stop signal, both the TMC & RUN LEDs are ON. When the stop signal come, the RUN LED becomes OFF.

When a measurement finishes, the TMC LED becomes OFF, but shortly becomes ON if the TMC is ready for next measurement. If the dual port memory of the module contains an event and next event is recorded in the TMC, the TMC LED becomes OFF until the event is read out. This means the TMC module has double buffer.

There is one additional LED inside module. This LED is used for debug purpose, and controlled through module CSR bit 2.

Input Connector Pin Assignment

Lower Connector

Pin No.	Assignment	Pin No.	Assignment
1	GND(*)	2	GND(*)
3	Ch 0 +	4	Ch 0 -
5	Ch 1 +	6	Ch 1 -
7	Ch 2 +	8	Ch 2 -
9	Ch 3 +	10	Ch 3 -
11	Ch 4 +	12	Ch 4 -
13	Ch 5 +	14	Ch 5 -
15	Ch 6 +	16	Ch 6 -
17	Ch 7 +	18	Ch 7 -
19	Ch 8 +	20	Ch 8 -
21	Ch 9 +	22	Ch 9 -
23	Ch 10 +	24	Ch 10 -
25	Ch 11 +	26	Ch 11 -
27	Ch 12 +	28	Ch 12 -
29	Ch 13 +	30	Ch 13 -
31	Ch 14 +	32	Ch 14 -
33	Ch 15 +	34	Ch 15 -

Upper Connector

Pin No.	Assignment	Pin No.	Assignment
1	GND(*)	2	GND(*)
3	Ch 16 +	4	Ch 16 -
5	Ch 17 +	6	Ch 17 -
7	Ch 18 +	8	Ch 18 -
9	Ch 19 +	10	Ch 19 -
11	Ch 20 +	12	Ch 20 -
13	Ch 21 +	14	Ch 21 -
15	Ch 22 +	16	Ch 22 -
17	Ch 23 +	18	Ch 23 -
19	Ch 24 +	20	Ch 24 -
21	Ch 25 +	22	Ch 25 -
23	Ch 26 +	24	Ch 26 -
25	Ch 27 +	26	Ch 27 -
27	Ch 28 +	28	Ch 28 -
29	Ch 29 +	30	Ch 29 -
31	Ch 30 +	32	Ch 30 -
33	Ch 31 +	34	Ch 31 -

(*) can be disconnected from GND by jumper pins.

Backplane Connector Pin Assignment

P1 : VME Bus

Pin	ROW A	ROW B	ROW C
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	(BG0IN*)	D11
5	D04	(BG0OUT*)	D12
6	D05	(BG1IN*)	D13
7	D06	(BG1OUT*)	D14
8	D07	(BG2IN*)	D15
9	GND	(BG2OUT*)	GND
10	(SYSCLK)	(BG3IN*)	(SYSFAIL*)
11	GND	(BG3OUT*)	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	(+5 V STDBY)	(+12 V)
32	+5 V	+5 V	+5 V

( ) --- signal not used in this module.

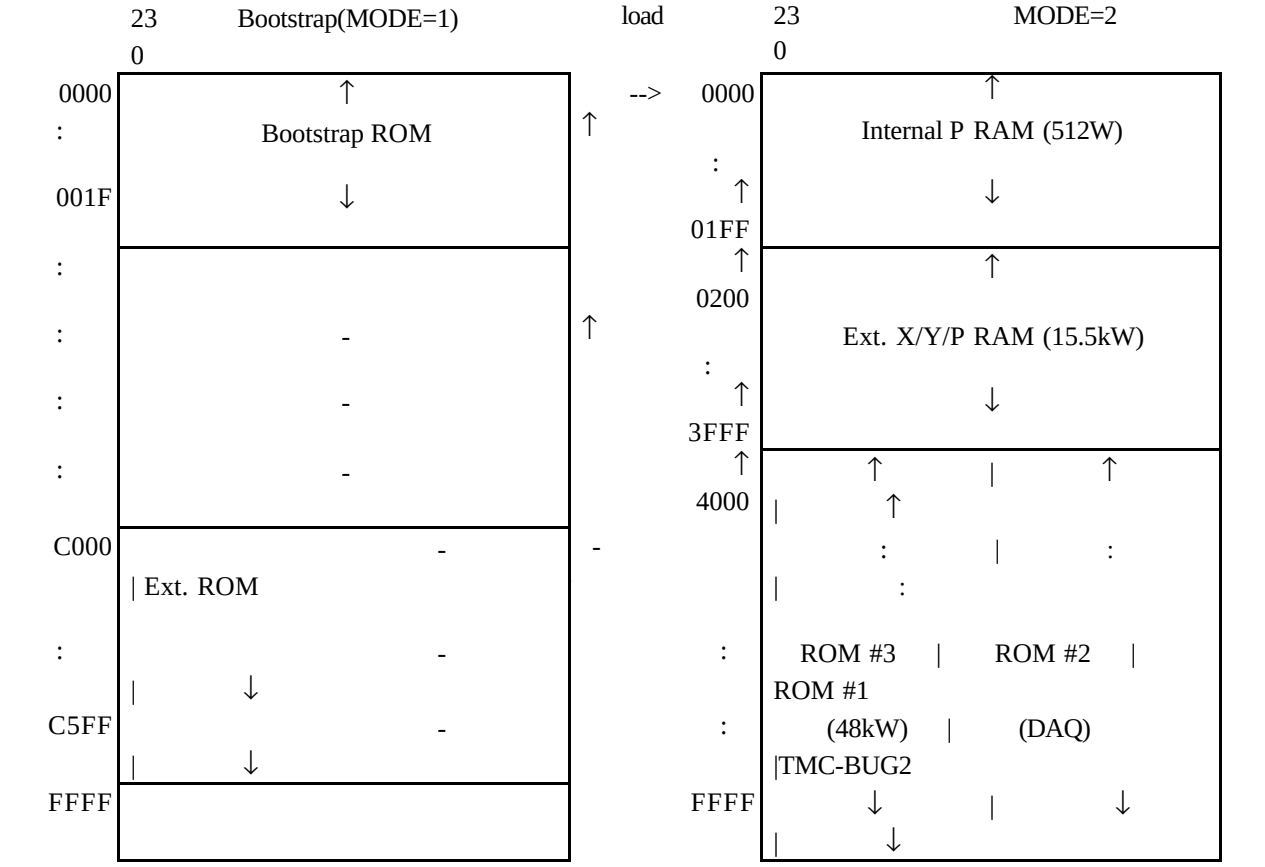
RS-232C Serial Port Pin Assignment

	Modular Jack			
SW14, 15	pin 1, 6	Pin 2,5	Pin 3	Pin4
Both Down	not used	GND	Rx	Tx
Both Up	not used	GND	TX	Rx

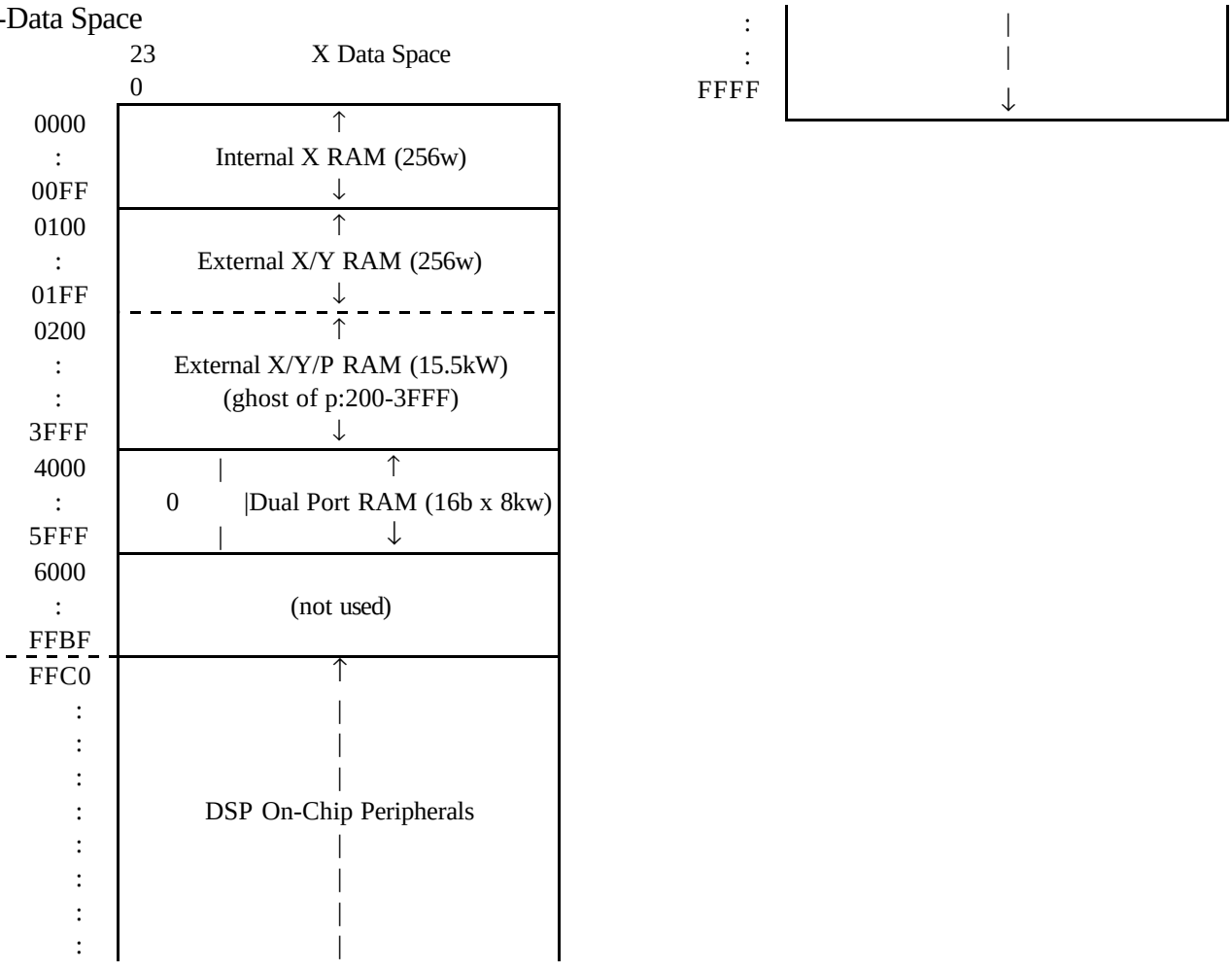
(Default setting: 9600 baud, 8 bit, No parity, XON/XOFF control)

DSP Space Address Map

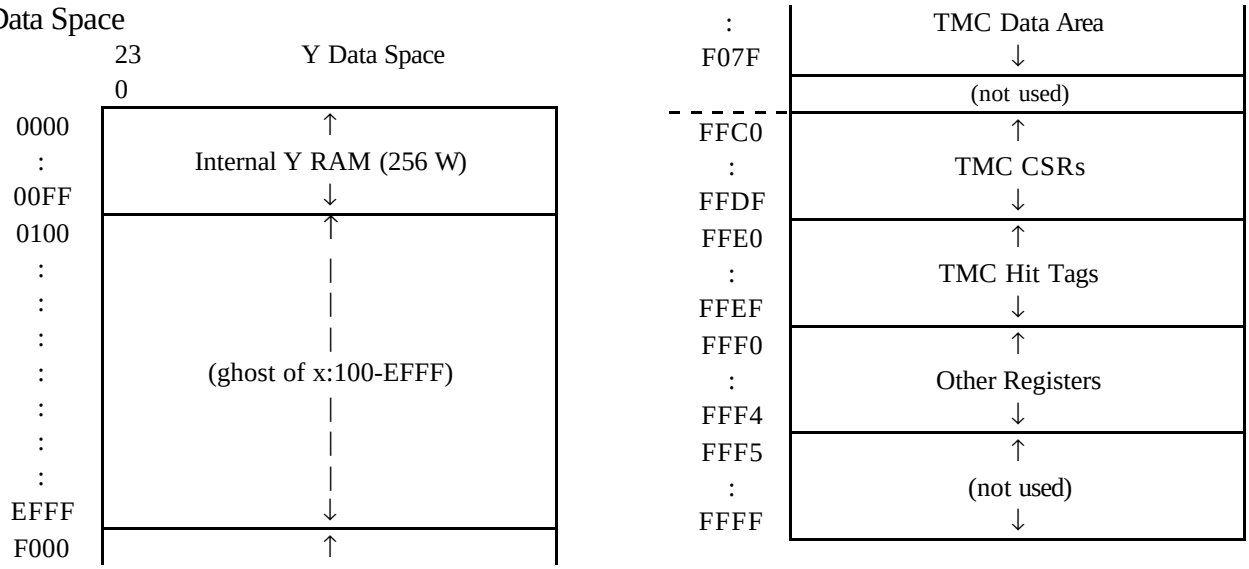
Program Space



X-Data Space



Y-Data Space



[minimum DSP wait cycles] X/P-memory = 0, Y=1, IO = 1 and ROM-access = 4.
(*) TMCBUG2 uses P:0-$80 and P:1300-1FFF.

TMC Data Address Assignment (X/Y-Space)

address	23 ... 8	7	6	5	4	3	2	1	0	name
F000	0	RTAG0	0	Ch0 Rising Edge Time						RDATA0
F001	0	FTAG0	0	Ch0 Falling Edge Time						FDATA0
F002	0	RTAG1	0	Ch1 Rising Edge Time						RDATA1
F003	0	FTAG1	0	Ch1 Falling Edge Time						FDATA1
:	0			:						
F03E	0	RTAG31	0	Ch31 Rising Edge Time						RDATA31
F03F	0	FTAG31	0	Ch31 Falling Edge Time						FDATA31
F040	0			Ch0 Rising Edge Time(†)						RDAT0
F041	0			Ch0 Falling Edge Time(†)						FDAT0
F042	0			Ch1 Rising Edge Time(†)						RDAT1
F043	0			Ch1 Falling Edge Time(†)						FDAT1
:	0			:						
F07E	0			Ch31 Rising Edge Time(†)						RDAT31
F07F	0			Ch31 Falling Edge Time(†)						FDAT31

External IO Space Assignment

address	23 ... 8	7	6	5	4	3	2	1	0	name
FFC0	0	Chip 0 CSR0* (†††)								CSR00
:	0	:								
FFC7	0	Chip 7 CSR0* (†††)								CSR07
FFC8	0	Chip 0 CSR1* (†††)								CSR10
:	0	:								
FFCF	0	Chip 7 CSR1* (†††)								CSR17
FFD0	0	Chip 0 CSR2* (†††)								CSR20
:	0	:								
FFD7	0	Chip 7 CSR2* (†††)								CSR27
FFD8	0	Chip 0 CSR3* (†††)								CSR30
:	0	:								
FFDF	0	Chip 7 CSR3* (†††)								CSR37
FFE0	0	FTAG3	RTAG3	FTAG2	RTAG2	FTAG1	RTAG1	FTAG0	RTAG0	TAGA0
:		:								
FFE7	0	FTAG31	RTAG31	FTAG30	RTAG30	FTAG29	RTAG29	FTAG28	RTAG28	TAGA7
FFE8	0 (†)	FTAG3	RTAG3	FTAG2	RTAG2	FTAG1	RTAG1	FTAG0	RTAG0	TAG0
:		:								
FFEF	0 (†)	FTAG31	RTAG31	FTAG30	RTAG30	FTAG29	RTAG29	FTAG28	RTAG28	TAG7
FFF0	0	Stop Counter								CNTR
FFF1	0	Module CSR								MCSR
FFF2	0	VME CSR								VCSR
FFF3-F	(not used)									

(†) The RCLK signal is not asserted for these registers (RDAT0..31 and FDAT0..31). Data are latched in output buffer with RCLK signal, so the data are old ones which are latched by last RCLK. When accessing other registers, such as RDATA0..31, FDATA0..31, TAGR0..7 and TAGF0..7, RCLK will be asserted.

(††) TMC Read Pointer is automaticaly incremented with RCLK when ENRPUP bit of CSR0 is set in MODE=2 or 3.

(†††) Data of the CSR00-CSR37 are negative logic value of the TMC CSR registers.

Module CSR(MCSR) Bit Assignment

Bit	Name	R/W	Common stop mode (COMST=0)	Common start mode (COMST=1)
0	MODSW1	R	Mode Switch 1 Status.	
1	MODSW2	R	Mode Switch 2 Status. (V2.0 or later board only)	
	(TRST)	W	TMC Reset (same as bit 7 except Latched)	
2	DBGLED	R/W	Debug LED	
3	TMC	R/W	Start TMC (=TMC LED)	
4	DSTART	R	Running (= RUN LED)	
		W	-	Internal Common Start Signal †
5	DSTOP	R	Stop Running	
		W	Internal Common Stop Signal †	-
6	COMST	R/W	Common Start (=1), Common STOP (=0) mode.	
7	TRST	R	0	
		W	TMC Reset†	

(†) These signals are not latched.

Address Map (VME Space)

Single word transfer(AM=$29,$2D,$39..$3F), and Block Transffer (AM=$3E,$3F).

DSP Addr	VME Addr	15 Upper byte 8 7 Lower byte 0	addr. symbol
$4000	x+0	Dual Port Memory (16 kB)	DPM
:	:		
$5FFF	x+3FFE		DPME
	x+4000	↑	
	:	(not used)	
	x+FF00	↓	
	x+FF02	0 | Interrupt Level | Interrupt Vector	INTR
$FFF2	x+FF04	0 | VME CSR .	VCSR
	x+FF06	↑	
	:	(not used)	
	x+FFEE	↓	
	x+FFF0	| Interrupt Control Register	ICR
	x+FFF2	| Command Vector Register	CVR
	x+FFF4	| Interrupt Status Register	ISR
	x+FFF6	(Host Port) | Interrupt Vector Register	IVR
	x+FFF8	| -	
	x+FFFA	| Rx/Tx Byte Register H	RXH/TXH
	x+FFFC	| Rx/Tx Byte Register M	RXM/TXM
	x+FFFE	| Rx/Tx Byte Register L	RXL/TXL

x = 0, $10000, $20000, ..., $FF0000 (upper 8 bit base address is switch selectable)

VME CSR(VCSR) Bit Assignment

Bit	from DSP	from VME	Contents	Name
0	R W	R W	0 Module Reset (no latch)	MRST
1	R/W	R/W	INTM Interrupt Status	INTM
2	R/W	R/w	INTM Interrupt Enable	INTMEN
3-15	R	R	0	

TMC CSR Registers

TMC CSR registers bit assignment

bit	7	6	5	4	3	2	1	0
CSR0	SHIFT (R/W:0)	MTEST (R/W:0)	**NRPSYN** (R/W:0)	**ENRPUP** (R/W:0)	- (R/W:0)	TCH (R/W:0)	TCH0 (R/W:0)	F/R* (R/W:0)
CSR1	0	**Read Pointer register [RPR]** (R/W:0)						
CSR2	0	**Write Pointer Register [WPR]** (R/W:0)						
CSR3	SOUT (R:0)	SIN (R/W:0)	Test Data Register [TDR] (R/W:0)					

(R/W: x) --- (Readable/Writeable: Initial value)

* CSR0 : Miscellaneous control.

- NRPSYN [read/write]: Disable synchronous count up of the read pointer with write pointer. When NRPSYN="0", the read pointer is incremented synchronous to the system clock when write cycle started. If the NRPSYN="1", this automatic count up is inhibited.
- ENRPUP [read/write] : Enable automatic count up of the read pointer after asynchronous readout. When ENRPUP="1" and in asynchronous read mode (RMODE=2 or 3), the read pointer is incremented after negation of the RCLK.
- F/R* [read/write]: Test data select, =0 rising edge, =1 falling edge.
- TCH0~1 [read/write]: Test channel select. TCH = [TCH1,TCH0].
- MTEST : Memory Test select. When this bit is set, output of the Test Data Register (TDR) is connected to the input of the DPM and the input of TDR is connected to the output of encoder logic selected by TCH bits and F/R* bit.
- SHIFT : Enable Shift In/Out. When this bit is set, the value of the SIN bit is shifted into the encode register which is selected by CH bits at the end of CSR3 read/write operation.[read/write]

* CSR1 : Read Pointer Register

- RPR [read/write]: Read Pointer Register. This is a 7-bit loadable up-counter which outputs are connected to the read addresses of the Dual Port Memory (DPM). The read pointer is set through this register and read back present value of the read pointer.

* CSR2 : Write Pointer Register

- WPR [read/write]: Write Pointer Register. This is a 7-bit up loadable up-counter which outputs are connected to the write addresses of the Dual Port Memory (DPM). The write pointer is set through this register and read back present value of the write pointer.

* CSR3 : Test Data Register

- TDR [read/write]: Test Data Register.
- SIN [read/write] : Serial Input bit.
- SOUT [read only] : Serial output bit.

Jumper Switch Settings [ ] -- default setting

• SW1 : Interrupt level switch. (bit 1-3, bit 4 is not used). Select same interupt level as in the SW4. [1]

• SW2 : Rest switch.

• SW3 : 8-bit base address switch.[00000001 = $01xxxx]

• SW4, 5, 6, 7, 8, 9, 10 : Interrupt request level setting. Insert a jumper in one of these position as shown below, and select same interrupt level as in the SW1. [IRQ1, SW4]

VME IRQ Level	SW1[bit 3,2,1]	SW4, 5, 6, 7, 8, 9, 10
IRQ1	[0,0,1]	Insert a jumper in SW4
IRQ2	[0,1,0]	Insert a jumper in SW8
IRQ3	[0,1,1]	Insert a jumper in SW5
IRQ4	[1,0,0]	Insert a jumper in SW9
IRQ5	[1,0,1]	Insert a jumper in SW6
IRQ6	[1,1,0]	Insert a jumper in SW10
IRQ7	[1,1,1]	Insert a jumper in SW7

• SW11 : Mode switch 1. Down=0 (run 'DAQ6U' program), Up=1(run 'TMCBUG'). [Down]

• SW12 : ispLSI SDO/Clock selection. Down=40MHz Clock, Up=SDO.[Up]

• SW13 : ispLSI programming chip selection. Down=TMC I/F chip, Up=VME I/F chip.[Up or Down]

• SW14, 15 : Serial communication Receive/Transmit signal setting. Please set both jumpers in same position. [UP or Down]

	Modular Jack			
SW14, 15	pin 1, 6	Pin 2,5	Pin 3	Pin4
Both Down	not used	GND	Rx	Tx
Both Up	not used	GND	TX	Rx

• SW16 : Reserv 0 and 2 connection.(not used)

• SW17 : Reserv 1 and 3 connection.(not used)

• SW18 : Ch0-15 connector GND connection. [Connected]

• SW19 : Ch16-31 connector GND connection. [Connected]

• SW20 : TMC clock selection. Right (down ††) =from OS3 (optional), Left (up ††)= DSP clock from OS1 divided by 2 (40MHz). [Left]

• SW21(†) : Mode Switch 2. Down =1, Up = 0. [Down]

• SW22(†) : Enable TMC Ring Oscillation check. Close = output the clock from test pad, Open = disable. [Open]

(†) --- Version 2 or later module.
(††) --- Version 1 module

Fuse

• Fuse T1 : -12 V power, 1A fuse.

• Fuse T2 : 5V power, 10A fuse.

ispLSI Download pin

• Pin1=SCLK, Pin2=GND, Pin3=MODE, Pin4=(plug), Pin5=ispEN*, Pin6=SDI, Pin7=SDO, Pin8=Vcc.

ROM

• IC18 : ROM bit 0 - 7 (DSPBUG2)

• IC17 : ROM bit 8-15 (ROM2: DAQ6U, etc.)

• IC16 : ROM bit 16-23.(user)