LOI Progress Report

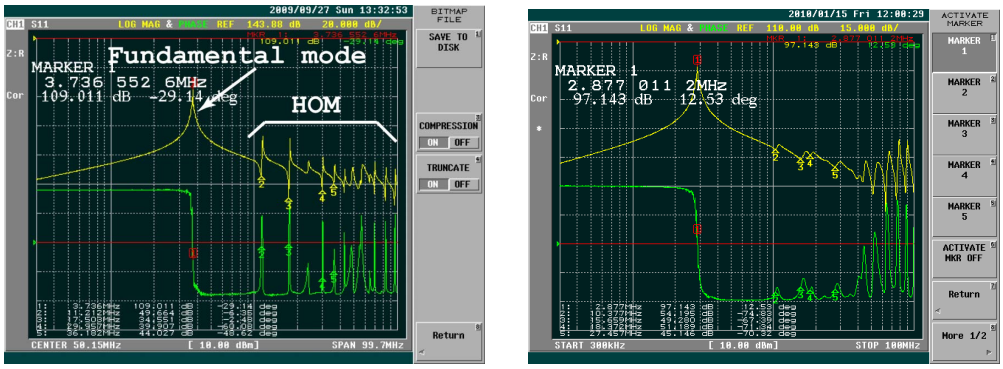
-- Summary of Experiment in January 2010 --

February 18, 2010

1. Introduction

Following the previous experiments in October, 2009, a new method to improve the RF waveform distortions was investigated. The anode and feedback chokes are provided with higher-order-mode (HOM) dampers in the new method (fig. 1). Waveforms below 4MHz were then slightly improved. However, waveforms at higher frequencies remained similar, ie. sub-harmonic distortions are still large. Optimization of the bias feedback loop started in January 22, and continued until the last day of the experiment. However, optimization in a whole frequency range could not be completed due to time shortage. The system ran very stable, except for several trips due to the mistuning of the bias feedback loop and the water leakage of the cavity cooling system.

In the following sections are reported, experimental setup in section 2, experimental results in section 3, short pulse excitation in section 4, faults and remedies in section 5, and conclusions in section 6. Supplementary data are given in the appendix.



(a) (b)

Fig.1 Isolated measurement of the final anode choke impedance (a) without and (b) with the HOM damper. HOMs lower than 50MHz are well damped by the damper, although they are rather enhanced above that. (see text in section 2.)

2. Experimental setup

In the previous experiments, the location of HOM peak in the final and driver anode chokes was slightly shifted with each other by shorting few turns of coil at one end [1]. In this experiment, anode choke and feedback coils are provided with an HOM damper circuit which comprises few-turn secondary windings at each end with termination resistor R~280ohms. Fig. 2 shows the skeleton and the photo of the final anode choke with a damper. The choke impedance of isolated measurement is shown in Fig. 1, where the choke is set apart from its original position in the HPD chassis. HOMs lower than 50MHz are well damped, although above that they are rather enhanced. The driver anode choke has the same damper structure with the final one having 2-turn secondary windings. The feedback coil has a short (N2=11) at one end and 4-turn secondary windings at the other. The experiments were performed for three cases where the damper is attached to (1) only the final anode choke, (2) both final and driver anode chokes, and (c) these two anode chokes and the feedback coil.

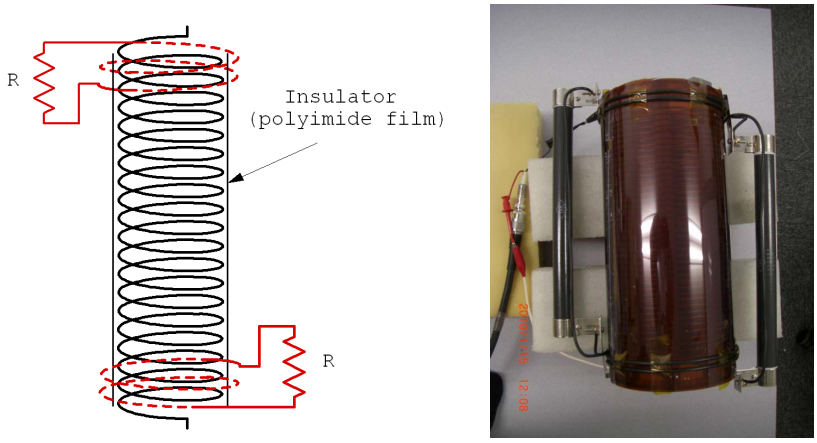


Fig. 2

Because of the feedback impedance (Zf) between plate and grid in the final triode, phase relation of the grid and plate voltages is NOT 180 deg. out of phase even when the cavity is tuned at its resonance (fig. 3). In order to compensate for this effect and the possible difference of the monitor cable lengths, the offset signal is added at the 'Δϕ offset' input of the phase detector. Optimization of the bias feedback loop is to find the optimum function of 'Δϕ offset' over the whole frequency range so as to keep the cavity input current at minimum value. It should be reminded, however, that the output current of the final triode is not the cavity input current in fig. 3, because part of the output current flows through the anode choke coil. From the power-saving point of view, the anode choke coil should be incorporated into the cavity resonant circuit. However at present, the choke current is not dominant, fortunately, comparing with the cavity input current as described in section 3. It is interesting to put another current probe at the filament side of the triode, and to observe the total output current.

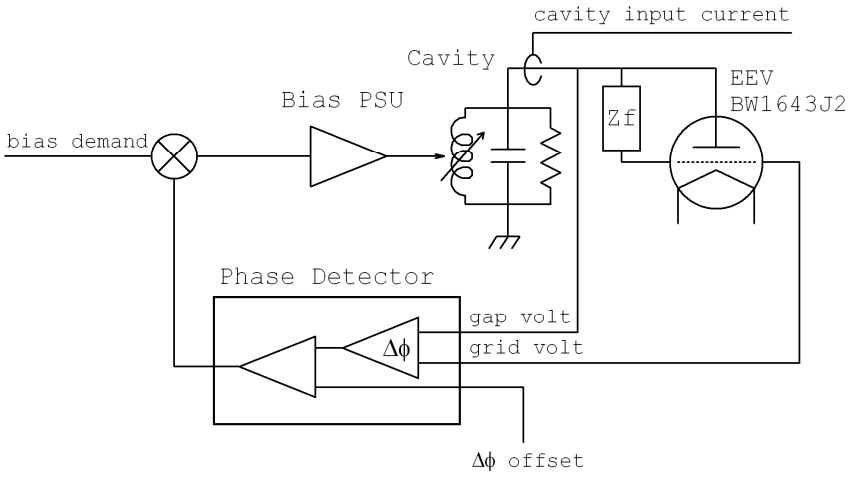


Fig. 3 Bias feedback loop

Amplitude modulation of the RF_law signal has a trapezoidal shape as shown in fig. 4. The automatic voltage control (AVC) loop is not applied yet.

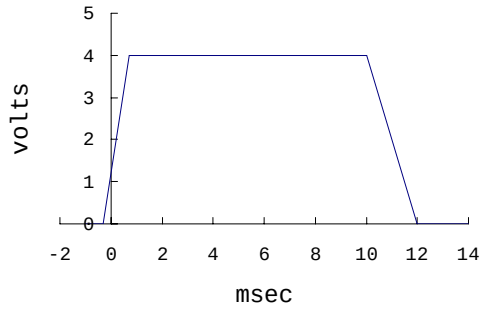


Fig. 4 Amplitude modulation to the RF_law signal.

3. Experimental results

It was expected that the waveform distortions would be much improved by using the new coils discussed above. However, waveforms were rather similar to those in the previous experiments: sub-harmonic distortions can be seen at higher frequencies. Fig. 5 shows typical waveforms, where the driver and final anode chokes are provided with dampers. It was confirmed that there is not so much difference in waveform distortions among three cases for damper arrangements.

Optimization of bias feedback loop was performed through trimming the $\Delta\phi$ offset, and it was mostly concentrated on the time range t<1msec, where the cavity input current appears highest. The offset function then showed a zigzag shape at t<1msec, peaking at ~2volts. However, at the end of the day during shutdown process, the bias power supply was found tripped by the 'over current'. We thought such a zigzag shape would be a reason for the trip (1/27). We then changed the optimization method from use of $\Delta\phi$ offset to trimming the bias demand hereafter. It was observed that the bump in the triode output current in fig. 5 decreased when the cavity gap-input current is minimized.

It is seen in fig. 5 the grid input currents are very sinusoidal (, although we do not know the reason!). We have tried to use this signal for input of the phase detector instead of grid volt. However, due to time shortage, this method was not fully investigated.

Day-by-day summary of this experiment is given in Table 1.

Fig. 6 shows the voltage gain of the final triode, which is defined as the ratio of the output voltage to the grid-input voltage. Each voltage was measured by simply using the function of the oscilloscope, "measure/amplitude peak-to-peak". Therefore, the gain curve over 4.5MHz where waveform distortions are significant is not correct. Calculated gain is also shown for comparison [2].

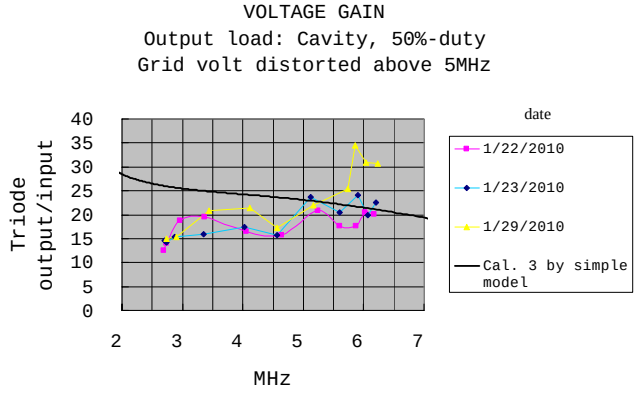


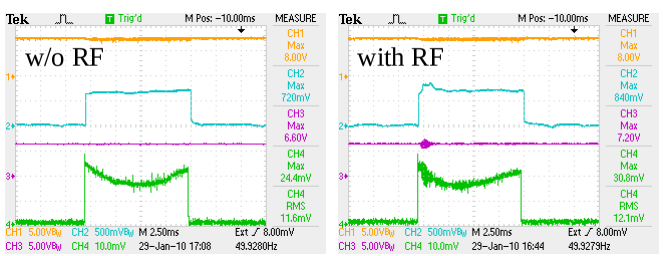
Fig. 6 Voltage gain of final triode

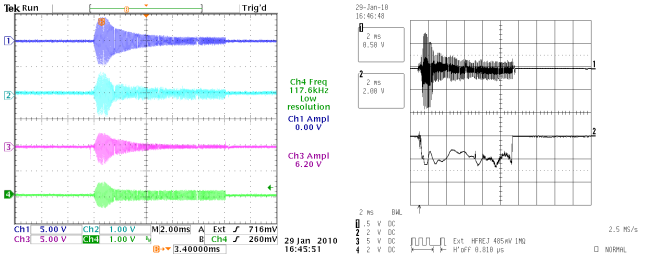
January 29, 2010

Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, trimming bias demand, phase detector offset=~0 volts.

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).





Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

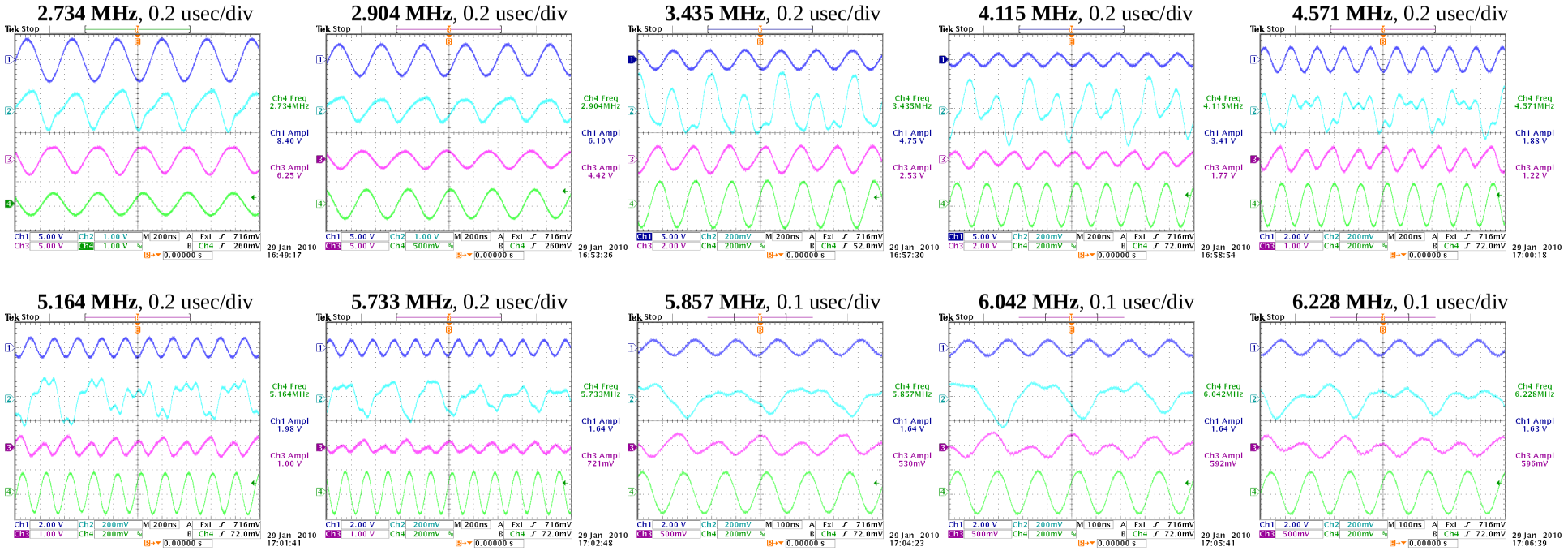


Fig. 5 RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

4. Short pulse excitation

In order to see the higher frequency components excited by a short pulse, a pulse with less than 1 usec width was fed at the input of 300W solid-state amplifier. The pulse was synchronized to the ISIS 50Hz and located ~7msec after the start of tetrode anode current. Figures 7 and 8 show the short pulse and its timing location relative to the tetrode anode current. The bias current to the cavity was set to 0 A, which corresponds to the cavity resonant frequency of ~2MHz.

Transients associated with the pulse are shown in fig. 9, where~190KHz and ~2.5MHz components can be seen. Although the cut-off frequency of the all-pass-network at the tetrode input is 16MHz [3], the ~20MHz component is slightly seen. The 2.5MHz component may cause a sub-harmonic distortion to the 5MHz waveform.

It is worth applying this method at each timing over the whole acceleration cycle to observe what sort of harmonics is excited.

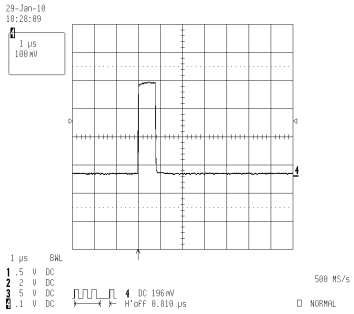


Fig.7 Short pulse

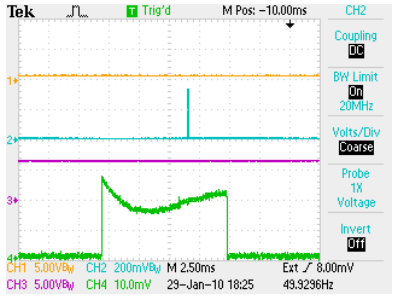


Fig. 8 Short pulse (2nd trace) and tetrode plate current (bottom trace)

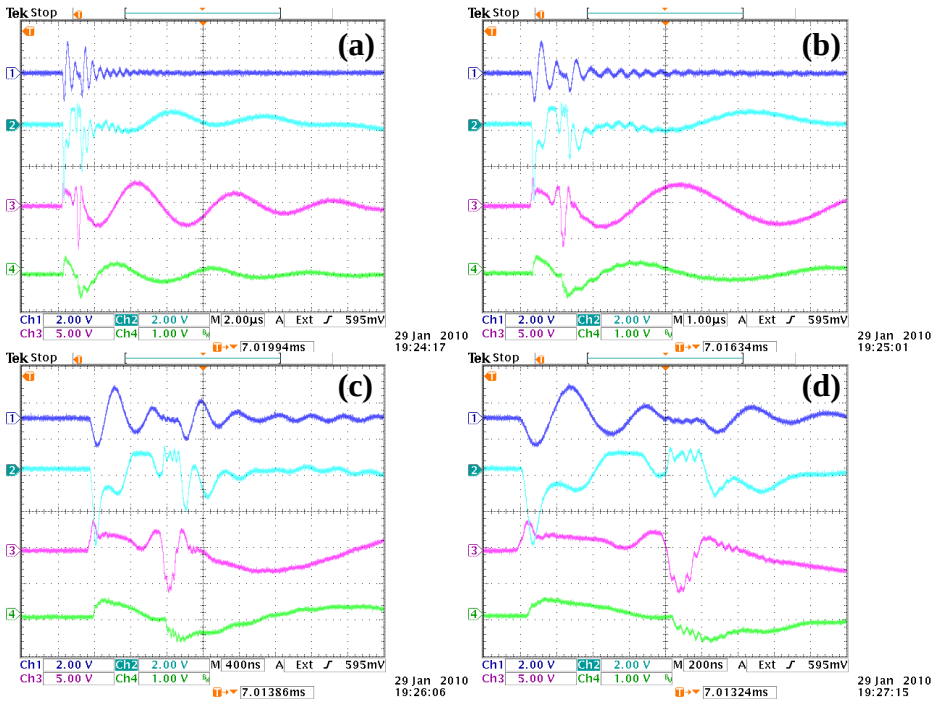


Fig. 9 Transient waveforms with 2nd Harmonic Cavity at dc bias with (a) 2usec/div, (b) 1usec/div, (c) 0.4usec/div and (d) 0.2usec/div. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

5. Faults and remedies

Faults and incomplete interlocks were found during the experiments. Remedies or temporary measures are summarized below, including the pending problems in the past.

(1) Grid-switcher fan (1/19/2010)
Current fan was also found failed. Two fans were replaced with new ones.
(2) AC lead of a triode heater supply was blown at the fuse box (8/21/ 2008).
Replaced with a larger-size lead and screwed tightly (1/20/2010).
(3) "Conductivity" of the liquid resistor was shorted at TB1 of the water manifold box. (10/14/2009)
This was linked to "FL6" interlock, but not working.
(4) BR trip level was changed to 7.0 (10/29/2009)
It was originally set at 6.0, which corresponds to 30Apeak. The reason of change is to avoid the current trip due to the peaking at the beginning of the pulse.
(5) Water leakage from the cavity cooling water hose (several times)
Water hose was replaced by the PVC pipe (1/28/2010).
(6) Feedback coil with damper was burnt (1/27/2010).
Probably due to excessive voltage across secondary winding. Replaced by the former coil with N2=12 and no damper.

6. Conclusions

Efforts to remove the waveform distortions of the grid voltage were made from view point of higher-order-mode of the anode choke coils. However, they still remain considerably at higher frequencies than 5MHz. It is expected that the response to short pulse excitation (section 4) may give more information on the waveform distortions. Further investigation should be required with bias current.

On the other hand, use of grid input current should be considered for bias feedback loop because the waveforms are very sinusoidal and are more suitable for phase detector input rather than the present grid voltage.

Reference:

[1] LOI progress report LOI-6, December 14, 2009,
http://www-accps.kek.jp/Low-Impedance_Cavity/LOI-6.pdf
[2] Parameters for calculated gain are taken from
T. Oki et al, NIM A565 (2006) 358-369.
[3] T. Oki et al, ibid.

Table 1. Day-by-day summary of experiments in January, 2010

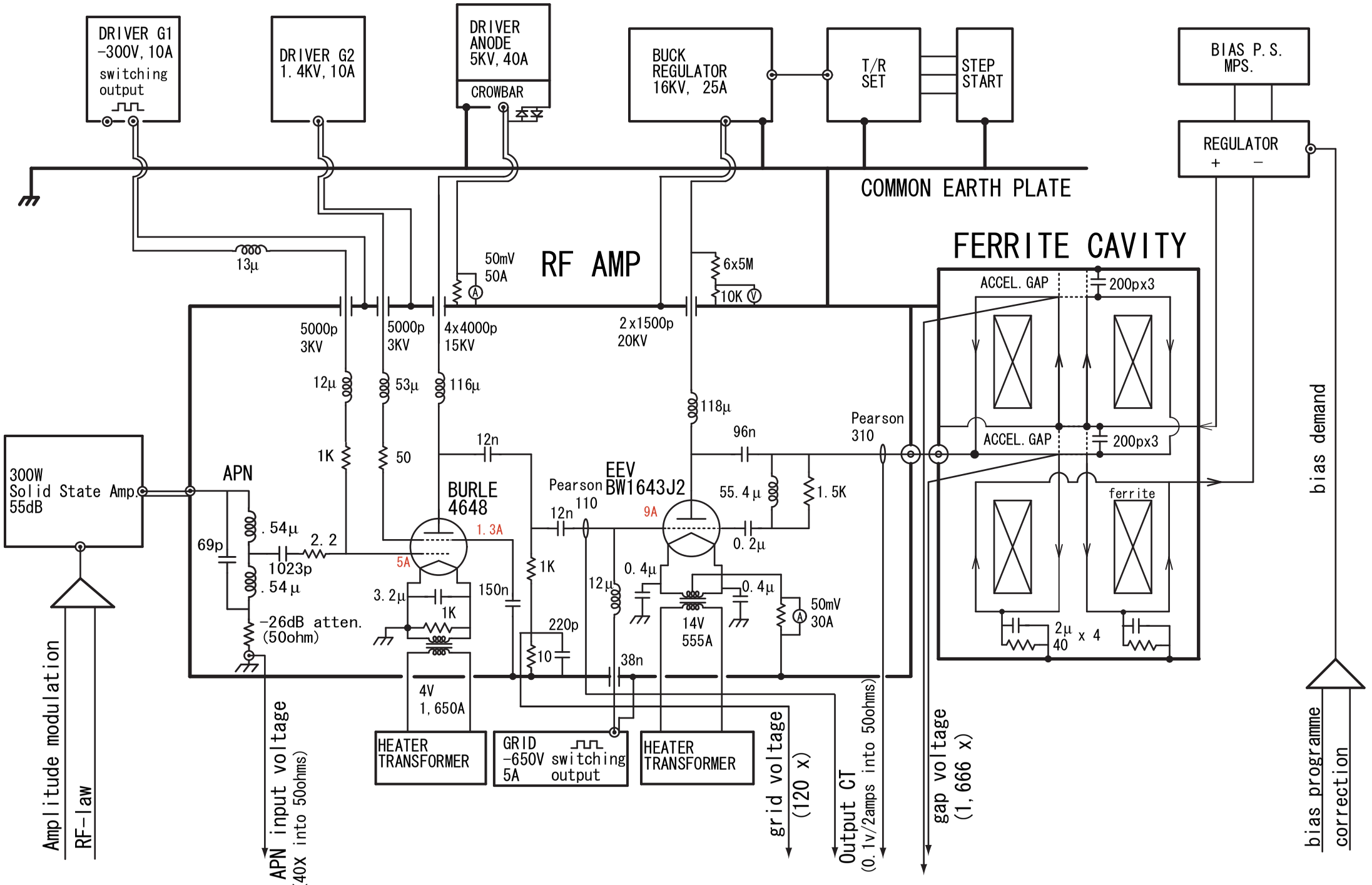
2010 January		ferrite bias	Damper 1			Temporary Re-arrangement in Driver Stage	Phase detection	Remarks
			Driver Anode Choke (New)	Final Anode Choke (Old)	Feedback Coil (FBC)			
20	W	dc	–	–	–			
21	T	ac	–	○	–		grid v., gap v.	Timing adjustment.
22	F	ac	–	○	–		grid v., gap v.	Optimization is made through trimming the demand offset.
23	S	ac	○	○	–		grid v., gap v.	Optimization cont'd.
26	T	ac	○	○	–	○ (1/2)	grid v., gap v.	Waveforms are worse. Restored to the original one (1/2). Optimization is made through $\Delta\phi$ offset.
27	W	ac	○	○	○		grid v., gap v.	Waveforms are similar, NOT improved with the FBC damper. Optimization is made through $\Delta\phi$ offset. Offset function is of a zigzag shape with time. Bias supply found tripped at shutdown process (due to zigzag shape?).
28	T	ac	○	○	–		grid curr., gap v.	FBC found to be burnt. Restored to the previous one with N2=12. Bias current goes to ~0 Arms when the grid current is fed to $\Delta\phi$ input instead of grid voltage (?)
		ac	○	○	–		grid v., gap v.	$\Delta\phi$ offset set to ~0 volt. Optimization is made through trimming the demand offset.
29	F	ac	○	○	–		grid v., gap v.	Optimization cont'd.
		dc	○	○	–			Short pulse excitation

APPENDIX

A-1 LOI schematic drawing as of February 3, 2010.

A-2 Supplementary Waveforms (WFs)
− number in ( ) stands for date in January, 2010 −

a2-1 WFs (22)
a2-2 WFs (23)
a2-3 WFs (26) -1/2
a2-4 WFs (26) -2/2
a2-5 WFs (27) -1/2
a2-6 WFs (27) -2/2
a2-7 WFs (28)



A-1. LOI Schematic Drawing

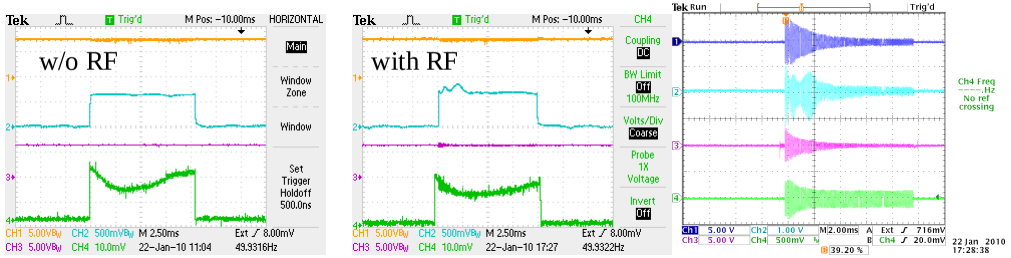
February 3, 2010 (YI)

a2-1: January 22, 2010

Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with feedback loop.

DRIVER New Choke	N2=4	Zgk	1st peak (2.418 MHz),	1st valley (10.382 MHz)	; 10/23/2009
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

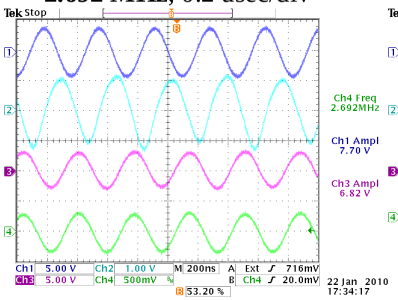
DC setup: Triode HV (2kV/V), output current (35A/V), Tetrode HV (1kV/V) and output current (10A/10mV).



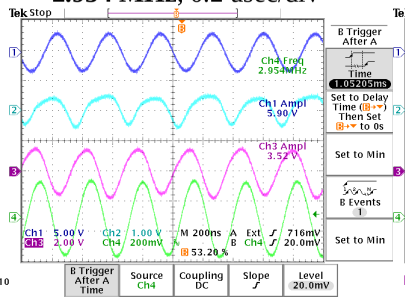
(foto
similar to Jan. 23)

Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

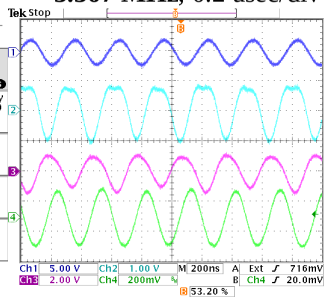
2.692 MHz, 0.2 usec/div



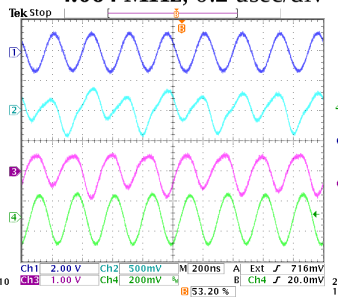
2.954 MHz, 0.2 usec/div



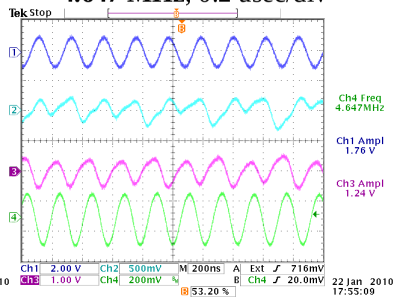
3.367 MHz, 0.2 usec/div



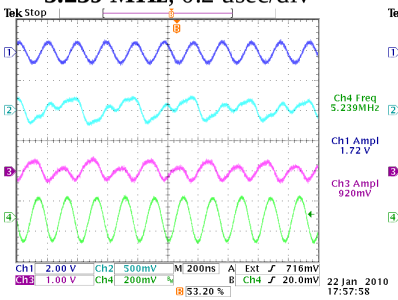
4.064 MHz, 0.2 usec/div



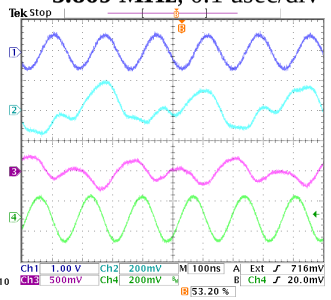
4.647 MHz, 0.2 usec/div



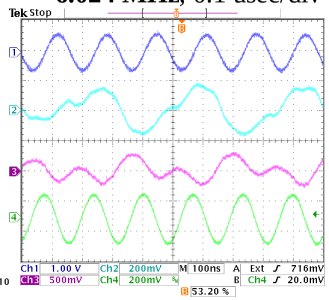
5.239 MHz, 0.2 usec/div



5.869 MHz, 0.1 usec/div



6.024 MHz, 0.1 usec/div



6.176 MHz, 0.1 usec/div

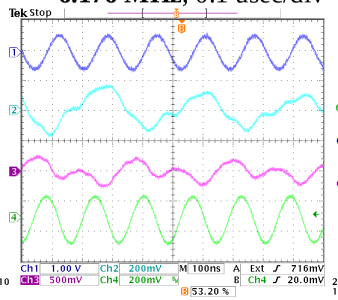


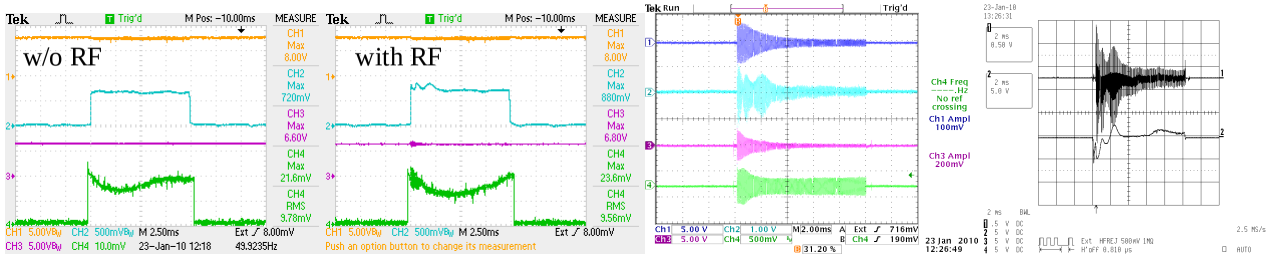
Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

a2-2: January 23, 2010

Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with feedback loop.

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV)..



Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

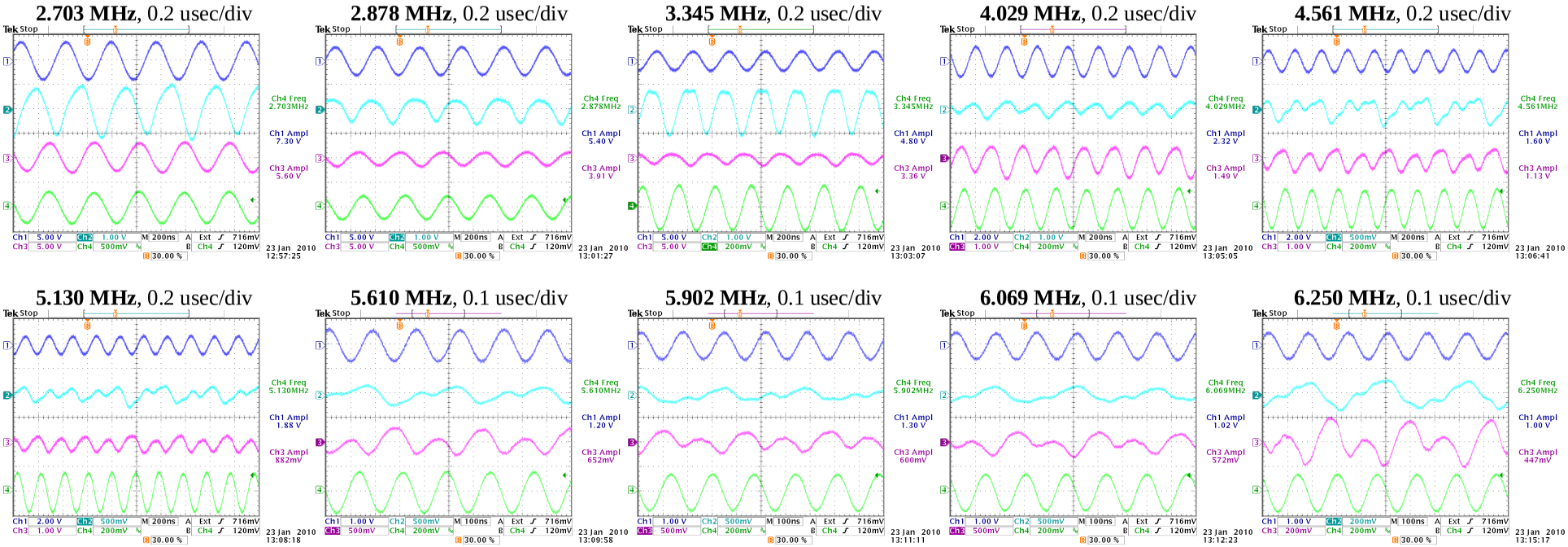


Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

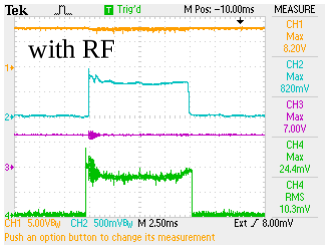
a2-3: January 26, 2010 - (1/2)

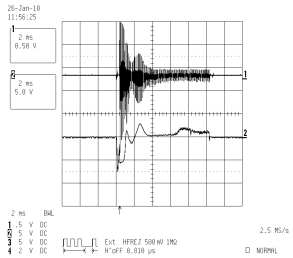
Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, Temporary modification at the driver stage

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).

w/o RF





Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

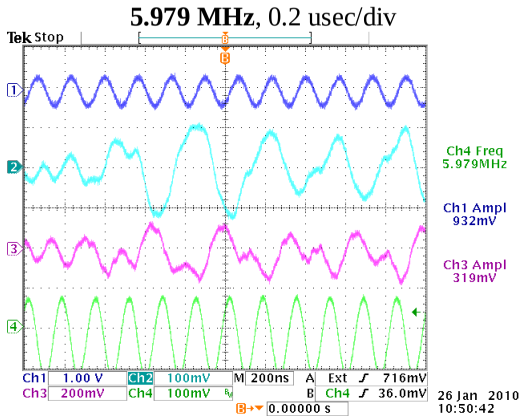


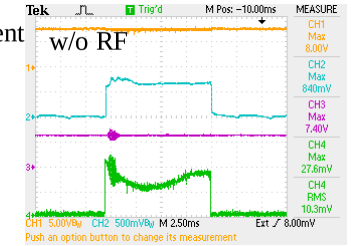
Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

a2-4: January 26, 2010 - (2/2)

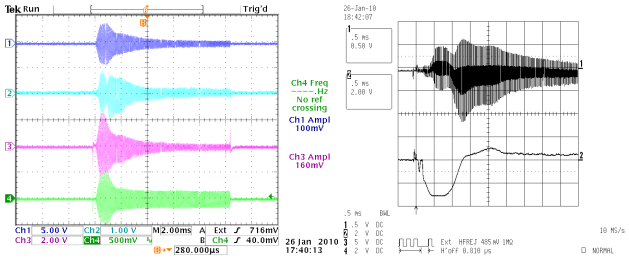
Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, Driver stage restored to original arrangement

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).



with RF



Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

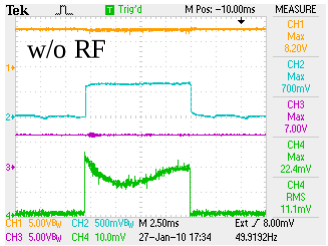
Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

a2-5: <u>January 27, 2010</u> - (1/2)

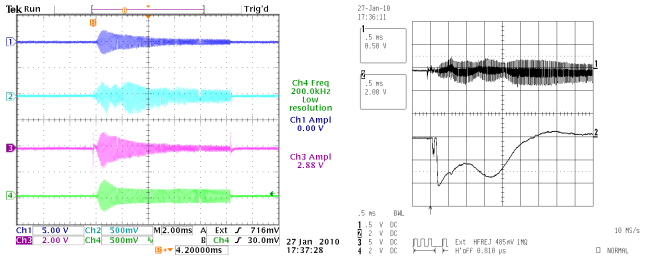
Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, phase detector offset=LOI_bias_3

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Damper 1	1st peak (6.242 MHz),	1st valley (~32 MHz)	; 1/26/2010, isolated measurement
	N2=11	Zpg	1st peak (2.040 MHz)	1st valley (17.002 MHz)	; 1/27/2010, new measuring lead

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).



with RF



Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

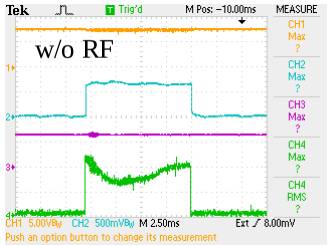
Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

a2-6: <u>January 27, 2010</u> - (2/2)

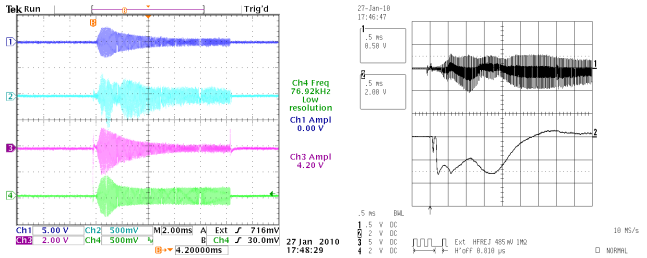
Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, phase detector offset=LOI_bias_4

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Damper 1	1st peak (6.242 MHz),	1st valley (~32 MHz)	; 1/26/2010, isolated measurement
	N2=11	Zpg	1st peak (2.040 MHz)	1st valley (17.002 MHz)	; 1/27/2010, new measuring lead

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).



with RF



Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

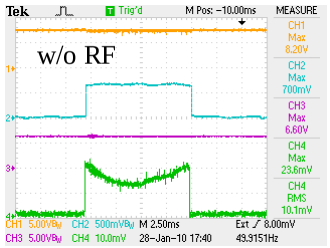
Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).

a2-7: January 28, 2010

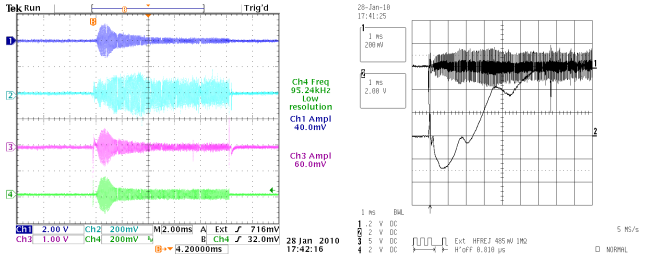
Experimental Conditions: 2nd Harmonic Cavity without Liquid Resistor, AC bias with Feedback Loop, trimming bias demand, phase detector offset=~0 volts.

DRIVER New Choke	N2=0	Damper 1	1st peak (3.200 MHz),	1st valley (~9.0 MHz)	; 1/23/2010, isolated measurements in-situ
		Zgk	1st peak (2.359MHz),	1st valley (~9.2MHz)	; 1/25/2010
FINAL Old Choke	N2=0	Damper 1	1st peak (~3.1 MHz),	1st valley (~9.8 MHz)	; 1/21/2010, isolated measurements in-situ
FEEDBACK COIL	N2=12	Zpg	1st peak (2.035 MHz)	1st valley (11.391 MHz)	; 10/23/2010

DC setup: Triode HV (2kV/V), Output Current (35A/V), Tetrode HV (1kV/V) and Output Current (10A/10mV).



with RF



Upper: Gap- Input Current (20A/V)
Lower: Δϕ Output (10deg/V, gap volt & grid volt) with "CAV TUNE"

Fig. RF envelopes (above) and waveforms with 2nd Harmonic Cavity at full cycle operation. From top to bottom line in each screen, cavity gap voltage (×1,590), gap-input current (20A/1V), grid-input voltage (×143) and grid-input current (20A/1V).