DRAFT LOI Progress Report

— Rejection of sub-harmonic content in the RF_law signal —

August 29, 2011

1. Introduction

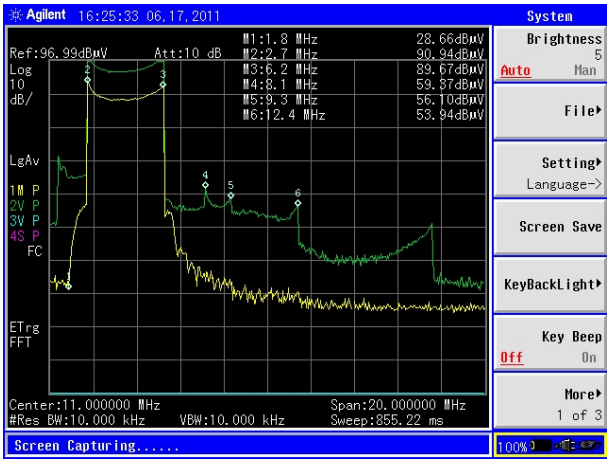
Waveform distortion of the grid voltage and cavity input current has been a longstanding issue. It was, however, pointed out in ref. 1 that the present LOI scheme easily produces waveform distortions if there exist only a small amount of sub-harmonic content in the master oscillator signal (RF_law) and/or higher harmonics generated at the following valve due to the non-linear response. The variable bandpass filter was then created on the National Instruments PXI platform to eliminate the second sub-harmonic ($f_{1/2}$) and those higher than $3\times f_{1/2}$ harmonic in the RF_law signal [2]. With the filter, waveforms approached rather sinusoidal ones, and the mysterious behaviour of the cavity input current at the cavity tuning was solved.

Because the filter was made only one channel and its delay time is 1.85us, it cannot be used for phase comparison. Instead, the triode grid input current, which is less distorted, was used for the phase detection with gap voltage. Frequent trips of the grid switcher, however, made it difficult to complete the gap voltage optimization under the limited machine time.

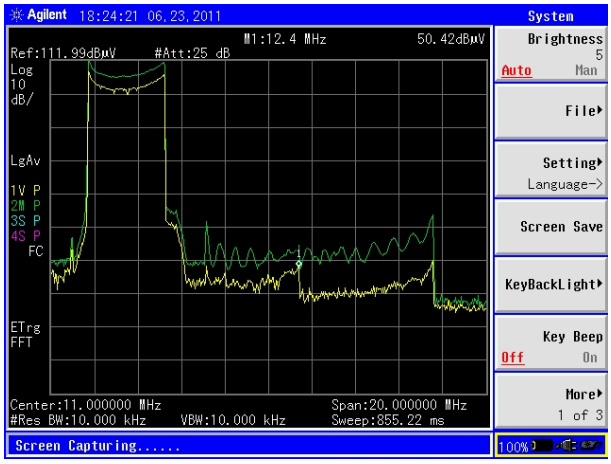
In the following sections are reported, experiments with variable bandpass filter in section 2, gap voltage optimization with grid input current in section 3, faults and remedies in section 4, and discussions & conclusions in section 5.

2. Experiments with variable bandpass filter

Frequency characteristic of the variable bandpass filter (hereafter, filter) is shown in fig. 1. The sub-harmonic content, which is -30dB without filter, is reduced to less than -40dB with filter at 1.3MHz for 1.2Vp-t-p output. Effect of filter on the RF waveforms was investigated by inserting filter at the locations shown in fig. 2. The results were shown in fig. 3, where the gap voltage was kept constant with 2.4kVp at the flat top, filter output 1.2Vp-t-p, and the gap and grid voltages were used for phase detection to the cavity tuning. The reduction of envelope height for both the grid voltage and gap input current is conspicuous, especially at the latter half of acceleration cycle. Waveform data was then sampled at 20us interval through the whole cycle. Frequency analysis is made of these waveforms using the Mathematica function ‘FindFit’. The fitted function has a form of



Green: Frequency Doubler (FD) Output,
Yellow: Filtered FD Output with 0.1Vp-t-p.



Green: Filtered FD Output with 1.2Vp-t-p,
Yellow: Filtered FD Output with 0.8Vp-t-p.

Fig. 1: Frequency spectra of frequency doubler (FD) output with and without filtering. Spectra depend upon the signal amplitude.

$$\mathrm{Wf}(t) = \mathrm{const.} + \sum_{n=1}^{nmax} a_n \,\mathrm{Sin}(2n\pi\, f_{1/2} t + \theta_n) \qquad (1)$$

where nmax = 12 and the frequency of second sub-harmonic component $f_{1/2}$ = 4.7MHz/2 in this analysis. The results are shown in fig. 4 with the experimental waveforms. Although this analysis does not reproduce irregular aspect of the waveform, general trend agrees well with experiments. Fig. 5 compares the frequency distributions with and without the filter. Without the filter, the $f_{1/2}$ content is comparable to, or larger than $2\times f_{1/2}$ content (fundamental component of the second harmonic RF (2RF) system) for both grid voltage and gap input current. However, it is reduced by more than ten by the filter, which explains the appreciable reduction of the envelope height in fig. 3. It is also seen that the $4\times f_{1/2}$ harmonic is not

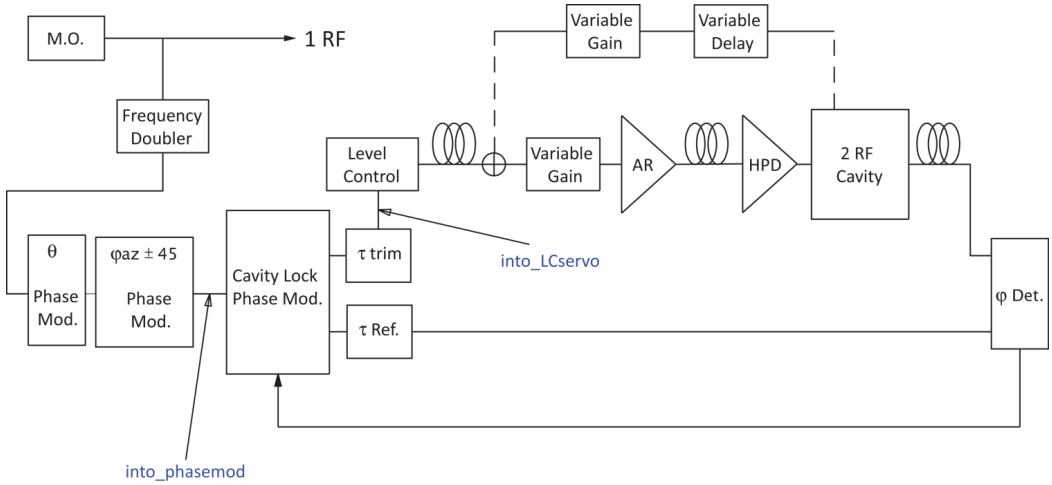
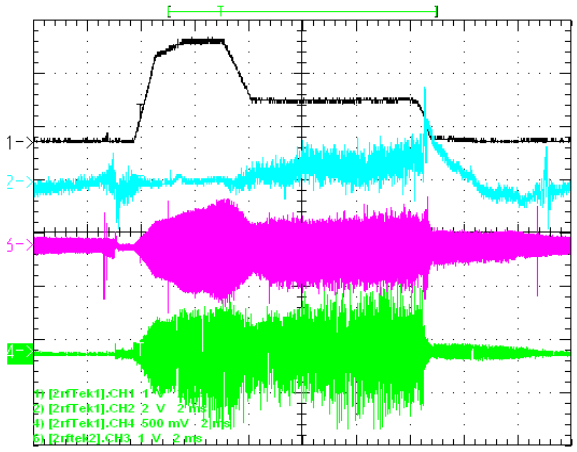
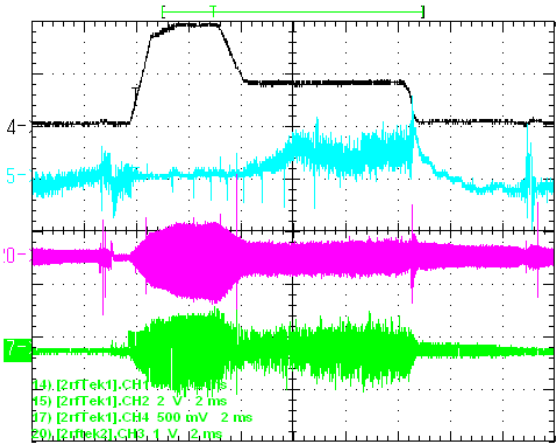


Fig. 2: 2RF low level control system. Variable bandpass filter is inserted for test at the input of cavity lock phase module (into_phasemod) and level control (into_LCservo).

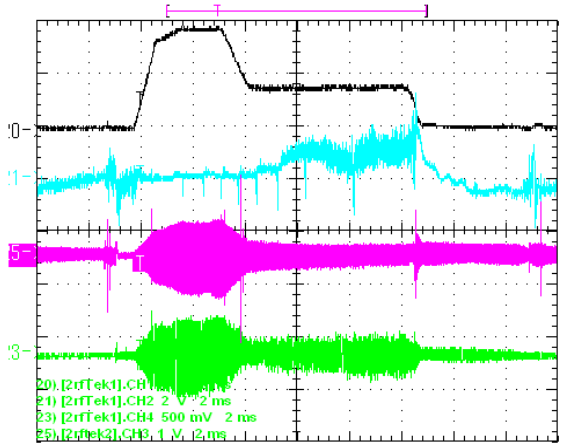


No filter.



Filter location at “into_phasemod” with 1.2Vp-t-p output.

Gridvolts and cavity input currents reduced. Spikes appeared at the PD.



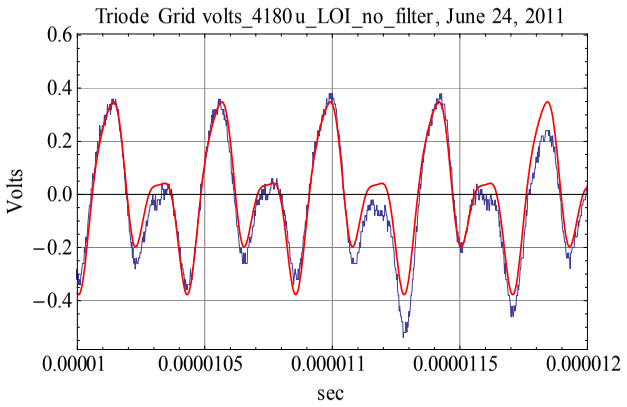
Filter location at “into_LCservo” with 1.2Vp-t-p output.

Gridvolts and cavity input currents reduced more. Spikes still appeared at the PD.

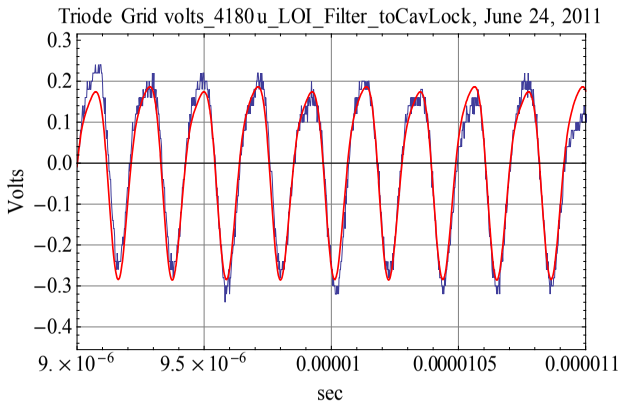
Fig. 3: Effect of bandpass filter upon RF waveforms. From top trace:
tek1 ch1: 2RF6 Gapvolts envelope monitor (1V=1.2kV/div)
tek1 ch2: 2RF6 PD monitor (2V=20degrees/div)
tek2 ch3: Triode grid volts monitor (1V=120V/div)
tek1 ch4: Cavity input current (0.5V=10A/div)

Triode Grid Volt

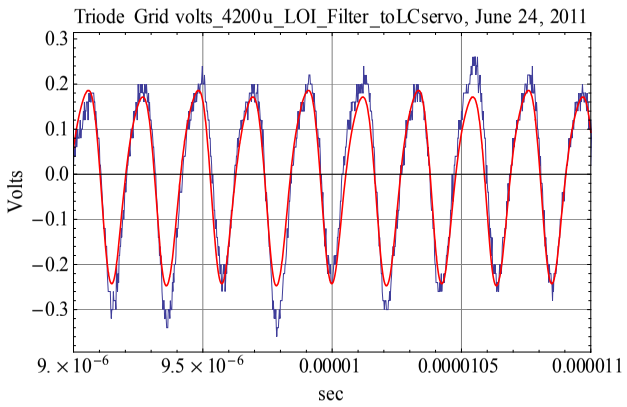
no filter



filter to phasemod

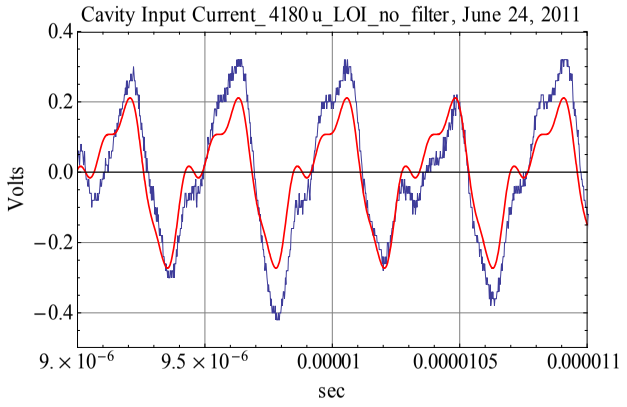


filter to LCservo

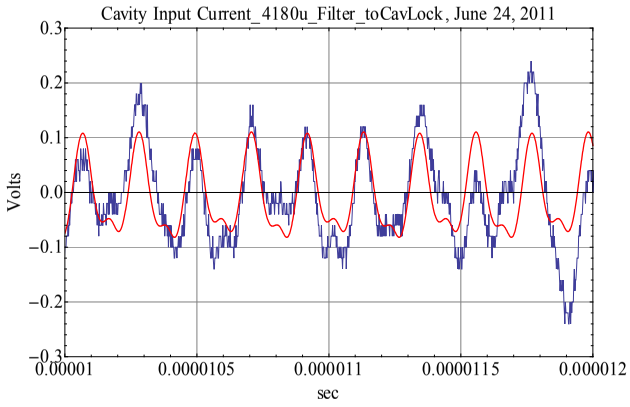


Cavity Input Current

no filter



filter to phasemod



filter to LCservo

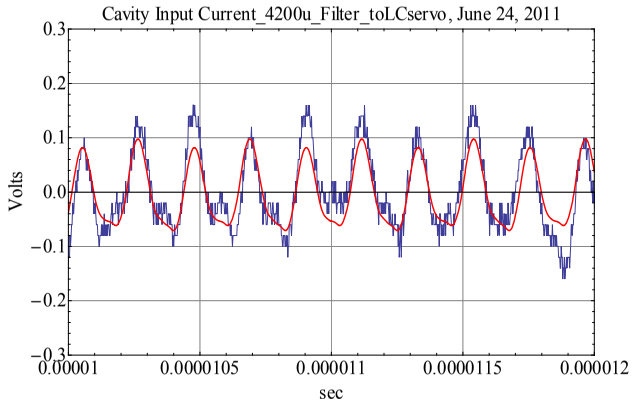


Fig. 4: Frequency analysis for triode grid voltage (upper) and cavity input current (lower) at 2RF frequency = 4.7MHz.

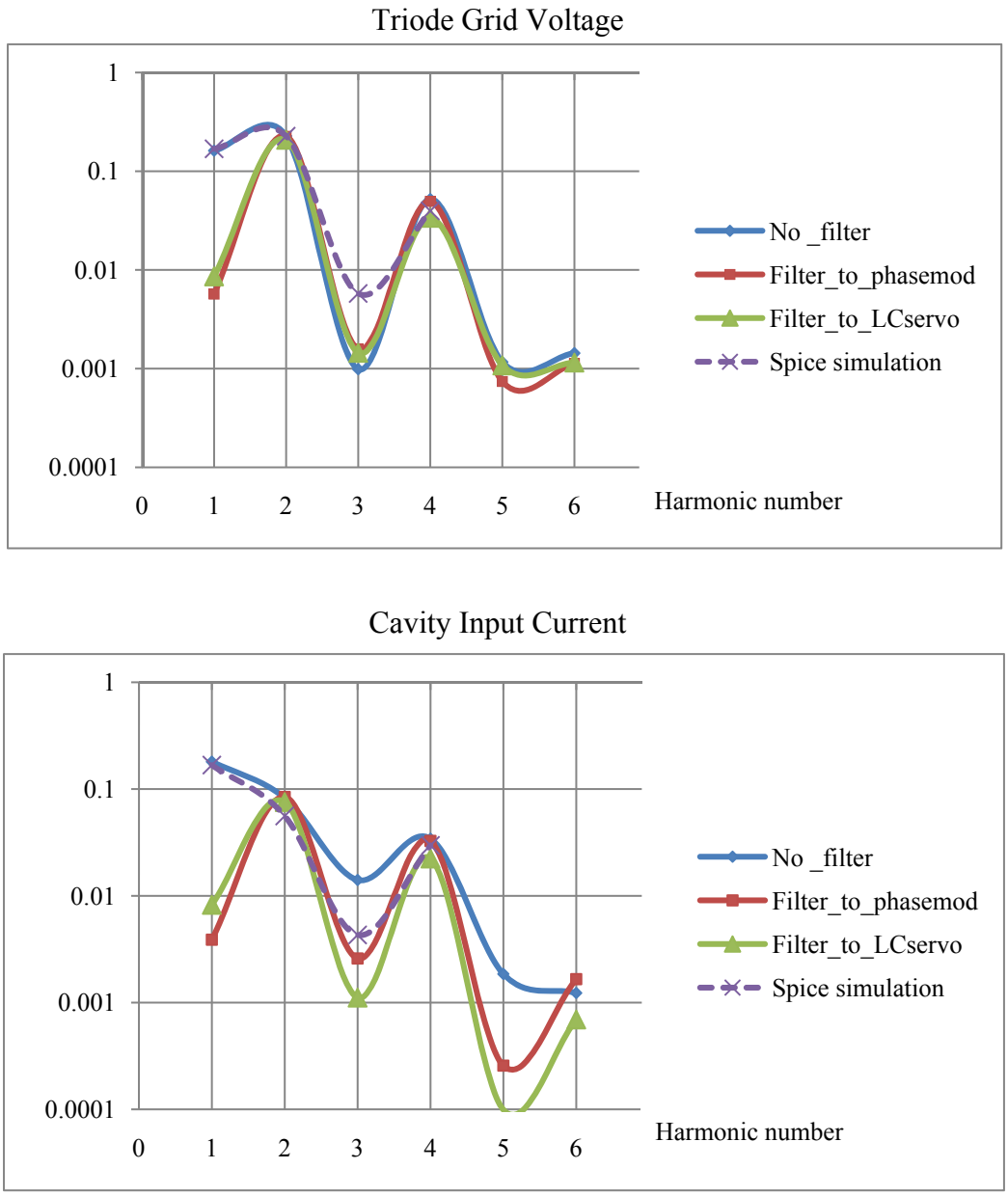


Fig. 5: Frequency spectrum of the triode grid voltage (upper) and cavity input current (lower) at 2RF frequency = 4.7MHz. Harmonic number in abscissa corresponds to the multiples of $f_{1/2}$ = 4.7MHz/2. Vertical coordinate shows the magnitude of a_n in eq. (1).

affected by the filter. This is probably because such component is generated by the non-linear response of the following circuits in the solid-state amplifier and/or the driver tetrode valve which is denoted by AR and HPD in fig. 2, respectively. As for $3\times f_{1/2}$ harmonic, filtering effect is not obvious in the grid voltage, while it is clear to see in the cavity input current. The TopSpice simulation was performed to compare with these experimental results for non-filtering case. The harmonic contents in the simulation are 2.2% and 0.6% for $f_{1/2}$ and $3\times f_{1/2}$, respectively, which are taken from fig. 1. The 5% content was assumed for $4\times f_{1/2}$ harmonic to fit the experimental data. The cavity comprises an LRC resonant circuit, and is

assumed to be tuned at resonance throughout the cycle. The cavity shunt impedance (R) is 538ohms [3]. The simulation result is also shown in fig. 5 with a dashed line, where the simulation output is normalized so that the 2RF component of grid voltage coincides with the experimental one. General trend is well explained by the simulation, although an agreement is not good for $3\times f_{1/2}$ component.

It should be noted how the cavity input current responds to the bias current tuning when it contains a lot of sub- or higher harmonics. Its amplitude then becomes quite insensitive to the bias current, because the cavity is already far from resonance for these harmonics.

3. Gap voltage optimization using grid input current

In order to achieve higher gap voltage, which method will be better to minimize (A) the triode current or (B) the cavity input current? In the former case, any triode loads, such as triode anode choke and the plate-grid feedback circuit, are incorporated into a resonant circuit with cavity. In the latter case only the cavity is tuned at resonance. The Spice simulation was carried out to see the difference of the two methods. In case of method (B), tetrode anode current limit (40Amps peak) will restrict the gap voltage below 10kV peak at 5ms and after. However, in case of method (B), triode anode current exceeds the limit (30Amps peak) even at the beginning of acceleration cycle to produce 10kV peak at the gap. The currents required to produce 1kV across the cavity gap in these methods are summarized in the appendix.

As was reported in [1], waveform of the grid input current is hardly affected by the harmonic contents, and shows rather smooth sine waveform. Investigation of phase relation between the grid input current and the gap voltage in the method (A) was then envisaged to produce as high gap voltage as possible during a couple of physics machine times: in June 30 and July 1 from 0:00am to 8:00am each. However, the grid switcher was tripped 4 times during the periods. The power switching transistor (IRG4PH20K) was then ‘bent’ and replaced, although the protection diodes were intact. Such frequent trips made it difficult to complete the experiment (fig. 6).

For the next experiment, it is necessary to check the length of cables which will be used for phase detection. Also, optimization process under the beam loading needs to be considered.

4. Faults and remedies

(1) Fig.7 shows the output voltage of the grid switcher measured at the output terminal of the grid switcher chassis. With the output cable connected, the rise and fall times in an exponential shape are mainly due to the time constant of the load capacitance and the resistance of the series and shunt legs of the switcher. These time constants are 5.1us and 8.4us for rise- and fall-time, respectively. However, without the output cable, these may indicate the switching speed of the power transistor. D Bayley suggested that an insufficient switching speed of the power transistor will overheat and damage the transistor. The fact 'protection diodes were intact' upon faults supports his suggestion. N Farthing is now designing a fast driving scheme of the power transistor.

(2) Flow interlock of the grid switcher
It was found at the end of this experiment that the flow interlock is not linked to the real water flow, but only to the AC switch on status of the chiller unit. Actually, we have operated the grid switcher without flow. Although the power switching transistor is forced-air cooled and is not using the cooling water, no water-flow operation may have caused ambient temperature rise within chassis. Flow meter with an interlock output should be provided for the chiller unit.

5. Discussions & conclusions

Experiments on the harmonic contents were performed with a newly designed "variable bandpass filter". Upon rejection of the unwanted harmonics in the RF_law signal, the triode grid voltage and cavity input current have nearly recovered their original sine waveforms. These waveforms will be used in the forthcoming tuning for the higher cavity voltage.

Restriction of the LOI experiments due to water shortage in the SP6 will be detrimental to an efficient work on the LOI. Improvement of the water cooling system to allow for the LOI operation at any time is highly required.

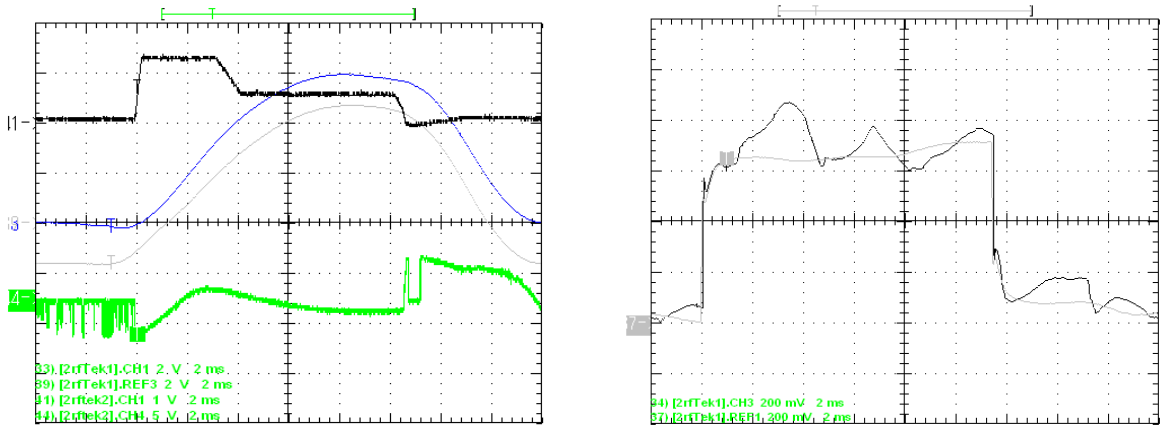
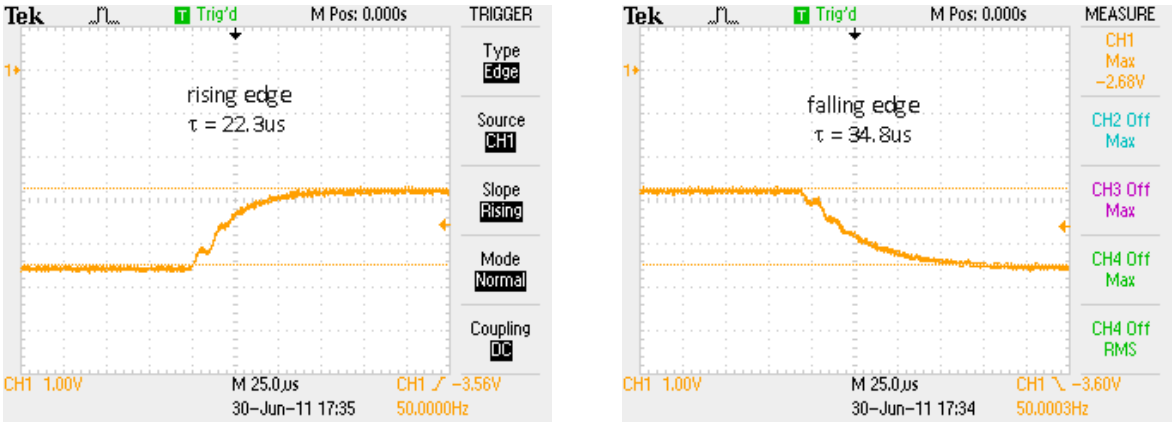


Fig. 6: Minimization of triode anode current with phase detection between grid input current and cavity gap voltage. Left: from top, gapvolts envelope (1V=1.2kV/div), bias demand and Cavtune PD monitor (5V=50°/div). Right: triode anode current (0.2V=5A/div) with (black) and without (grey) RF on. All traces are on 32 average.

(a) With load



(b) Without load

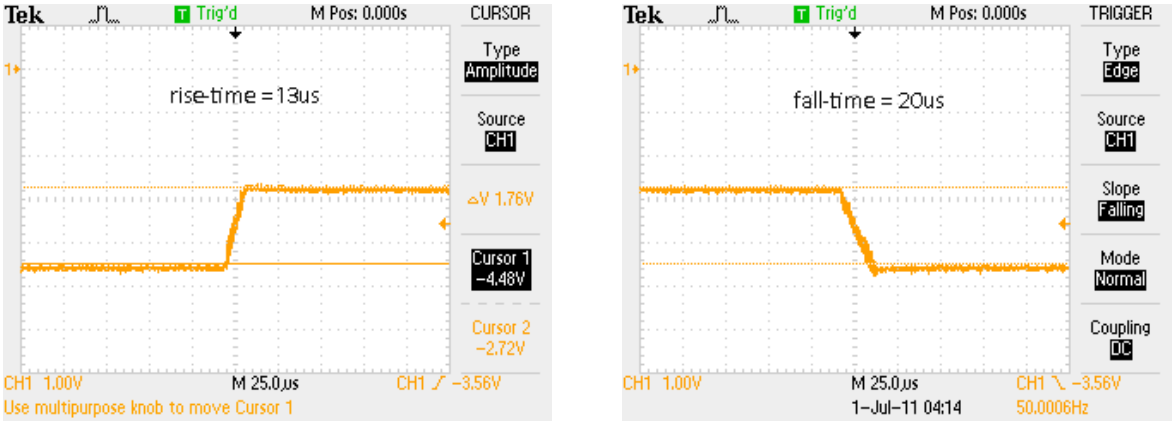


Fig. 7: Output voltage of the grid switcher (a) with and (b) without load.

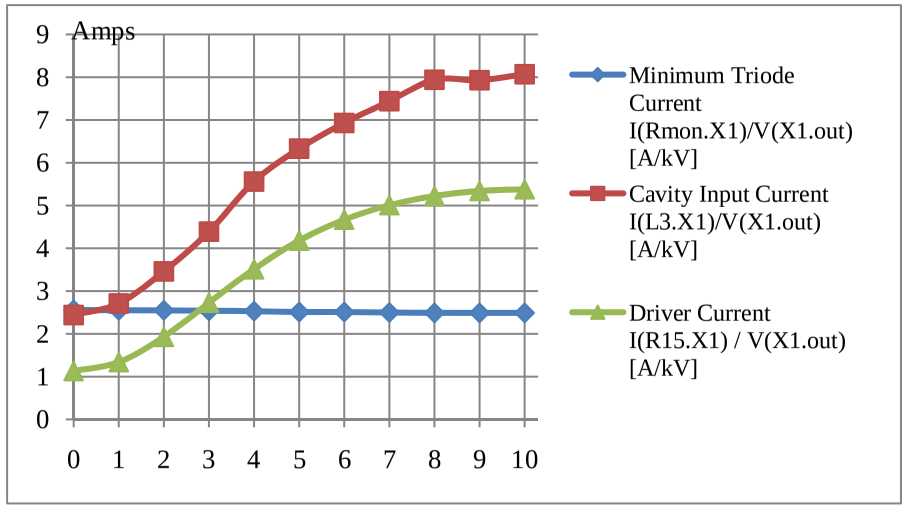
References:

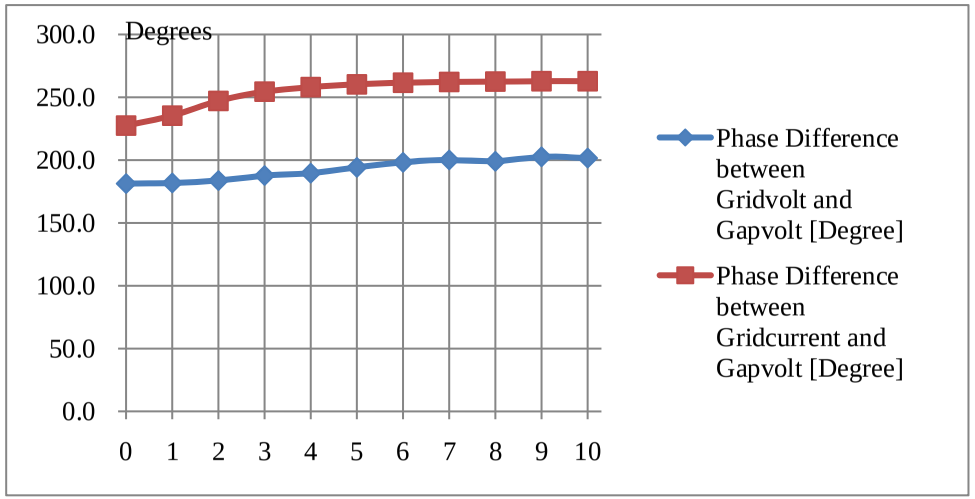
[1] LOI progress report LOI-8, September 13, 2010.
[2] D Allen and A Seville, to be published elsewhere.
[3] LOI progress report LOI-2, September 24, 2005.

Appendix:

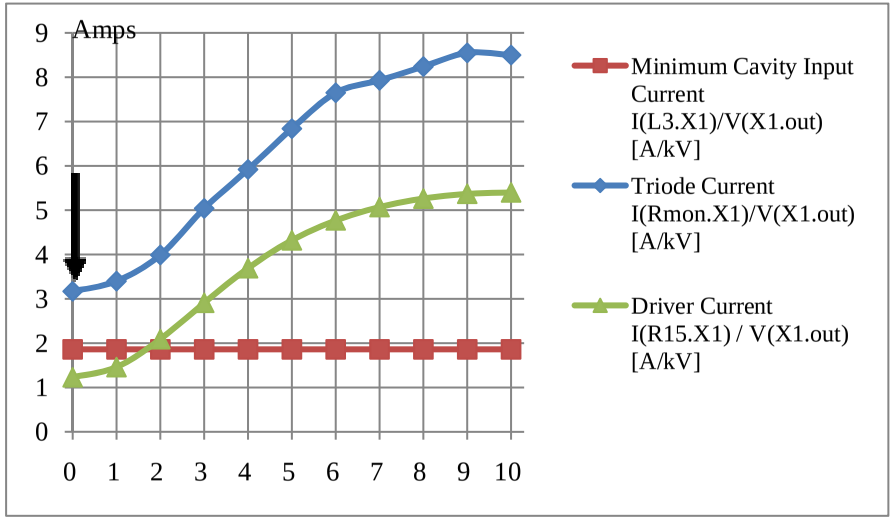
Comparison of two minimization methods: one is to minimize the cavity input current, and the other to minimize the triode current to produce 1kV at the cavity gap. Beam loading is not included.

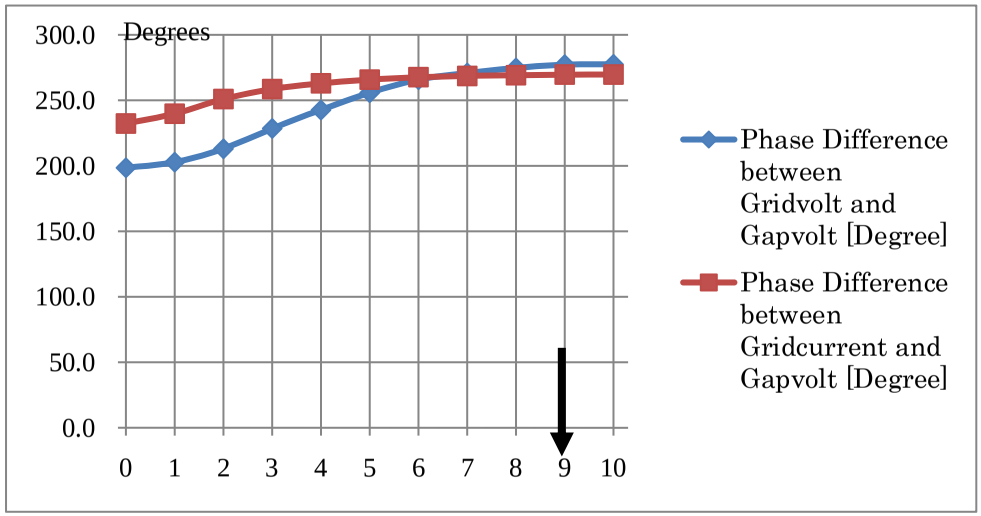
Minimized Triode Current to produce 1kV across Cavity Gap





Minimized Cavity Input Current to produce 1kV across Cavity Gap





*) Arrow shows the time when the current exceeds its maximum rating when the cavity gap voltage is reaching 10kV.