Summary LOI Developments

--1996 through 2003--

1. Introduction

why the Low Output Impedance?

2. History of the scheme

(1) cathode follower design (~1998)

(2) floating grid-cathode drive (1998~1999)

(3) grounded cathode scheme with p-g feedback (2000~)

3. Results

(1) RF data

(2) voltage gain & output impedance

(3) discussions

4. Power/water requirements for installation at ISIS

appendix) LOI schematic drawing

ANL/ISIS/KEK collaboration

(presented by Y Irie)

http://www-accps.kek.jp/Low-Impedance_Cavity

1. Introduction

In order to capture and accelerate higher beams without beam losses, compensation techniques for heavy beam loading are essential. The beam loading for the accelerating mode cavity has been overcome successfully by the beam-feed forward system combined with the beam-phase loop to damp the dipole oscillations. A 2^{nd} harmonic system is used to control the beam density distributions. Although a 2^{nd} harmonic system is operated in the non-accelerating mode, i.e. beam-cavity phase is nearly zero, a large 2^{nd} harmonic component of the beam would distort the cavity voltage, resulting in unstable control of the density. The low-output-impedance amplifier can provide a method to control the beam distribution more effectively because the beam loading to the system is negligibly small.

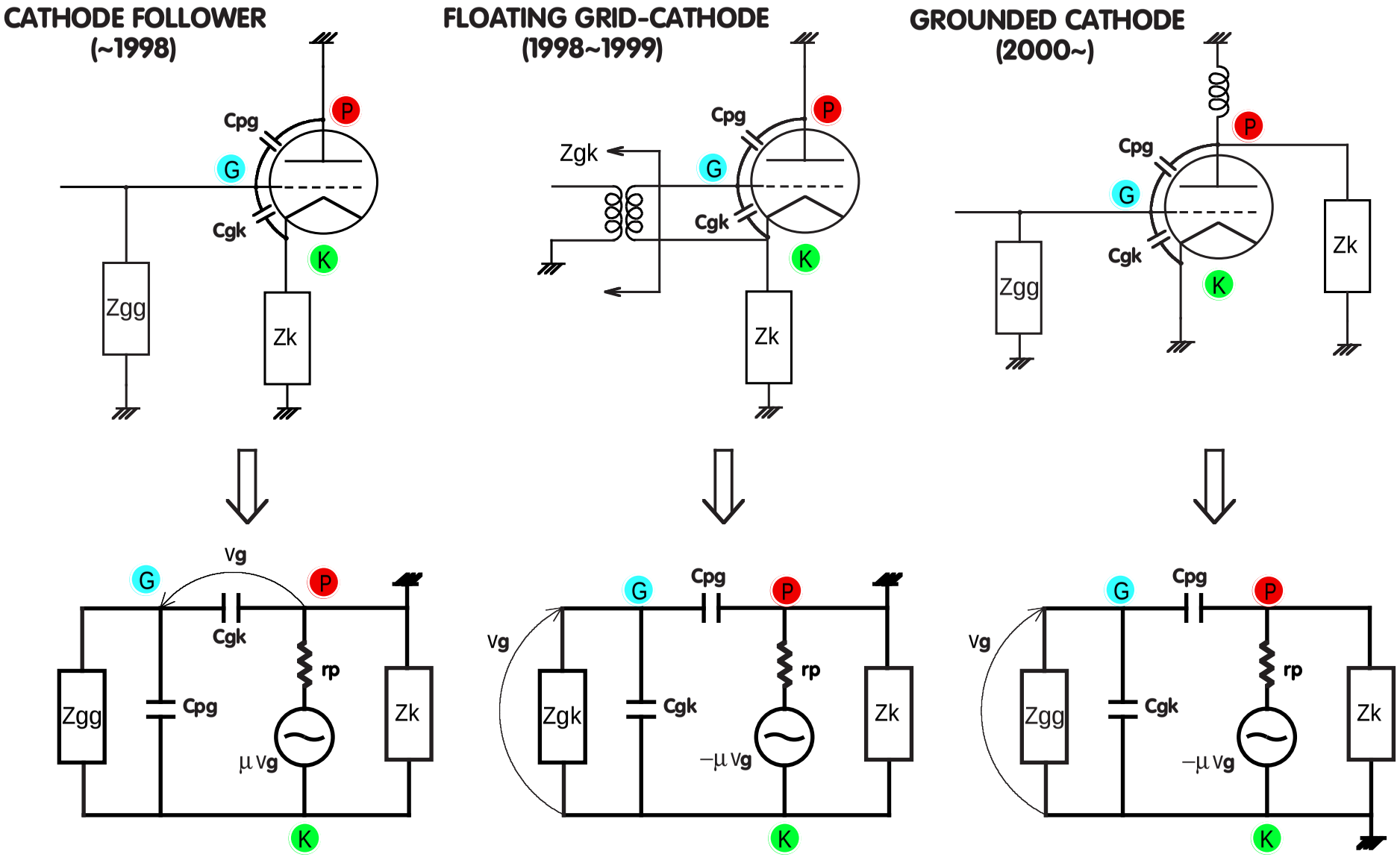


Fig.1 History of the LOI scheme

3. Results

The test has been performed until early February 2003, nearly at the plate-dissipation limit of the final triode, and at the breaker limit of the switch board to the driver tetrode. The experiment was almost stable, and more than 12KVpeak-to-peak was obtained in the middle point of the acceleration period. However, the waveforms are distorted at the higher frequencies. We did not have enough time to investigate the reason of distortion (cavity? amplifier? or both?). We probably need some time at ISIS for such investigations.

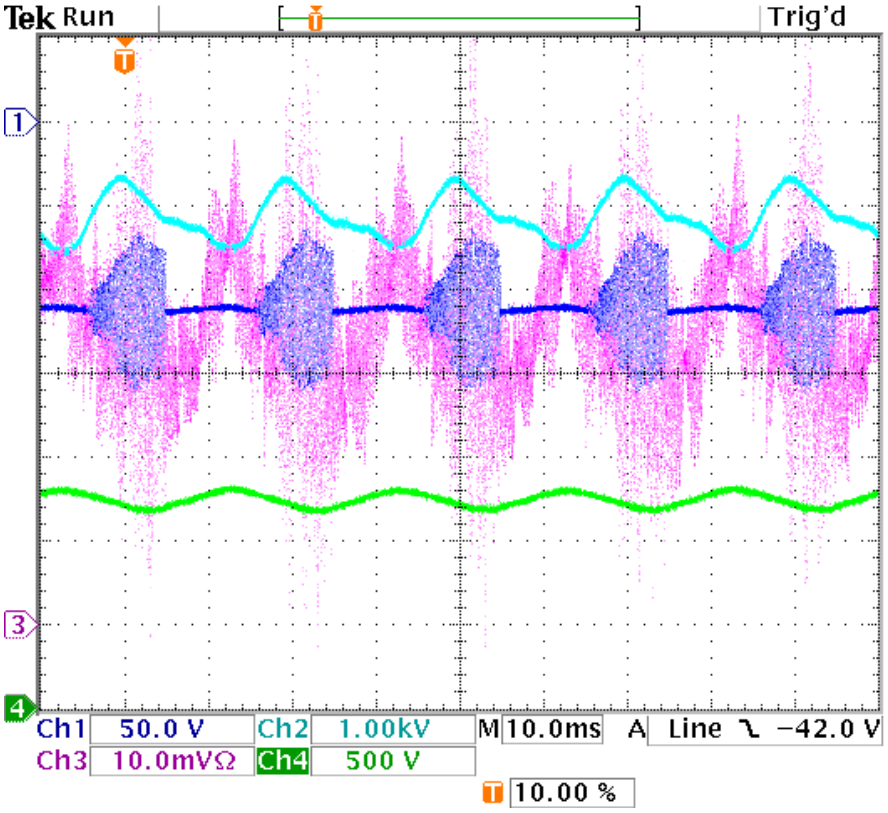
No provisions with AVC and bias tuning loops. The cavity input current was, however, minimized by adding offsets to the original (sinusoidal) waveform of the cavity bias current. The repetition rate was 50Hz with a frequency range from 2.6 to 6.3MHz.

References:

http://www-accps.kek.jp/Low-Impedance_Cavity/collaboration_report.pdf
http://www-accps.kek.jp/Low-Impedance_Cavity/LOIC_progress_2000-2002.pdf
http://www-accps.kek.jp/Low-Impedance_Cavity/FEB03.pdf

3.1 RF data

4648 tetrode driver stage



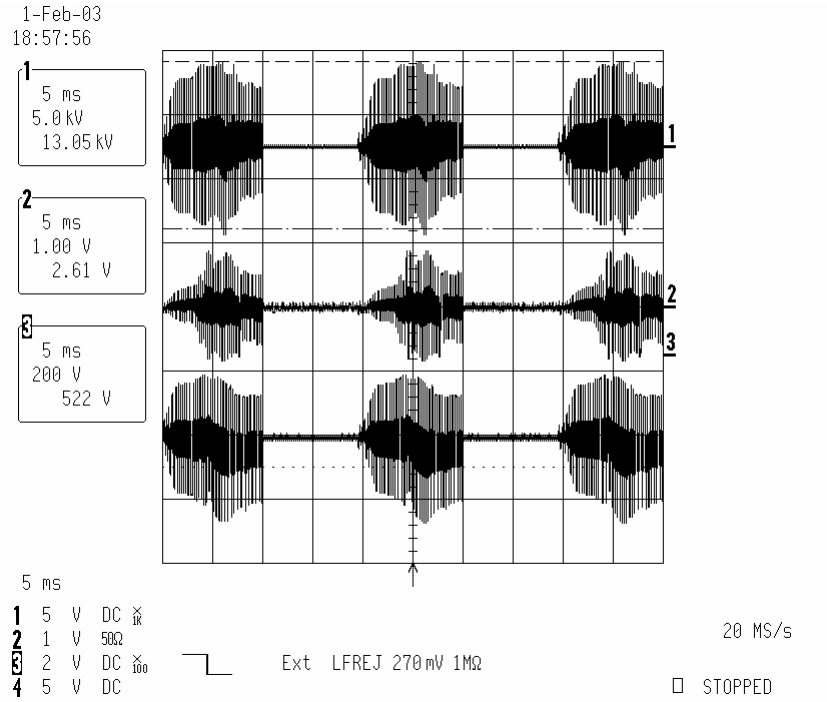


Fig. 1 RF envelopes. upper trace: cavity voltage (5KV/div), middle trace: cavity input current (20Amps/div), and grid input voltage (200V/div).

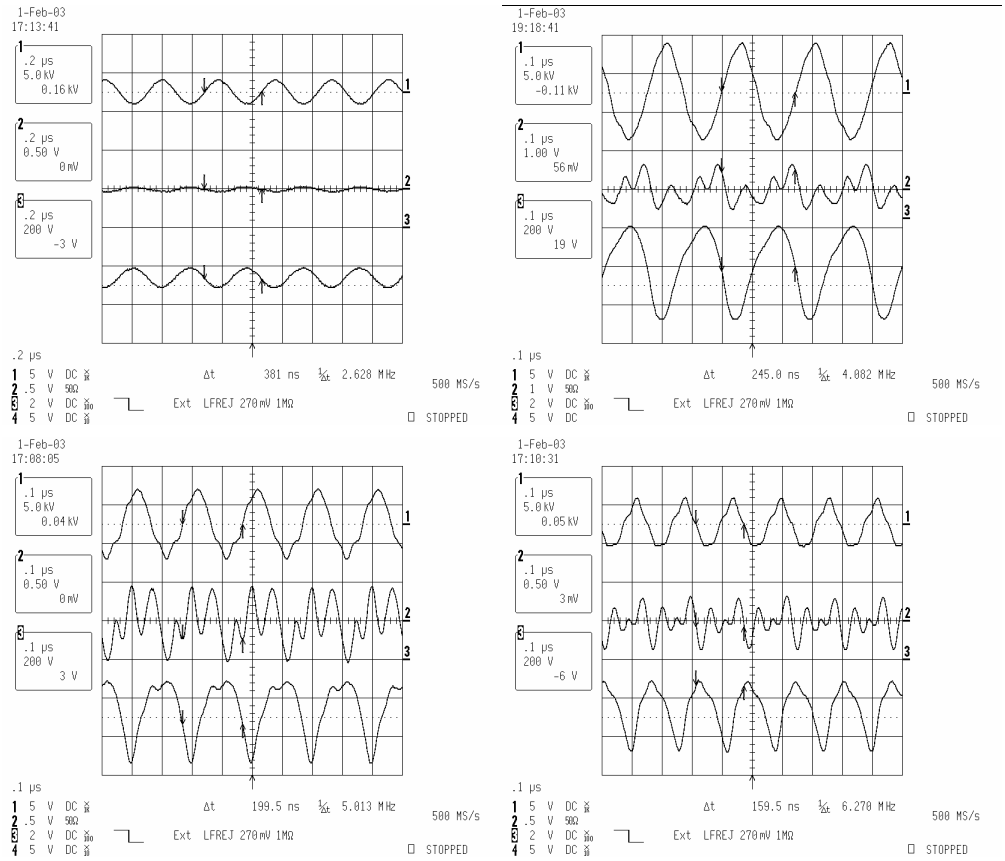
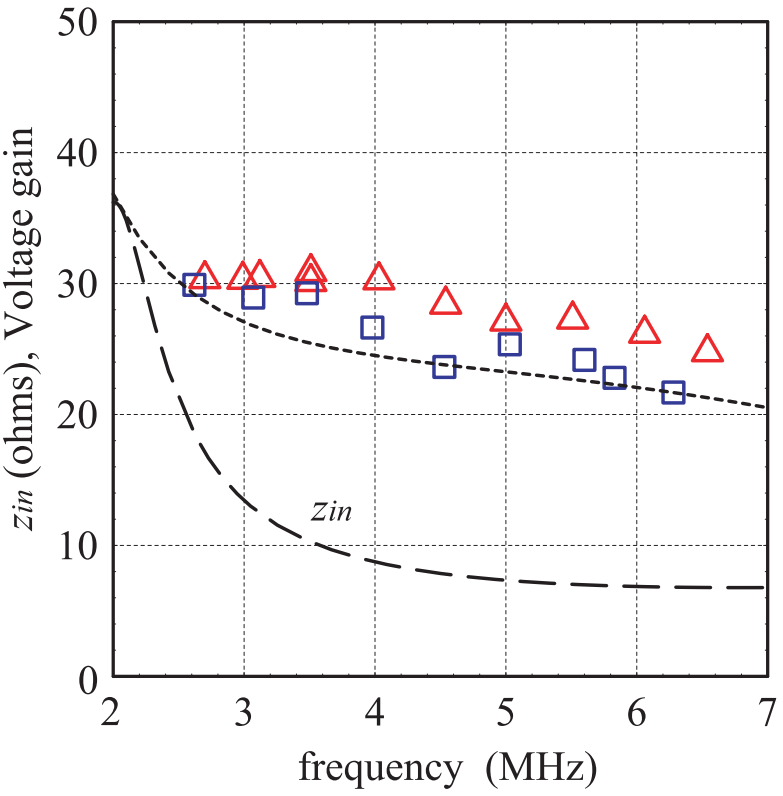


Fig. 2 Detailed waveforms at 2.6, 4.1, 5.0 and 6.3MHz.

3.2 voltage gain & output impedance



measured voltage gain with frequency swept (box) and unswept (triangle) mode. Zin is the input impedance looking into the grid of the final triode

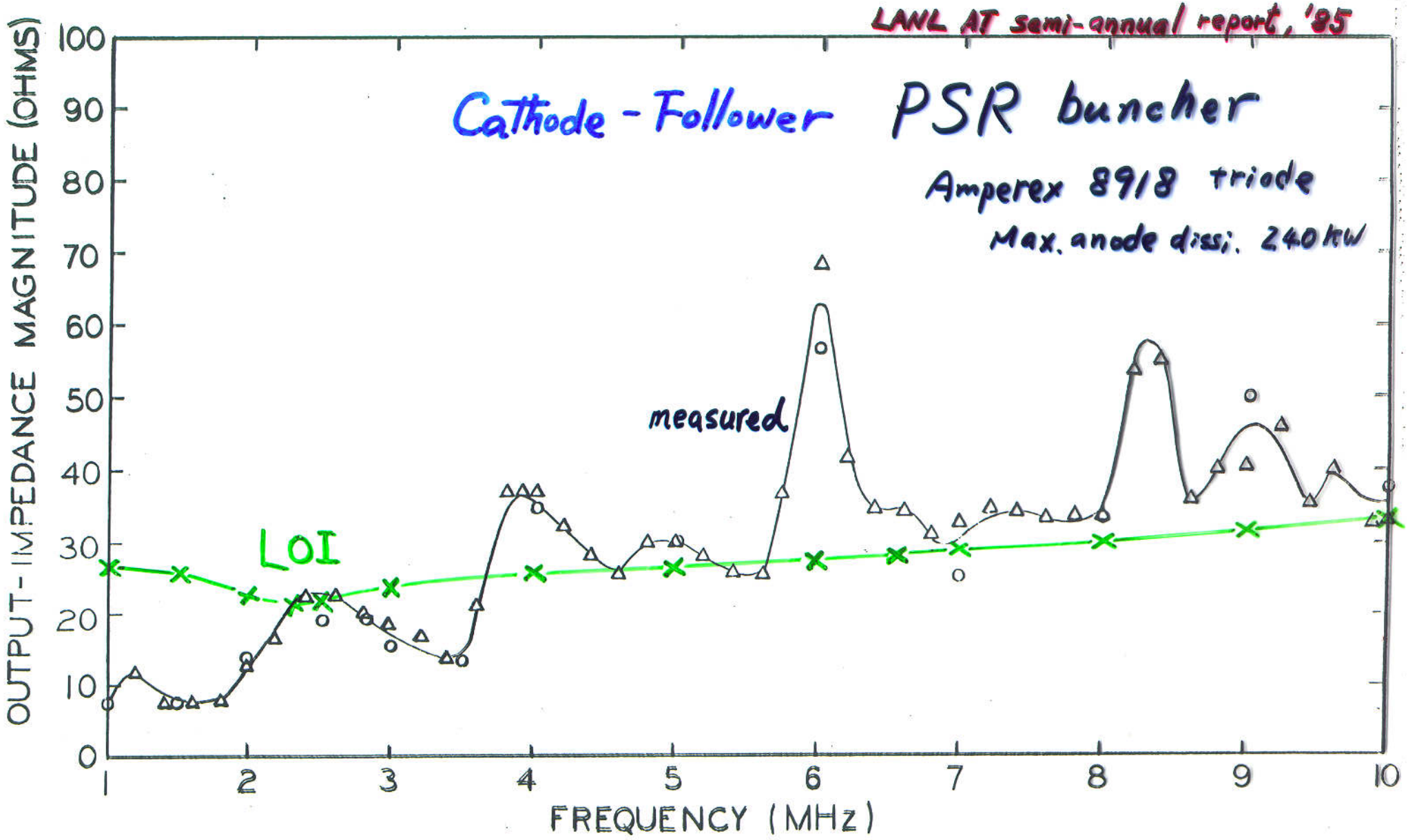


Figure 2. Plot of the 2.8 MHz buncher system impedance vs. frequency, obtained by wire excitation of the cavity.

3.3 discussions

1. Driver stage tetrode seems luxurious. Introduction of a transformer into the driver stage may help save the operation cost. However, we did not think of it further because we were anxious about the unnecessary inductance and capacitances by the transformer. The operating point of the tetrode at ISIS is Ep=5kV with Ip=40Amps.

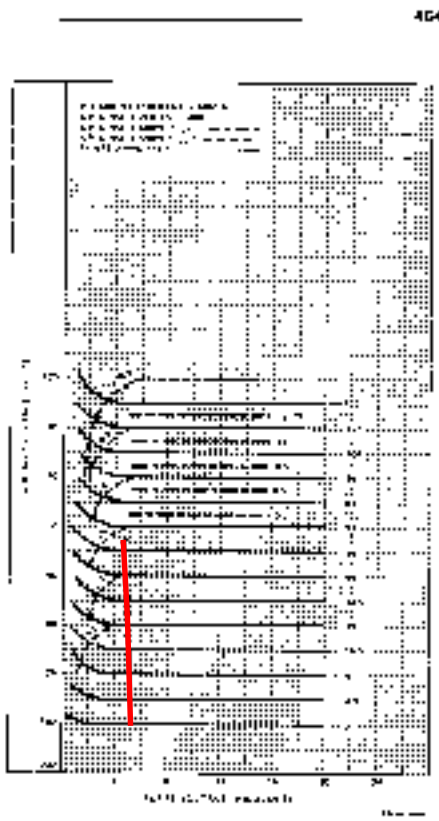


Figure 3 – Typical Characteristic Eb-g = 1400 V

2. Grid switching system

Final triode is operated with Ep=16kV and Ip=25amps. Since the plate dissipation of the triode is 240kW, it should be operated with duty factor 60%. The grid switching system is indispensable. Such system is also very useful for the driver tetrode.

3. Dummy load?

How long can LOI be tested with load (2nd harmonic cavity) before Xmas 2004? Probably more than a month will be necessary for tuning. Otherwise, dummy load is needed at MICE hall.

load-line of BURLE 4648 tube

Fig. 2.3 quiescent current 30 amps at 5 KV.

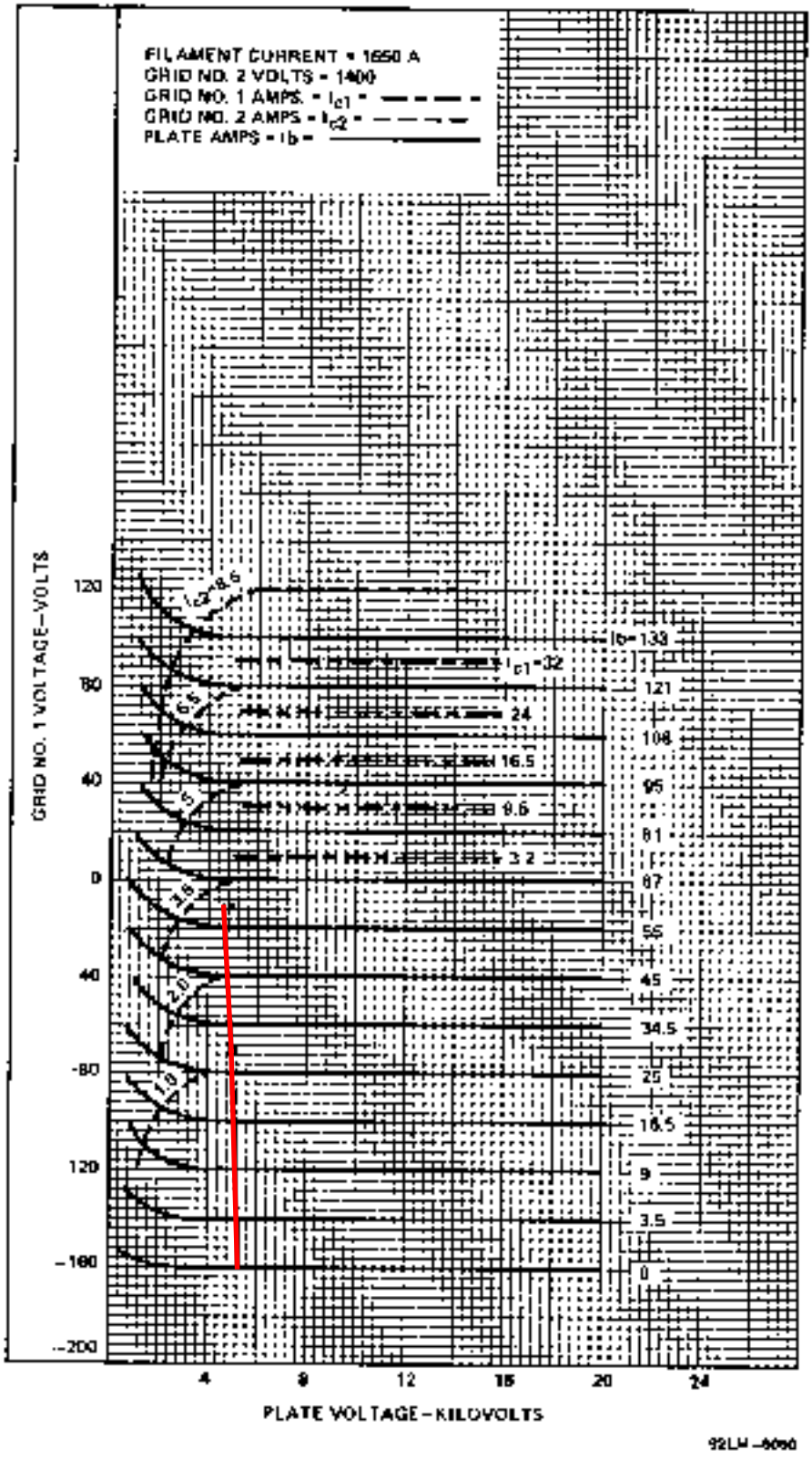


Figure 5 - Typical Characteristic (E_{c2} = 1400 V)

LOI power and water requirements

EQUIPMENT	POWER		COOLING WATER		REMARKS
	VOLTS	KVA	l / min	dissipation, KW	
FINAL ANODE(EEV BW1643J2)	3ϕ, 400V	peak 400 ave. 240	180◆	240.0	pmax<7 kg/cm^2, Δp=1.84kg/cm^2, inlet<50°C, Δt=20°C 16KV, 25A with 60% duty
step-start	1ϕ, 200V	4.0			
buck regulator			19-38		5-10gpm@60psi (4.2kg/cm2)
DRIVER ANODE(Burle 4648)	3ϕ, 400V	200.0	200◆	200.0	pmax<7 kg/cm^2, Δp=1.4kg/cm^2, outlet<70°C, Δt= , resistivity>1 Mohm-cm
	1ϕ, 200V	0.4			
BIAS POWER SUPPLY	3ϕ, 400V	100.0			
stainless circuit			40.0		7.5 bar, 21°C
copper circuit			80.0		2.7 bar, 24°C
FINAL FILAMENT	1ϕ, 200V	10.0			
FINAL GRID SUPPLY	1ϕ, 200V	1.5			
DRIVER FILAMENT	1ϕ, 200V	10.0			
DRIVER G1 SUPPLY	1ϕ, 200V	1.0			
DRIVER G2 SUPPLY	3ϕ, 200V	3.0			
CAVITY			130.0		pmax<7 kg/cm^2, Δp=4.5kg/cm^2, inlet=20°C, Δt=3°C
SOLID-STATE-AMPLIFIER	1ϕ, 200V	2.0			
ANCILLARY					
FAN etc	3ϕ, 200V	0.7			
4648 Fil, Fil Gnd, G1, G2			38◆		
SHUNT LOAD (Rsh)			40◆	15.0	
LOI COTROL CONSOLE	1ϕ, 100V	0.3			
	1ϕ, 200V	0.2			
TOTAL		peak 733.1 ave. 573.1	727 ~746	455.0	◆LOI requires 458 ℓ/min, but 270 ℓ/min is available at SP8.

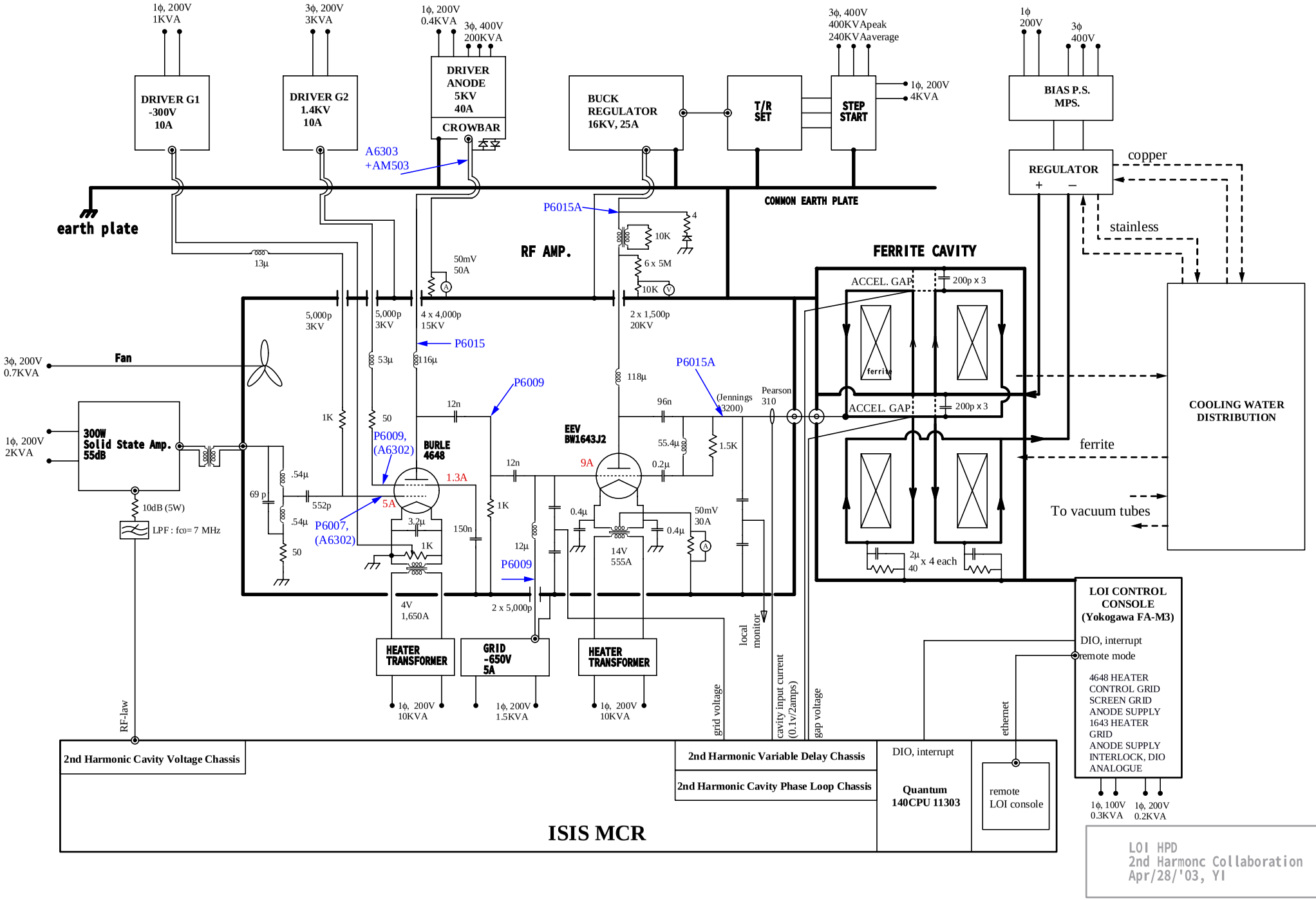
LOI ac power details
(except for bias power supply)

type KVA	EQUIPMENT	POWER VOLTS	 KVA	SPECIFICATIONS	adaptability to RAL ac-rating	Remarks
3ϕ, 400V	FINAL ANODE(EEV BW1643J2)	3ϕ, 400V	peak 400 ave. 240		(ok)	original ac input volatge is 480volts. (Feb/22/99)
	DRIVER ANODE(Burle 4648)	3ϕ, 400V	200.000	Tecno input tap: 400,420,440	ok	
peak 600 ave. 440						
3ϕ, 200V	DRIVER G2 SUPPLY	3ϕ, 200V	3.000	Yamabishi HT-393 1/2~2/2 input: 50/60Hz, 210Vac output: tapped 1.8, 2.2, 3.4KV	−	usable at 240Vac input if output not exceeds 3KVA (6/2/03, Mr Hagiwara, Yamabishi) see 3ϕ variac
	ANCILLARY	3ϕ, 200V	0.700		trafo	fan, blower, etc
4.0			3.700			
1ϕ, 200V	STEP START	1ϕ, 200V	4.000	Toyozumi SD21-21KB primary: 240, 220, 200, 0 secondary: 0, 100, 110, 115	ok	
	DRIVER ANODE CONTROL	1ϕ, 200V	0.400		trafo	
	FINAL FILAMENT	1ϕ, 200V	10.000	Matsunaga slide regulator MP-2050-C input: 200Vac +5% output: 0-200Vac (50Amax)	trafo	saturated at 240Vac input, including motor-drive power
	FINAL GRID SUPPLY	1ϕ, 200V	1.500	Takasago GP0650-5R	trafo	
	DRIVER FILAMENT	1ϕ, 200V	10.000	Matsunaga slide regulator MP-2050-C input: 200Vac +5% output: 0-200Vac (50Amax)	trafo	saturated at 240Vac input, including motor-drive power
	DRIVER G1 SUPPLY	1ϕ, 200V	1.000	Takasago GP0350-10R	trafo	
	SOLID-STATE-AMPLIFIER	1ϕ, 200V	2.000	ENI A-300 230Vac +6%~-12%	ok	
	LOI COTROL CONSOLE	1ϕ, 200V	0.200		trafo	
32.0			29.100			
1ϕ, 100V	LOI COTROL CONSOLE	1ϕ, 100V	0.300		trafo	
	OSCILLOSCOPES					
	TDS3014B (2 pieces)		0.075	47~440Hz 100Vac~240Vac (±10%)	ok	replace ac-cord 125V/7A

LOI ac power details
(except for bias power supply)

	LeCroy9354AL		0.350	45-66Hz 90-132Vac or 180-250Vac automatic selection	ok	replace ac-cord 125V/7A
	NETWORK-ANALYSER HP4195A		0.500	48~66Hz 100Vac, 120Vac, 220Vac (±10%) 240Vac +5%, -10%	ok	replace ac-cord 125V/12A
	printer (HP DeskJet 970CXi)		0.100	50/60Hz 100~240Vac	ok	(0.7A)
	printer interface	1ϕ, 100V	0.009	60Hz 120Vac	trafo	
	Tektronix TM502A		0.090	48~440Hz 100, 120Vac(±10%) 1.0A SLOW 250V 220, 240Vac(±10%) 0.5A SLOW 250V	ok	change fuse
1.6			1.424			

LOI HIGH POWER DRIVE SYSTEM



LOI HPD
2nd Harmonc Collaboration
Apr/28/'03, YI