I'm not working on TGC Electronics, but I'd like to show you something about

LSI Design
MDT Frontend Electronics
ATLAS Muon TDC
First Integrated Circuit

Nobel Prize in Physics, Jack Kilby, the invention of the integrated circuit.

A transistor and other components on a slice of germanium, 7/16-by-1/16-inches in size. (1958)
Moore's Law

Year

No. of Transistors

Intel = x20/10 year

KEK = x5/10 year

Slave Board ASIC

Moore's Law
First Microprocessor

Year 1971
2300 transistors
10 $\mu$m technology
Then ....

Pentium II
CMOS Process Technology

- TMC1004
- TMC304
- TMCPHX1
- AMT1

Commercial process
Slave Board ASIC

Design Rule [µm]

Year
Gate Delay and Interconnect Delay

Simple Shift Register

Delay

Gate Delay

Interconnect Delay

Technology

0.1 ns 1 ns 10 ns

2 µm 1.5 µm 1 µm 0.8 µm 0.5 µm 0.35 µm

Good Old Days

Nowadays
MDT Electronics Collaboration

12 production centers
21 Institutes
8 Countries

MDT

ASD -> TDC

Chamber Service Module

Muon Readout Driver

Michigan

KEK, TUA&T

Boston Harvard

NIKEF
ATLAS MDT Frontend Electronics
MDT Readout Flow

<18 Boards / Chamber

MDT Readout Flow

<18 Links / CSM

< 6 Links / MROD

40Mbps LVDS

JTAG, I2C

640 Mbps Fiber

Clock

Faraday Cage

USA15

S-Link

ROB (Readout Buffer)
Block Diagram of the ATLAS Muon TDC

- **Clock (40 MHz)**
- **Inputs (24ch)**
- **Serial Data Out**
- **Strobe Out**
- **JTAG signals**

**Key Components:**
- **Trigger FIFO (25b x 8W)**
- **First Level Buffer (35b x 256W)**
- **Encoder & Formatter**
- **Channel Buffer (44b x 4W)**
- **Parallel to Serial Converter**
- **Readout FIFO (32b x 64W)**
- **Coarse Counter**
- **Parallel to Serial Converter**
- **Trigger Matching**
- **28-bit Write Pointer**
- **28-bit Read Pointer**
- **28-bit Start Pointer**
- **13-bit Fine Time (16b)**
- **PLL**
- **JTAG Controller**

**Specifications:**
- **Parallel to Serial Converter**
- **Clock (40 MHz)**
- **Inputs (24ch)**
- **80 MHz**
- **25-bit Trigger FIFO (25b x 8W)**
- **35-bit First Level Buffer (35b x 256W)**
- **44-bit Channel Buffer (44b x 4W)**
- **32-bit Readout FIFO (32b x 64W)**

**Date:** 99.11.17 Y.Arai
Photograph of the AMT-1 chip
Development of ATLAS MDT TDC (AMT)

- ~370 k channels, 400 kHz input rate, 100 kHz trigger rate.
- Sub-ns timing resolution.
- Leading and trailing edge time measurement.
- Low-cost, Low-power & High-density (24 ch/chip).
- LVDS interface, JTAG control.
- Radiation Tolerant (~11 krad, 1.2x10^{13} n/cm^2).

- Design study in collaboration with CERN/EP -MIC group.
- Quick test chip (AMT-0) in a 0.7 μm process (10 kch)
- Develop a test element group chip (AMT-TEG) in a new 0.3 μm process (Toshiba Gate-Array) which will be used in a final chip.
- Circuit performance test and radiation tolerance test was done.
Voltage Controlled Ring Oscillator

Osc frequency vs Control Voltage ($V_g$)

- 80MHz
- simulation (worst)
- simulation (typical)
- simulation (best)
- measurement
PLL Oscillation Jitter Histogram

$f_{PLL} = 80$ MHz

$V_{dd} = 3.3$ V

$s \sim 130$ ps
PLL Oscillation Stability vs Freq

- PLL Osc Freq [MHz]
- \( \sigma_{tp} \) [ps]
- \( V_{dd} = 3.3V \)
- \( f(PLL):f(IN) = 2:1 \)

PLL Stability vs Vdd

- PLL Osc Freq [MHz]
- \( \sigma_{tp} \) [ps]
- \( f(IN) = 40MHz \)
- \( f(PLL) = 80MHz \)
Channel Buffer Speed

Leading + Trailing edge mode

5ns 5ns 5ns

Leading Edge only mode

9ns 9ns 9ns

Multiple Edge Resolution = 5 ns (Double Edge)
= 9 ns (Single Edge)

Channel Buffer (4 Words)

Input

Channel Controller

Fine Time (Leading Edge)
Fine Time (Trailing Edge)

Coarse Time
Coarse Time

PLL

40 MHz

Clock

80 MHz

to Level 1 Buffer

x24ch

13
Data Transfer Rate to L1 Buffer

Minimum Period required for 100% data
(Leading + Width, Periodical input pulse, 40MHz clock)

No Data Loss

50ns + 25ns x Nch

Min. Period T [ns]

No. of Hit Channels N
AMT-TEG1 Timing Resolution

RMS=305 ps
AMT-TEG1 Differential Nonlinearity

Max=+/−0.14ns, RMS=0.06ns

AMT-TEG1 Integral Nonlinearity

Max=+/−0.13ns, RMS=0.07ns
LVDS Serial Output

Single End

Data

Strobe

Ch1 1.00 VΩ Ch2 1.00 VΩ

25 Apr 2000 16:26:38

LVDS

Data

Strobe

Ch1 300mV Ch3 300mV
Ch2 300mV Ch4 300mV

5 Sep 2000 15:07:45
00.05.02 Y.A.
**AMT-TEG1 Ring Oscillator**

Diagram of the AMT-TEG1 Ring Oscillator with Enable* and Osc Out nodes. The diagram shows a total of 33 stages.

**Frequency vs Dose**

Graph showing the frequency of oscillation (in MHz) versus dose (in krad) before irradiation. The graph includes data points for Chip O and Chip P.

**Chip Current (2 chips) vs Dose**

Graph showing the chip current (in A) versus dose (in krad) before irradiation. The graph includes data points for Chip O+P.
## Summary of Measurements

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<th>Measurements</th>
<th>Requirements</th>
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<tr>
<td><strong>PLL</strong></td>
<td>Freq. = 40 ~ 120 MHz</td>
<td>80 MHz</td>
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<tr>
<td></td>
<td>Vdd = 2.8 ~ 3.8V</td>
<td>3.3V</td>
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<tr>
<td><strong>Coarse Time Counter</strong></td>
<td>120 MHz</td>
<td>&gt; 80 MHz</td>
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<td><strong>LVDS receiver: ΔV</strong></td>
<td>&gt; 100 mV</td>
<td>&gt; 100 mV</td>
</tr>
<tr>
<td></td>
<td>Vcm 0.2 ~ 2.2 V</td>
<td>0.2 ~ 2.2V</td>
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<tr>
<td><strong>LVDS driver (6.5m cable)</strong></td>
<td>&gt; 100 MHz</td>
<td>&gt; 50MHz</td>
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<tr>
<td><strong>Multiple edge resolution</strong></td>
<td>&lt; 5 ns</td>
<td>&lt; 30 ns</td>
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<tr>
<td><strong>L1B input speed</strong></td>
<td>(2 + N) clocks</td>
<td>&lt; (5 + N) clocks</td>
</tr>
<tr>
<td><strong>Time Resolution</strong></td>
<td>305 ps RMS</td>
<td>&lt; 500 ps RMS</td>
</tr>
<tr>
<td><strong>Diff./Int. Non-linearity</strong></td>
<td>&lt; 70 ps RMS</td>
<td>&lt; 300 ps RMS</td>
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<tr>
<td><strong>Radiation hardness for γ</strong></td>
<td>&gt; 30 krad</td>
<td>&gt; 11 krad</td>
</tr>
<tr>
<td><strong>Radiation hardness for n</strong></td>
<td>&gt; 1.6 x 10^{13} n/cm^{2}</td>
<td>&gt; 1.2 x 10^{13} n/cm^{2}</td>
</tr>
</tbody>
</table>
**Power Consumption**

**Simulation:**
- 400 mW (Internal Circuit)
- + 480 mW (16mW x 30 LVDS receivers)
- = ~900 mW/chip

**Measurement:**
- 3.3V x 148 mA = 488 mW/chip (20mW/chan)
- (@400kHz hit, 100kHz Trigger)

**LVDS receiver:**
- New Low Power design will be designed at Toshiba.
- Thus more reduction in power is expected.
Summary

• LSI technology will advance beyond year 2015.
• Design methodology is also changing rapidly.
• We must keep up with this change.
• Challenge to Cost, Complexity, Testability, Radiation damage...

• MDT electronics group are now making 10k channels for MDT test.
• Start system tests in many places.
• AMT-1 chip is working and any serious flaw is not found.
• Final AMT chip (with Low Power LVDS receivers) will be completed in next spring.